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Research paper

Implementation of logic gates using CNFET for energy constraint applications

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Abstract

Since the advent of semiconductors and throughout the history of designing ICs in VLSI for everything from computer hardware to mobile phones, the basic principle of Moore's law has persisted to be the same the number of transistors on a given area of silicon doubles every two years. The transistor rely on today's propelled multicore processors will be arriving at those extent about three billions, a in length best approach starting with the 6800 processor of the mid 1970s which comprised of Exactly 5000 transistors. Semiconductor manufacturing commercial enterprises need aid supporting of the most extreme degree to make this Growth feasible by presenting scaled CMOS gadgets utilizing field impact transistor (FET) technology, the place the most recent hub adequately multiplied those entryway thickness contrasted with those past era each few for A long time. As the approach will be crashing towards sub-nano meter reach that is past 90-nm node, spillage turned into a paramount element. Same time those MOS gadgets arrived at the end of its versatile limit, those semiconductor industry found elective gadget for example, such that CNFET (carbon nano tube field impact transistor), which will be acknowledged to the best decision for following era units. Large portions semiconductor commercial enterprises need aid placing their deliberations On CNFET innovation.

Keywords: *Logic Gates; Ultra-Low Power; Performance; CNTFET; and MOSFET.*

1. Introduction

The most recent few a considerable length of time seen an emotional expansion for nanotechnology Scrutinize. "around others, a standout amongst those The greater part energizing fields will develop is nano electronics, the place An heap from claiming possibilities are showing up in the structure for sensors, actuators, Also transistors, every portrayed Toward characteristic sizes of the request of a couple of nano meters. At this advancement need been fuelled Eventually Tom's perusing the revelation about new materials and the creation about manufacturing systems that permit outline Furthermore advancement toward such each moment scale. Carbon nano tubes are in the bleeding edge of these new materials, because of the exceptional mechanical What's more electronic properties that provide for them, for example, remarkable quality and conductivity. Person energizing plausibility will be those creation of nano meter-scale transistors [1-3] , maybe should be embedded, in the future, inside complex and miniscule electronic circuits that will aggravate today's chips appear gigantic in examination. Moreover, these nano tubes show a enormous current-carrying ability, conceivably permitting for expanded scaling down from claiming high-sounding Also high-potential circuits. In spite of the fact that exactly units have at that point been produced, the innovation is still to its outset when compared to, for instance, that for bulk-silicon MOSFETs. This postulation may be a report card for investigations performed throughout the time 2002-2005 with those UBC Nano electronics Group, for those point about seeing what's more acquiring execution predictions for carbon nano tube field-effect transistors (CNFETs). During the time this research was being conducted, there were few published works illustrating certain phenomena predicted herein [4].

2. Literature review

The essential rule from claiming this sort of transistor might have been to start with protected by Julius Edgar Lilienfeld over 1925. Twenty five a considerable length of time after when chime phone endeavored will patent those intersection transistor, they found Lilienfeld generally considering a patent, worded as it were that might incorporate know sorts for transistors. Chime Labs might have been capable will fill in out a concurrence with Lilienfeld, who might have been even now alive in that run through (it is not referred to though they paid him cash or not). It might have been at that run through those ringer Labs rendition might have been provided for those sake bipolar intersection transistor, or essentially intersection transistor, What's more Lilienfeld's configuration took the sake field impact transistor In 1959, DawonKahng and Martin M. (John) Atalla at Bell Labs invented the Metal–oxide–semiconductor field-impact transistor (MOSFET) concerning illustration a branch of the protected FET plan [5] . Operationally What's more structurally unique in relation to those bipolar intersection transistor, the MOSFET might have been produced Toward executing or neglecting an insulating layer on the surface of the semiconductor et cetera putting a metallic entryway cathode on that. It utilized crystalline silicon to those semiconductor Furthermore a thermally oxidized layer of silicon dioxide for the insu-

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lin. The silicon MOSFET didn't produce restricted electron traps In the interface between the silicon What's more its local oxide layer, Also In this way might have been naturally free from the trapping Furthermore diffusing about transporters that required obstructed those execution for prior field-effect transistors.

3. Related work

The accepted metal–oxide–semiconductor (MOS) structure may be got Eventually Tom's perusing developing a layer of silicon dioxide (SiO2) looking into highest priority on a silicon substrate Furthermore depositing An layer about metal or polycrystalline silicon (the last is ordinarily used). Similarly as the silicon dioxide will be a dielectric material, its structure may be proportional with a planar capacitor, for a standout amongst the electrodes swapped by a semiconductor. The point when a voltage will be connected crosswise over An MOS structure, it modifies the dissemination of charges in the semiconductor. Whether we think about An p-sort semiconductor (with those thickness about acceptors, p those thickness for holes; p = na in impartial bulk), a sure voltage, starting with entryway with form (see figure) makes An exhaustion layer by forcing the positively charged gaps away starting with the gate–insulator/semiconductor interface, taking off uncovered a carrier-free district from claiming immobile, contrarily charged acceptor ions (see doping (semiconductor)). On will be helter skelter enough, a secondary centralization from claiming negative charge transporters manifestations over a reversal layer spotted for a dainty layer following of the interface the middle of that semiconductor and the insulin. Conventionally, the entryway voltage in which the volume thickness of electrons in the reversal layer is those same concerning illustration the volume thickness from claiming gaps in the physique is known as the edge voltage. When those voltages between transistor entryway Also hotspot (VGS) surpass the edge voltage (Vth), it may be known as overdrive voltage.

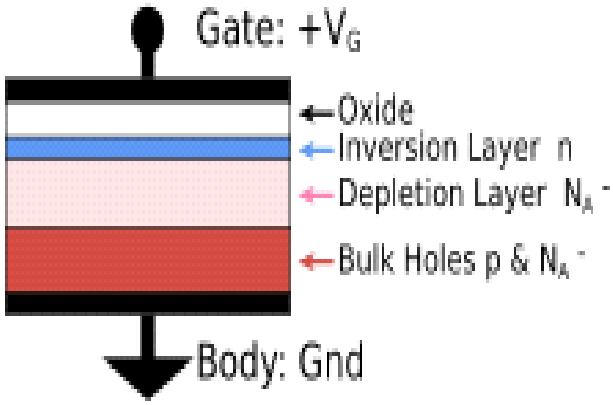


Fig. 1: Metal–Oxide–Semiconductor Structure on P-Type Silicon.

This structure for p-type particular figure is those groundwork of the n-type MOSFET, which obliges s were as about n-type hotspot Also channel areas. The operation of a MOSFET cam wood make differentiated fewer than three different modes, relying upon the voltages at those terminals. In the accompanying discussion, a streamlined mathematical model is utilized. Up to date MOSFET qualities need aid all the more perplexing over the mathematical model exhibited. Ohmic contact on muscle to to guarantee no physique bias; Main left: Sub threshold, top banana right: ohmic mode, bottom left: animated mode In onset for pinch-off, bottom right: animated mode great under pinch-off – channel period regulation obvious. For an enhancement-mode, n-channel MOSFET, those three operational modes are: Cut off, sub threshold, what's more weak-inversion mode.

When $V_{GS} < V_{th}$-

Where Vgs is gate-to-source bias and Vth is the threshold voltage of the device

Over powerless reversal the place the hotspot will be tied to bulk, those current varies exponentially with Vgs Similarly as provided for roughly by.

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}},$$

$$\kappa = \frac{C_{OX}}{C_{OX}+C_D},$$

With Cd = capacitance of the depletion layer and Cox = capacitance of the oxide layer. This equation is generally used, but is only an adequate approximation for the source tied to the bulk. For the source not tied to the bulk, the sub threshold equation for drain current in saturation is

$$I_D \approx I_{D0} e^{\frac{\kappa(V_G-V_{th})-V_S}{V_T}},$$

Where the k is the channel divider that is given by:

$$\kappa = \frac{C_{OX}}{C_{OX}+C_D},$$

For cd = capacitance of the depletion layer Also cox = capacitance of the oxide layer. To An long-channel device, there is no channel voltage reliance of the current When Vds>Vth, However Concerning illustration channel length may be lessened drain-induced boundary bringing down introduces channel voltage reliance that relies On an intricate best approach upon those gadget geometry (for example, the channel doping, those intersection doping along these lines on). Frequently, edge voltage Vth to this mode may be characterized similarly as the entryway voltage In which An chosen quality about present ID0occurs, for example, ID0 = 1 μA, which might not a chance to be those same Vth-value utilized within the equations to the Emulating modes.

3.1. CNFET

A carbon nano tube field-impact transistor (CNFET) alludes should An field-impact transistor [6-8] that uses An solitary carbon nano tube or an exhibit from claiming carbon nano tubes Concerning illustration the channel material As opposed to mass silicon in the accepted MOSFET structure. 1st showed in 1998, there bring been significant developments for CNTFETs [11]

As stated by Moore's law, the extents about individual units clinched alongside an incorporated information preparing have been diminished toward an element about roughly two each two quite some time. This scaling down about units need been the main impetus clinched alongside innovative developments since that late twentieth century. However, Concerning illustration noted Toward ITRS 2009 edition, further scaling down need confronted genuine breaking points identified with creation innovation organization Furthermore gadget exhibitions Similarly as those incredulous extent contracted down on sub-22 nm extent. [3] Those breaking points include electron tunnelling through short channels also slim insulin films, those co-partnered spillage currents, latent force dissipation, short channel effects, Furthermore varieties over gadget structure Also doping. These breaking points might make beat with exactly degree and encourage further scaling down from claiming gadget measurements toward modifying the channel material in the customary heft MOSFET structure for a solitary carbon nano tube or a show of carbon nano tubes [8-9].

3.2. Electronic structure of carbon nanotubes

The exceptional electrical properties of carbon nanotubes arise from the unique electronic structure of grapheme itself that can roll up and form a hollow cylinder. The circumference of such carbon nanotube can be expressed in terms of a chiral vector:

$\hat{C}_h = n\hat{a}_1 + m\hat{a}_2$ which connect two crystal graphically equivalent sites of the two-dimensional grapheme sheet. Here n and m are integers and $\hat{a}_1$ and $\hat{a}_2$ are the unit vectors of the hexagonal honeycomb lattice. Therefore, the structure of any carbon nanotube can be described by an index with a pair of integers (n,m) that define its chiral vector.

In terms of the integers (n,m), the nanotube diameter d_t and the chiral angle θ are given by:

$$d_t = \frac{\sqrt{3} a_{C-C} \sqrt{m^2 + mn + n^2}}{\pi}$$

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}\, n}{2m + n}\right)$$ [5]

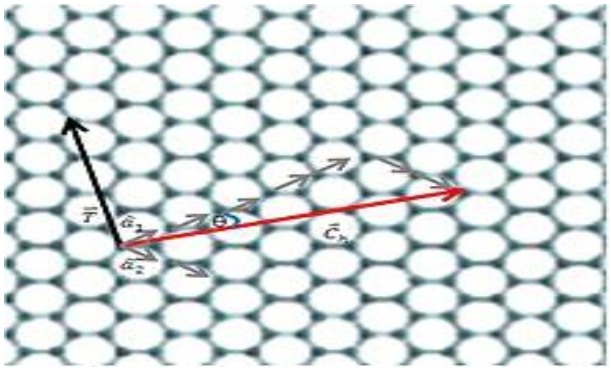


Fig. 2: Graphene Atomic Structure with A Translational Vector T and A Chiral Vector $\hat{C}_h$ of A CNT.

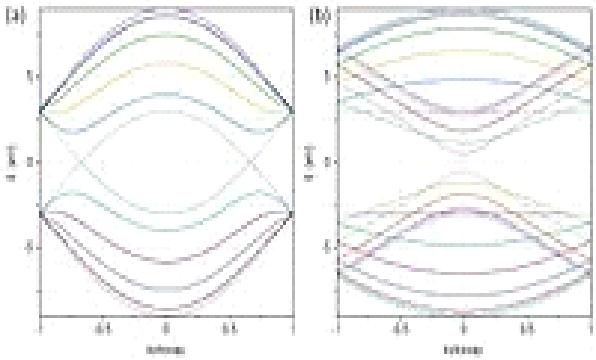


Fig. 3: One-Dimensional Energy Dispersion Relations for (A) (N, M)=(5,5) Metallic Tube, (B) (N,M)=(10,0) Semiconducting Tube.

The differences in the chiral angle and the diameter cause the differences in the properties of the various carbon nanotubes. For example, it can be shown that an (n,m) carbon nano tube is metallic when n = m, has a small gap (i.e. semi-metallic) when n – m = 3i, where i is an integer, and is semiconducting when n – m ≠ 3i.[6] This is due to the fact that the periodic boundary conditions for the one-dimensional carbon nanotubes permit only a few wave vectors to exist around the circumference of carbon nanotubes [7-9].

3.3. Back-gated CNTFETs

The most punctual strategies to fabricating carbon nano tube (CNT) field-effect transistors included pre-patterning parallel strips for metal over An silicon dioxide substrate, and then depositing those CNTs with respect to highest point in a irregular example. The semiconducting CNTs that happened will fall over two metal strips help every last one of necessities vital for a simple field-impact transistor. Particular case metal strip is those "source" contact same time alternate may be those "drain" contact. The silicon oxide substrate might a chance to be utilized similarly as the entryway oxide what's more including a metal contact on the once more makes the semiconducting CNT entryway equipped.

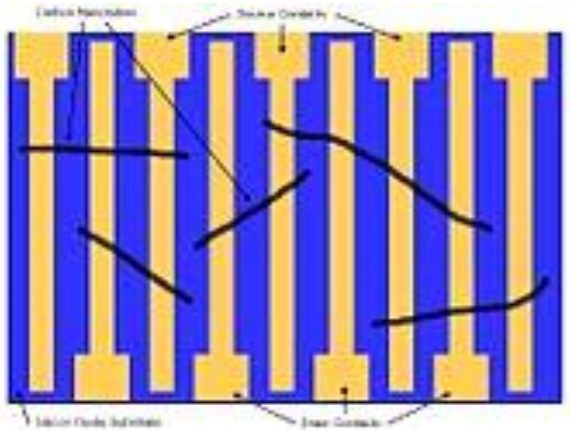


Fig. 2.1: Top View of Carbon Nano Tubes Deposited on A Silicon Oxide Substrate Pre-Patterned with Source and Drain Contacts.

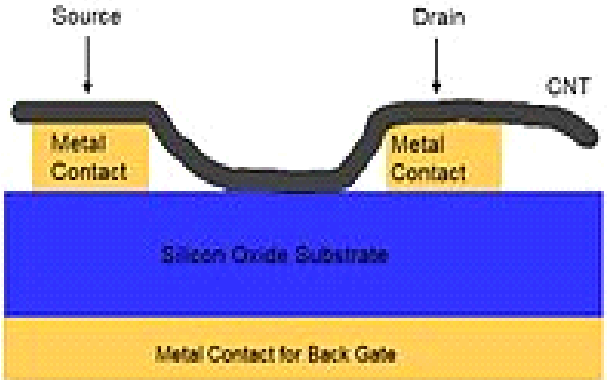


Fig. 2.2: Side View of Carbon Nanotubes Deposited on A Silicon Oxide Substrate Pre-Patterned with Source and Drain Contacts.

4. Implementation

Rationale entryways would the heart from claiming advanced hardware. An entryway will be a electronic gadget which will be used to figure An work with respect to An two esteemed sign. Rationale entryways would those fundamental building square from claiming advanced circuits. Basically, every last bit rationale entryways have one yield and two inputs. Some rationale entryways similar to NOT entryway or inverter need special case enter What's more you quit offering on that one yield. The inputs of the rationale entryways are outlined should accept just double information (only low 0 alternately helter skelter 1) Eventually Tom's perusing accepting the voltage enter. The low rationale level speaks to zero volts and helter skelter rationale level speaks to 3 alternately 5 volts sure supply voltage [10-11].

4.1. Logic gates & their operation with results and discussion

Inverter operation

It is An solitary data gadget which need a yield level that is typically during rationale level "1" What's more dives "LOW" should a rationale level "0" when its absolute enter is during rationale level "1", at the end of the day it "inverts" (complements) its data indicator. Those yield starting with An NOT entryway best returns "HIGH" once more when its enter is In rationale level "0". The circlet for inverter will be indicated to fig.

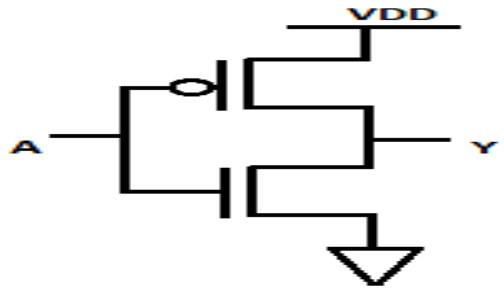


Fig. 3: Inverter Circuit.

Table 1: Truth Table of Inverter

INPUT	OUTPUT
A	Y
0	1
1	0

Inverter out is actualized utilizing CMOS and also CNFET toward an supply voltage of 150 mv On profound sub threshold locale. Those purposes of the out may be watched and the voltage swing will be seen on make secondary toward 150 mv Also low at 0 v. Broad simulations are performed during 16-nm innovation hub and the values need aid tabulated.

Table 2: Design Metrics of Inverter Circuit @ 16 Nm Node

V_{DD}	Inverter	Power (W)	Delay (Sec)	PDP (W-Sec)	EDP (W-Sec^2)
150mV	CMOS based	9.253e-12	6.454e-7	61.461e-19	396.669e-26
	CNFET based	1.152e-14	4.301e-10	4.954e-24	21.307e-34

4.2. AND operation

The output state of a "Logic AND Gate" only returns "LOW" again when any of its inputs are at a logic level "0". In other words for a logic AND gate, any LOW input will give a LOW output.

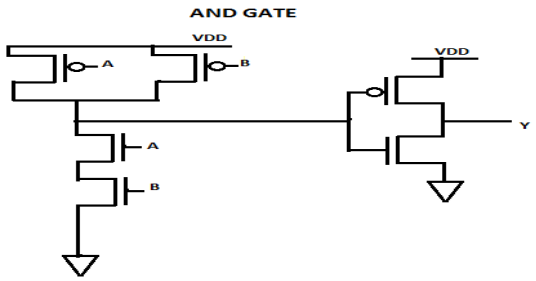


Fig. 3.1: AND Gate.

Table 2: Truth Table of AND Gate

INPUTS		OUTPUTS
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND circuit is implemented using CMOS as well as CNFET at a supply voltage of 150 mV in deep sub threshold region. The functionality of the circuit is observed and the voltage swing is seen to be HIGH at 150 mV and LOW at 0 V. Extensive simulations are performed at 16-nm Technology node and the values are tabulated.

Table 3: Design Metrics of AND Gate Circuit @ 16 Nm Node

V_{DD}	AND GATE	Power (W)	Delay (Sec)	PDP (W-Sec)	EDP (W-Sec^2)
150mV	CMOS based	2.612e-11	3.124e-7	8.159e-18	25.488e-25
	CNFET based	4.136e-13	2.370e-9	9.802e-22	23.230e-31

4.3. OR operation

The output, Y of a "Logic OR Gate" only returns "LOW" again when ALL of its inputs are at a logic level "0". In other words for a logic OR gate, any "HIGH" input will give a "HIGH", logic level "1" output [10].

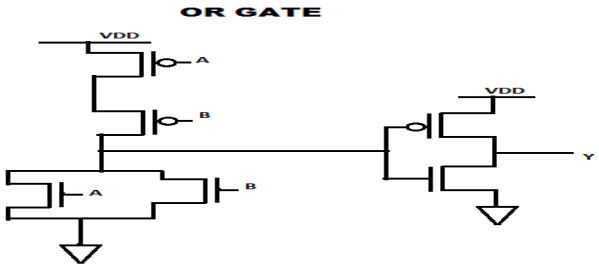


Fig. 3.2: OR Gate Circuit.

Table 3: Truth Table of OR Gate

INPUTS		OUTPUTS
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

4.4. OR

Circuit is implemented using CMOS as well as CNFET [11] at a supply voltage of 150 mV in deep sub threshold region. The functionality of the circuit is observed and the voltage swing is seen to be HIGH at 150 mV and LOW at 0 V. Extensive simulations are performed at 16-nm Technology node and the values are tabulated

4.5. NAND operation

When the both inputs A & B is high then only the output Y is low and in all the remaining conditions the output is high. It is the complement of AND gate.

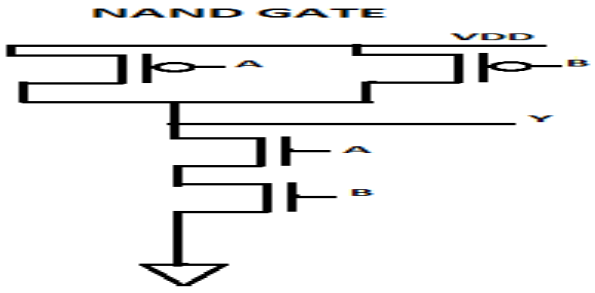


Fig. 3.3: NAND Gate.

Table 4: Truth Table of NAND Gate.

INPUTS		OUTPUTS
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND circuit is implemented using CMOS as well as CNFET at a supply voltage of 150 mV in deep sub threshold region. The functionality of the circuit is observed and the voltage swing is seen to be HIGH at 150 mV and LOW at 0 V. Extensive simulations are performed at 16-nm Technology node and the values are tabulated.

Table 4.1: Design Metrics of NAND Gate Circuit @ 16 Nm Node

V_{DD}	NAND GATE	Power (W)	Delay (Sec)	PDP (W-Sec)	EDP (W-Sec^2)
150mV	CMOS based	4.257e-11	3.154e-7	13.426e-18	42.345e-25
	CNFET based	1.158e-13	1.182e-9	1.368e-22	1.616e-31

Table 4.2: Design Metrics of NAND Gate Circuit @ 16 Nm Node

V_{DD}	NOR GATE	Power (W)	Delay (Sec)	PDP (W-Sec)	EDP (W-Sec^2)
150mV	CMOS based	5.256e-11	7.240e-7	38.053e-18	275.503e-25
	CNFET based	9.952e-14	5.720e-9	56.925e-23	325.611e-32

5. XOR operation

The truth table above shows that the output of an Exclusive-OR gate ONLY goes “HIGH” when both of its two input terminals are at “DIFFERENT” logic levels with respect to each other. If these two inputs, A and B are both at logic level “1” or both at logic level “0” the output is a “0” making the gate an “odd but not the even gate”. In other words, the output is “1” when there are an odd number of 1’s in the inputs.

XOR circuit is implemented using CMOS as well as CNFET at a supply voltage of 150 mV in deep sub threshold region. The functionality of the circuit is observed and the voltage swing is seen to be HIGH at 150 mV and LOW at 0 V. Extensive simulations are performed at 16-nm Technology node and the values are tabulated in Table. 4.12.

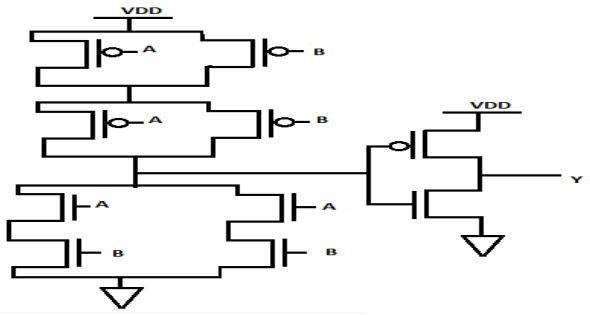


Fig. 3.4: EXOR Gate.

INPUTS		OUTPUTS
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Table 4.4: Design Metrics of XNOR Gate Circuit @ 16 Nm Node

V_{DD}	XNOR GATE	Power (W)	Delay (Sec)	PDP (W-Sec)	EDP (W-Sec^2)
150mV	CMOS based	6.589e-11	6.561e-7	43.230e-18	283.632e-25
	CNFET based	1.697e-13	4.357e-9	7.393e-22	32.211e-31

6. Conclusion

Two novel high-performance ternary full adder cells have been proposed based on CNFET. The proposed circuits have been designed based on multiple-vth devices by utilizing unique characteristics of CNFET. Simulation results indicate the superiority of the proposed designs in terms of delay and pdp compared to the other existing circuits in various conditions.

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