International Journal of Engineering & Technology, 7 (4.30) (2018) 234-239

SPC

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper



Analysis of Symmetric and Asymmetric Multilevel Inverter Topologies Using Reduced Number of Switching Devices Circuit Structure

M. H. Yatim[1*], A. Ponniran[2], A. A. Bakar[3], A. N. Kasiran[4], M. K. R. Noor[5], J.N. Jumadril[6]

[1,2,3,4,5,6] *Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Malaysia*
**Corresponding author E-mail: fizieizi69@gmail.com*

Abstract

This paper presents symmetric and asymmetric multilevel inverter principles using reduced number of switching devices circuit structure. Principally, asymmetric multilevel inverter topology able to produce higher output voltage level without modification of the structure in order to reduce total harmonic distortion at the output voltage. In contrast, the number of switching devices need to be increased with symmetric principle when higher output voltage level is considered. In this study, 5-level reduced number of switching devices circuit structure is selected as a circuit configuration for symmetric (5-level structure) and asymmetric (7-level and 9-level structures) multilevel inverters. For switching strategy, modified pulse width modulation and sinusoidal pulse width modulation are selected to produce output voltage levels of the inverter. Modified pulse width modulation used low switching frequency in producing signal and needs higher output voltage levels to achieve low total harmonic distortion. In contrast, sinusoidal pulse width modulation used high switching frequency in order to minimize total harmonic distortion. Theoretically, total harmonic distortion is reduced when number of output voltage level is increased for both cases. The findings show that, the 9-level asymmetric topology has lower total harmonic distortion compared to the 5-level symmetric topology and 7-level asymmetric topology, whereby these inverters using the same circuit configuration. The results show that, the total harmonic distortions of 9-level asymmetric topology, 7-level asymmetric topology and 5-level symmetric topology are 14.54%, 18.08% and 26.92%, respectively with sinusoidal pulse width modulation switching strategy. Meanwhile, with modified pulse width modulation switching strategy, the total harmonic distortions of 9-level asymmetric topology, 7-level asymmetric topology and 5-level symmetric topology are 18.7%, 21.68% and 28.99%, respectively. Therefore, 9-level asymmetric with sinusoidal pulse width modulation switching strategy show the lowest total harmonic distortion with optimum number of switching devices.

Keywords: *Pulse Width Modulation; Sinusoidal Pulse Width Modulation; Symmetric and Asymmetric Multilevel Inverter; Total Harmonic Distortion.*

1. Introduction

Generally, power inverters are one of converter that converting direct current (DC) to alternating current (AC) for any systems that required this type of power conversion [1]. Multilevel inverters (MLI) have become a selection for uses in electric utility and for medium to high power industrial applications. In a recent number of years, the industry has begun to request greater power equipment, which now reaches the megawatt level and start to grow even further. For these causes, MLI have been developed as the key for working with higher voltage levels. Generally, MLI consists of an array of power semiconductors and direct current (DC) voltage sources, then the output voltages with stepped waveforms will be generated. MLI consists of three main different topologies, i.e., neutral point clamp multilevel inverter (NPCMLI), flying capacitor multilevel inverter (FCMLI) and cascaded H-bridge multilevel inverter (CHBMLI) [2]. Specifically, multilevel inverter has the advantages of generating better output quality by consideration number of level and modulation technique used [3]. For example, by considering suitable design of modified pulse width modulation (MPWM) technique, inverters are able to eliminate unwanted harmonic.

Currently, there are numerous of researches conducted referring to these three main topologies. Basically, the primary objective in creating multilevel inverters is to maintain a low harmonic distortion (THD) at output side by considering less numbers of semiconductor devices [4][5]. Several improvements had been done in order to produce high efficiency converter. For example, several researchers are focusing on reducing semiconductor devices by rearranging the circuit configuration [6][7]. Several topologies had been introduced in order to reduce the number of semiconductor devices such as symmetric multilevel inverter (SMLI) and asymmetric multilevel inverter (AMLI) which improve conventional multilevel inverter structures. Generally, the asymmetric topology which can be reducing the number of semiconductor devices that implemented in the conventional inverter structure. Then, almost half the numbers of semiconductor devices can be reduced [8]. Therefore, power losses in semiconductor devices especially switching loss can be drastically reduced. The obvious difference between symmetric and asymmetric is the DC sources. Whereby, in symmetric topology all DC sources voltage are same, meanwhile in asymmetric topology each DC source voltage is different [9]. These two topologies had been selected and become the main focus in this study.

This paper focuses on symmetric and asymmetric multilevel inverter topologies by using two modulation techniques, i.e., modi-

Copyright © 2018 Authors. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

fied pulse width modulation (MPWM) and sinusoidal pulse width modulation (SPWM). Total harmonic distortion (THD) is observed in simulation of SMLI and AMLI by using MPWM and SPWM techniques. Therefore, simulation works are conducted in order to confirm the principles of SMLI and AMLI

2. Multilevel Inverter

Figure 1 is the illustration of the concept for symmetric and asymmetric topologies. The concept of symmetric topology is same with cascaded H-bridge topology which increase number of switching devices to achieve higher level of output voltage. In contrast, asymmetric topology used the same number of switching device as symmetric topology to achieve higher level of output voltage [10]. In this study, 5-level cascaded H-bridge structure is selected to implement symmetric and asymmetric topologies. From Fig. 1, it shows that by maintaining the number of switching devices in 5-level symmetric can increase the number of output level using asymmetric topology. Therefore, using asymmetric topology in cascaded H-bridge structure automatically can reduced the number of switching devices in order to achieve higher level of output voltage.

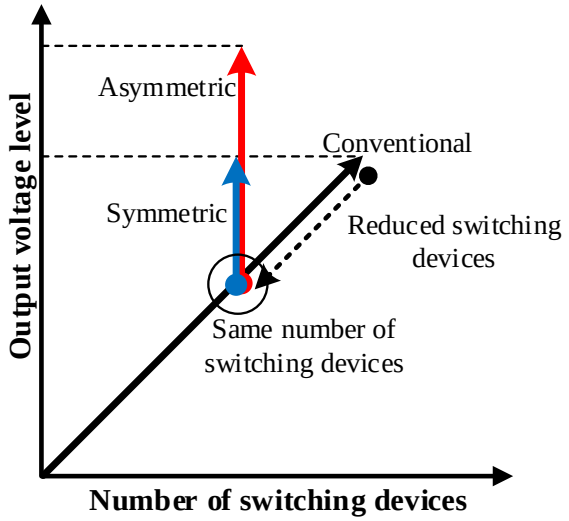


Fig. 1: Symmetric and asymmetric concept

2.1. Cascaded H-Bridge principle

Cascaded structure includes several modules and each module consists of a DC source and four switches in H-bridge configuration. Each module able to generate two and three output voltage levels. The conventional cascaded shows the number of level proportional to the number of switching devices. To determine the N-level of structure, expression N_{level} = 2n + 1 is used where n is number of DC source. Thus, in order to generate 9-level output voltage, four modules consist of four separated DC sources must be considered and expression N_{sw} = 6(n-1) is used to estimate the required number of switching devices. Figure 2 shows the N-level, single-phase CHBMLI. The AC output voltage of each module is connected in series in order to form an output voltage, V_{out}. The number of H-bridge module (M), depends on the number of levels (N) required and can be written as M = (N-1)/2.

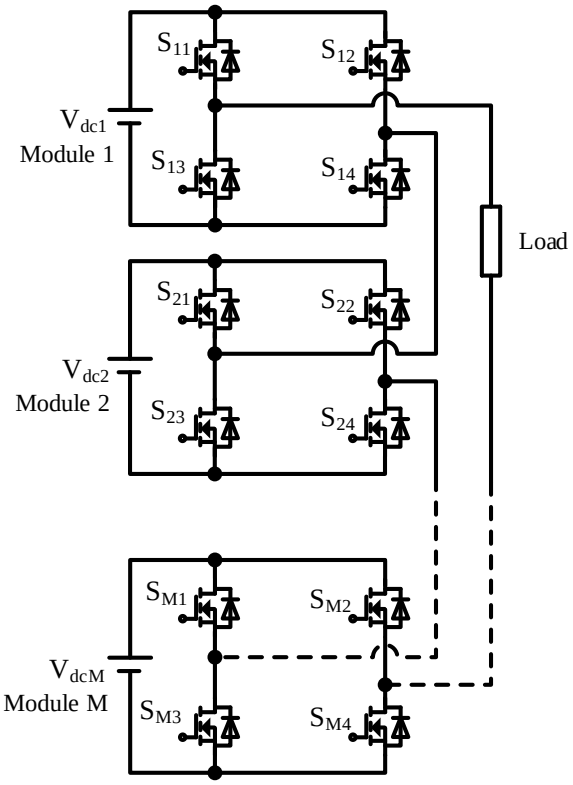


Fig. 2: Structure of Cascaded H-Bridge MLI

2.2. Symmetric and asymmetric MLI principles

In reduced number of switching devices circuit structure, the DC voltage may or may not be equal. If DC voltage given to all source is same, the converter is called symmetric multilevel inverter (SMLI). Otherwise, if DC voltage is different, then it is called asymmetric multilevel inverter (AMLI). SMLI principle is same as CHBMLI principle where the number of output level depends to the numbers of switches. In AMLI, DC voltage with ratio binary and ternary are the most popular [11]. In binary progression, the DC voltages have ratio of 1: 2: 4: 8. . : 2N and the maximum voltage output would be (2N-1) V and the voltage levels will be (2N+1-1). While in the ternary progression shows the amplitude of DC voltages have ratio of 1: 3: 9: 27. . : 3N and the maximum output voltage reaches to ((3N- 1)/2) V and the voltage levels will be (3N). Common advantage of asymmetric topology is, it able to generate high level of output voltage by using the same structure of symmetric topology. As an example, for asymmetric topology with different DC voltages, i.e., Vdc1 = Vdc, Vdc2 = 2Vdc, Vdc3 = 4Vdc, Vdc4 = 8Vdc and so on compared to symmetric topology, i.e., Vdc1=Vdc2=Vdc3. Asymmetric topology with the DC sources has different values and modulation technique is complex and can upgrade the level up to two level higher. Figure 3 shows the circuit structure that been selected for 5-level SMLI and 7-level AMLI while Fig.4 shows the circuit structure for 9-level AMLI where there is an additional switch. Based on circuit structure, it able to generate five level of output voltages. By applying asymmetric principle in this structure, it able to generate up to seven and nine level of output voltages. 16 switches are needed for the conventional cascaded structure to generate nine level of output voltages compared to AMLI which just needed 7 switches to produce nine level of output voltages. Therefore, the number of switching devices and switching loss are reduced.

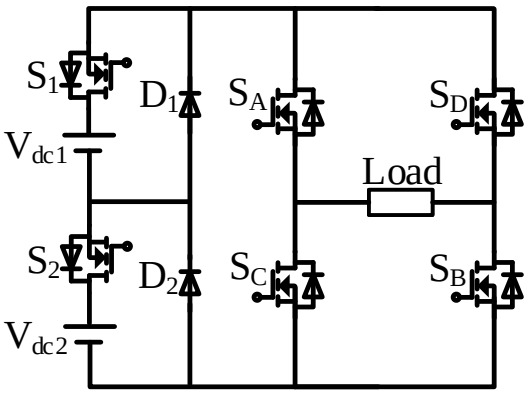


Fig. 3: Circuit structure for 5 level SMLI and 7 level AMLI

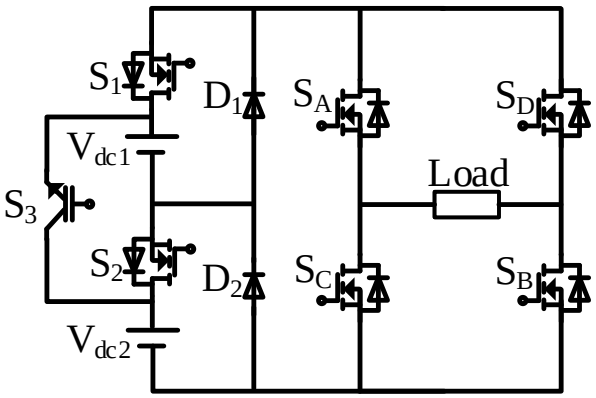


Fig. 4: Circuit structure for 9 level AMLI

2.3. Modulation techniques

Modified Pulse Width Modulation (MPWM) is a technique to generate low frequency output signals from high frequency pulses. Based on MPWM concept, if a duty cycle changed sinusoidally, a sinusoidal voltage can be generated at the output. In its simplest form PWM output signals are constructed by comparing two control signals as shown in Fig.4, several carrier signals and a modulation signal is known as sinusoidal PWM [12]. The carrier signal is a high frequency of triangular waveforms. If the peak of the modulation is less than the peak of the carrier signal, the output will follow the shape of the modulation signal.

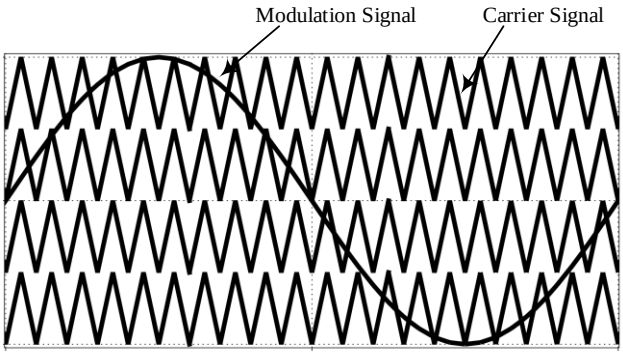


Fig. 5: Sinusoidal PWM

Generation of MPWM and SPWM switching signals are based on the operation mode of circuit structure. Table 3 shows the switching sequence to generate 5-level SMLI that the highest level is +2Vdc. Two DC voltages connected as the input sources and summation both voltages generate the level of output voltage by switching 'ON' of S1, S2, SA and SB. Then, +Vdc generated when the circuit operated and connecting only one DC voltage in 'ON' state of S2, SA and SB. If only SA is 'ON', the output voltage is 0 V.

Table 1: Switching sequence for 5-level symmetric cascaded MLI

V_{out}	S_1	S_2	S_A	S_B	S_C	S_D
$+2V_{dc}$	1	1	1	1	0	0
$+V_{dc}$	0	1	1	1	0	0
0	0	0	1	0	0	0
$-V_{dc}$	0	1	0	0	1	1
$-2V_{dc}$	1	1	0	0	1	1

Tables 2 and 3 show the switching sequence for 7-level and 9-level ACMLI, respectively. Output voltage for SCMLI is a summation between two DC voltages. Different with ACMLI, whereby the output voltage generated involves the addition and subtraction operations between two DC sources in order to generate higher level with regard to the structure capability. The modulation technique for ACMLI is complicated compared to the SCMLI, whereby the level of output voltage need to be specified accordingly.

Table 2: Switching sequence for 7-level asymmetric cascaded MLI

V_{out}	S_1	S_2	S_A	S_B	S_C	S_D
$+3V_{dc}$	1	1	1	1	0	0
$+2V_{dc}$	0	1	1	1	0	0
$+V_{dc}$	1	0	1	1	0	0
0	0	0	1	0	0	0
$-V_{dc}$	1	0	0	0	1	1
$-2V_{dc}$	0	1	0	0	1	1
$-3V_{dc}$	1	1	0	0	1	1

Table 3: Switching sequence for 9-level asymmetric cascaded MLI

V_{out}	S_1	S_2	S_3	S_A	S_B	S_C	S_D
$+4V_{dc}$	1	1	0	1	1	0	0
$+3V_{dc}$	0	1	0	1	1	0	0
$+2V_{dc}$	0	0	1	1	1	0	0
$+V_{dc}$	1	0	0	1	1	0	0
0	0	0	0	1	0	0	0
$-V_{dc}$	1	0	0	0	0	1	1
$-2V_{dc}$	0	0	1	0	0	1	1
$-3V_{dc}$	0	1	0	0	0	1	1
$-4V_{dc}$	1	1	0	0	0	1	1

Tables 1, 2 and 3 can be used for both modulation techniques, MPWM and SPWM which the circuit operation mode is same. The different between these two modulation techniques is the quality of the output voltage generate by the circuit structure. Theoretically, SPWM able to produce higher quality of the output voltage than MPWM.

2.4. Symmetrical and asymmetrical features

2.4.1. Features

The implementation of SMLI and AMLI is same but the DC voltages are different for both topologies. Table 4 shows the details about the principle and difference between these topologies. Principally, AMLI is better in terms of THD and number of switches compared to the SMLI, where the AMLI able to generate higher level of output voltage using the same circuit of SMLI. Ternary method has a potential to generated two levels of output voltage higher than SMLI. Some structures need a combination of two topologies to create an AMLI, however by using this circuit structure, SMLI and AMLI topologies can be applied because the structure is appropriate. Specifications of SMLI and AMLI in this study is shown in Table 5.

Table 4: Comparison of symmetric and asymmetric principles

	Symmetric multilevel inverter	Asymmetric multilevel inverter	
		Binary	Ternary
Number of dc	N	N	N

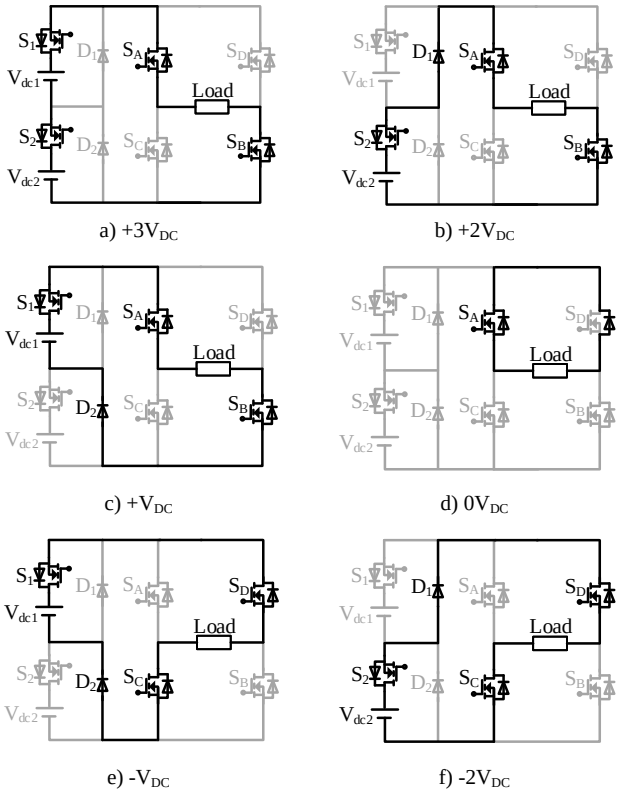
voltage			
Dc voltage	$V_{dc1}=V_{dc2}$	V_{dc1}, $V_{dc2}=2V_{dc1}$	V_{dc1}, $V_{dc2}=3V_{dc1}$
Number of switches	4N	4N	4N
Output level	2N+1	2^{N+1}-1	3^N
$V_{out\ max\ (pu)}$	N	2^N-1	$(3^N-1)/2$
Potential to generate higher level	No	Up to one level higher	Up to two level higher

Table 5: Specification of symmetric and asymmetric features

	Symmetric multi-level inverter	Asymmetric multilevel inverter	
		Binary	Ternary
Number of dc voltage	2	2	2
Dc voltage	V_{dc1} = 170 V V_{dc2} = 170 V	V_{dc1} = 113 V V_{dc2} = 226 V	V_{dc1} = 85 V V_{dc2} = 255 V
Number of switches	8	8	8
Output level	5	7	9
$V_{out\ max\ (pu)}$	2	3	4

2.4.2. Operation mode

Operation mode shown in Fig. 6 is for 5-level SMLI and 9-level AMLI. Figure 6(a) shows the operation of SMLI and AMLI to generate the highest level for each circuit where the summation between both DC voltages produce +2Vdc and +3Vdc consecutively. In order to generate +2Vdc for AMLI and +Vdc, only second DC voltage connected as shown in Fig. 6(b) to create the level. Voltage +Vdc for 7-level AMLI is produced by connecting Vdc1 in the operation of the circuit shown in Fig. 6(c). To obtain zero level, none of the DC voltages is connected for both topologies.



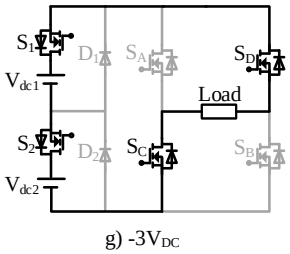
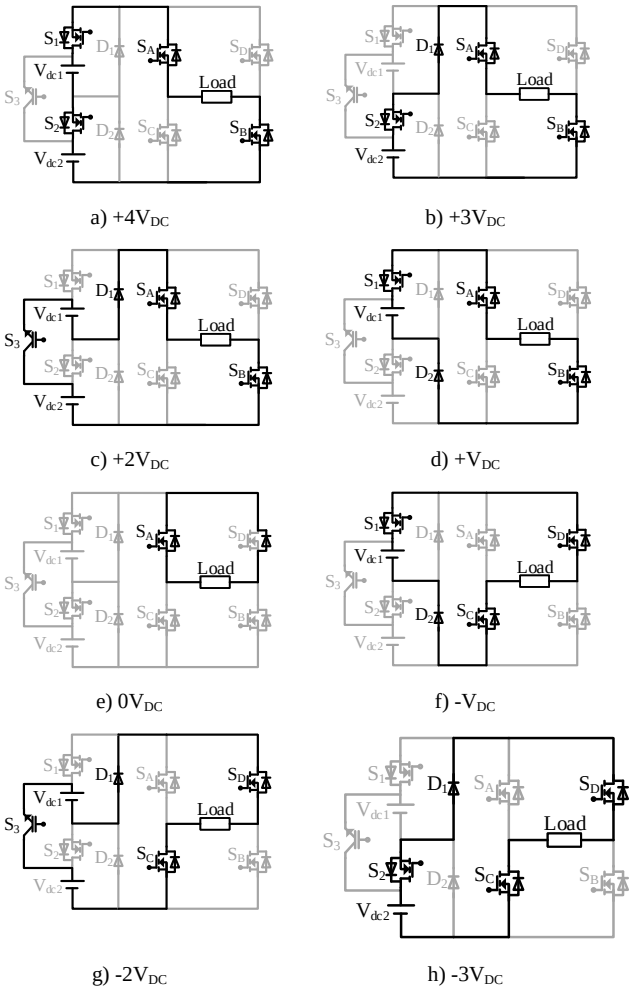
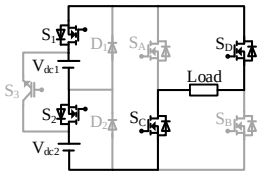


Fig. 6: Mode of operation for 5-level SMLI and 7-level AMLI

Operation mode shown in Figure 7 is for 9-level AMLI. Figure 7(a) shows the operation of AMLI to generate the highest level where the summation between both DC voltages produce +4Vdc. In order to generate +3Vdc for AMLI, only second DC voltage connected as shown in Figure 7(b) to create the third level. The subtraction between Vdc2 and Vdc1 is shown in Figure 7(c), it generates +2Vdc for AMLI as the second level. Voltage +Vdc is produced by connecting Vdc1 in the operation of the circuit shown in Figure 7(d). To obtain zero level, none of the DC voltages is connected as shown in Figure 7(e). Based on the operation mode for both topologies, it shows that SMLI does not involve subtraction between DC voltages to generate output level but AMLI involves the subtraction operation in order to produce another level. Therefore, different DC voltages help AMLI to increase the level of output voltage compared to SMLI.





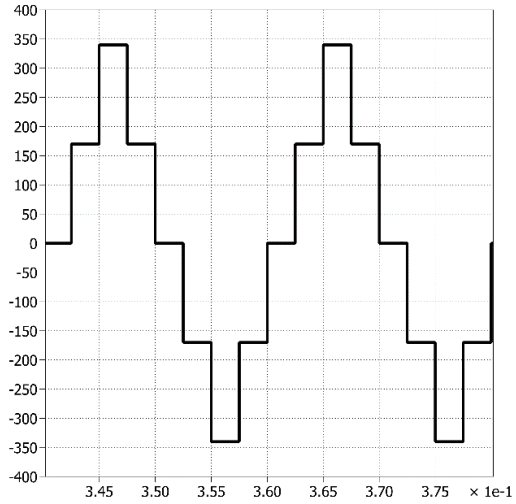
i) -4V_{DC}

Fig. 7: Mode of operation asymmetric 9 level MLI

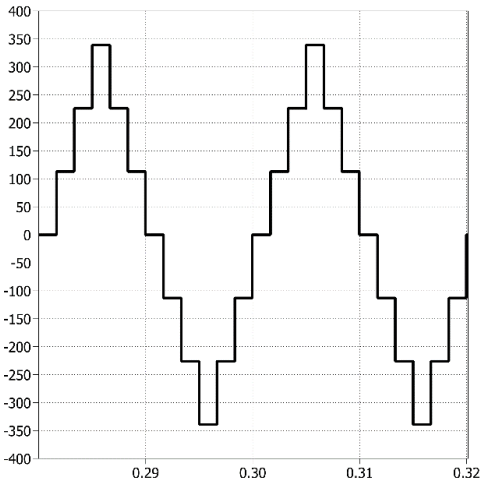
3. Results and analysis

3.1. Simulation result using MPWM

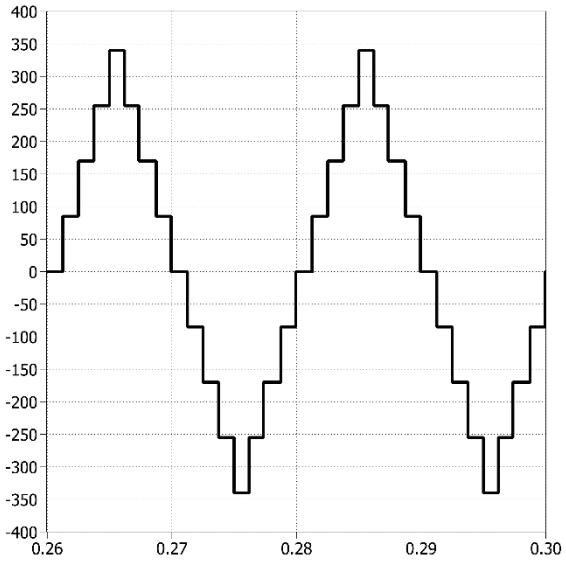
Figure 8 shows the results of SMLI and AMLI using MPWM technique. Figure 8(a) shows the simulation result of the 5-level output voltage of SMLI, it proves this structure only able to generate five levels of the output voltage by connecting two same DC voltages. Figure 8(b) shows the results for 7-level of output voltage of the AMLI with different DC voltages, i.e., Vdc1=113 V and Vdc2=226 V using the same circuit structure of the SMLI. It proves the switching sequence of Table 2 able to generate up to seven voltage levels. Furthermore, by applying switching sequence of Table 3 in the same circuit with different DC voltages, Vdc1=85 V and Vdc2=255 V, it able to generate up to nine levels of output voltage as shown in Fig. 8(c). The principle of symmetric and asymmetric MLI are proved by the simulation results. Switching frequency for the MPWM is 50 Hz and the output frequency is 50 Hz as well.



a) 5-level SMLI



b) 7-level AMLI

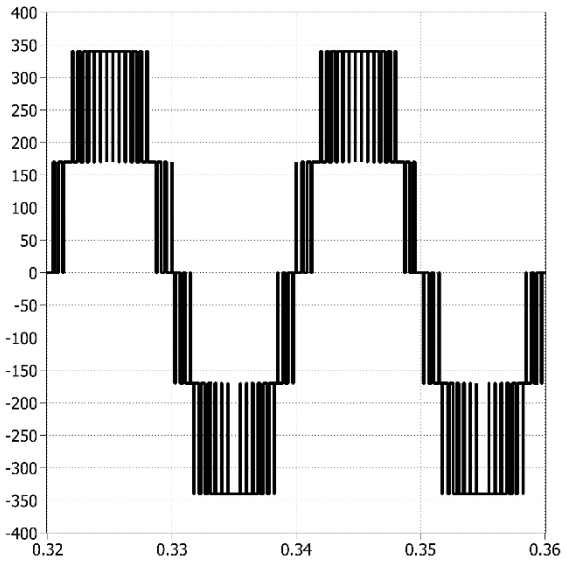


c) 9-level AMLI

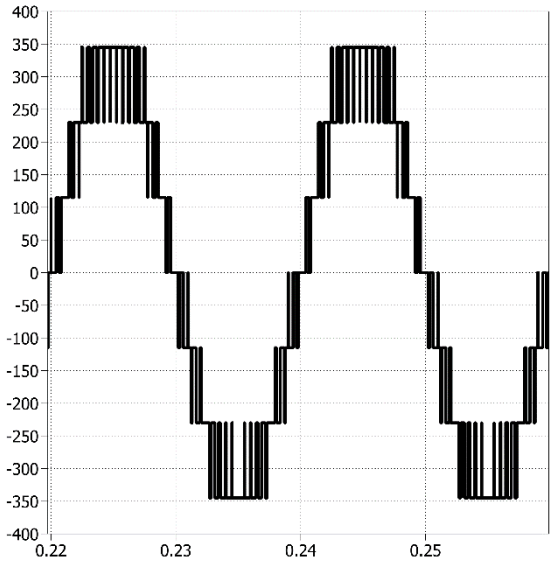
Fig. 8: Simulation results using MPWM

3.2. Simulation result using SPWM

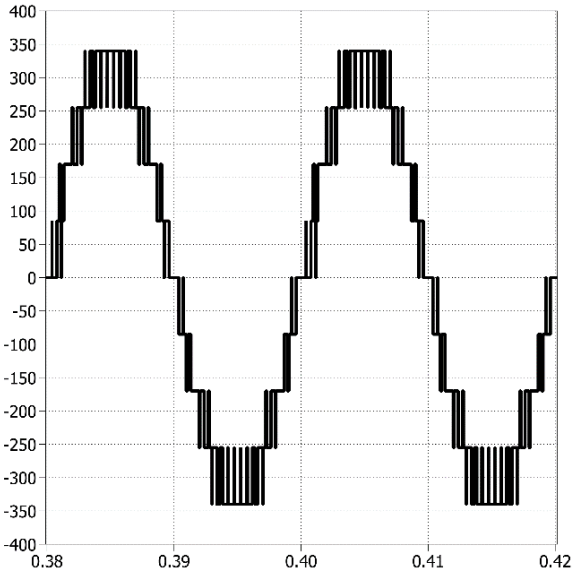
Figure 9 shows the results of SMLI and AMLI using SPWM technique. Figure 9(a) shows the simulation result for 5-level output voltage of SMLI, it proves this structure only able to generate five levels by two same DC voltages. Figure 9(b) shows the results for 7-level of output voltage of the AMLI with different DC voltages, Vdc1=113 V and Vdc2=226 V using the same circuit structure of the SMLI. It proves the switching sequence of Table 2 able to generate up to seven voltage levels. Furthermore, by applying switching sequence of Table 3 in the circuit that added an additional switch with different DC voltages, Vdc1=85 V and Vdc2=255 V, it able to generate up to nine levels of output voltage as shown in Fig. 9(c). The principle of symmetric and asymmetric MLIs are proved by the simulation results. The switching frequency for the SPWM is 2 kHz and the output frequency are 50 Hz.



a) 5-level SMLI



b) 7-level AMLI



c) 9-level AMLI

Fig. 9: Simulation results using SPWM

3.2. Total Harmonic Distortion (THD)

THD results of the SMLI and AMLI for MPWM and SPWM is shown in Table 5. Referring to the 5, 7 and 9 levels of the MLIs, the SPWM shows the lowest THD content compared to the MPWM. Thus, the quality of output voltage from the SPWM is higher (closer to sinusoidal waveform) compared to MPWM.

Table 5: THD based on topologies structure and level of output voltage using MPWM and SPWM

Topology	Level of Output Voltage	THD%	
		MPWM	SPWM
SCMLI	5	28.99	26.82
ACMLI 1	7	27.80	18.08
ACMLI 2	9	18.70	14.54

4. Conclusion

In this paper, comparison between symmetric and asymmetric MLIs is analysed based on two modulation techniques, i.e., MPWM and SPWM, in order to observe the THD performance at the output voltage. From the results, it has been observed that by increasing output level of MLI, the THD is reduced significantly. In this study, asymmetric MLI shows the lowest THD by producing the highest level which is 9 by using the same circuit structure with symmetric MLI and an additional switch. Between MPWM and SPWM techniques, SPWM shows lower THD than MPWM. The finding shows, asymmetric MLI of 9-level with SPWM switching technique produces the lowest THD compared to others.

Acknowledgement

The authors would like to express their appreciation to the Universiti Tun Hussein Onn Malaysia for the funding support, research grants GPPS Vot H029, Tier 1 Vot U858 and Research Fund, UTHM.

References

[1] Malinowski M, Gopakumar K, Rodriguez J & Perez MA, "A Survey on Cascaded Multilevel Inverters", IEEE Trans. Ind. Electron., Vol. 57, No. 7, (2010), pp. 2197–2206.

[2] Babaei E, Alilu S, Laali S & Member S, "A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge", IEEE Trans. Ind. Electron., Vol. 61, No. 8, 2014, pp. 3932–3939.

[3] Jimenez OL, Vargas RA, Aguayo J, Arau JE, Vela G & Claudio A, "THD in cascade multilevel inverter symmetric and asymmetric", Proc. - 2011 IEEE Electron. Robot. Automot. Mech. Conf. CERMA, (2011), pp. 289–295.

[4] Mosa M, Balog RS, Abu-Rub H & Elbuluk M, "A modified symmetric and asymmetric multilevel power inverter with reduced number of power switches controlled by MPC", in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), (2017), pp. 488–493.

[5] Mokhberdoran A & Ajami A, "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology", IEEE Trans. Power Electron., Vol. 29, No. 12, 204, pp. 6712–6724.

[6] Zinoviev GS & Lopatkin NN, "Evolution of multilevel voltage source inverters", in 2008 9th International Conference on Actual Problems of Electronic Instrument Engineering, (2008), Vol. 1, pp. 125–136.

[7] H HH, P A, K NA, H MA, G DA, Yatim MH, "A Single Phase 7-Level Cascade Inverter Topology with Reduced Number of Switches on Resistive Load by Using PWM", J. Phys. Conf. Ser., Vol. 995, No. 1, pp. 12061, 2018.

[8] Landge SS, Kamble VS & Shingare SS, "Simulation of Seven Level Asymmetric Multilevel Inverter", Int. J. Electr. Electron., Vol. 4, No. 1, (2014), pp. 187–196.

[9] Prathiba T & Renuga P, Performance analysis of symmetrical and asymmetrical cascaded H bridge inverter, Vol. 13. 2013.

[10] Yatim MH, Ponniran A, Zaini MA, Shaili MS, Ngamidun NAS, & Kasiran AN, "Symmetrical and Asymmetrical Multilevel Inverter Structures with Reduced Number of Switching Devices", Indones. J. Electr. Eng. Comput. Sci., Vol. 11, No. 1, (2018), pp. 144–151.

[11] Chaudhari HN, Patel DA, Patel DM & Chaudhari MA, "Comparison of Symmetrical and Asymmetrical Cascaded Current Source Multilevel Inverter", Int. J. Res. Eng. Technol., (2013), pp. 175–178.

[12] Lu Y. Jiao PP & Zhang B, "The principle and realization of single-phase SPWM wave based on the counter method", 2012 3rd Int. Conf. Syst. Sci. Eng. Des. Manuf. Informatiz. ICSEM 2012, Vol. 1, (2012), pp. 10–13.