International Journal of Engineering & Technology, 7 (4.4) (2018) 19-20

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design of Falling-Edge Triggered T Flip-Flop based on Quantum-Dot Cellular Automata

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Abstract

A T flip-flop, which is an essential element of a counter, has been proposed as various types of quantum-dot cellular automata (QCA) circuits, but practicality is not expected because there is no clock in circuit. A T flip-flop is a circuit which outputs value changing in synchronization with the rising or falling edge of a clock. In a QCA circuit, a clock pulse generator outputs the time at which the clock changes and it is required for the circuit. In this paper, we propose a falling-edge triggered T flip-flop based on QCA.

Keywords:: Nanotechnology, Quantum-Dot Cellular Automata, T Flip-Flop.

1. Introduction

Complementary metal-oxide-semiconductor (CMOS) technology has been able to sustain Moore's Law, but now device size has reached its limit and the need for new alternative technologies has increased [1]. Quantum-dot cellular automata (QCA), which emerged as a new alternative, are attracting attention as nanoscale size and low power consumption [2], and various logic circuits from basic gate unit to sequential circuit have been proposed in QCA [3-4].

A flip-flop, one of the sequential circuits, is a circuit that stores and holds information. The T flip-flop is called a toggle flip flop and is a circuit used to configure the counter. T flip-flops can be classified into rising-edge triggered and falling-edge triggered flip-flops depending on the clock signal. The state of the output value changes depending on when the clock rises or falls. Conventional QCA T flip-flop circuits ignore this and use only T as an input to design relatively simple. However, in this paper, we design a clock pulse generator that generates a clock change point and propose a more practical T flip-flop by connecting it with a T flip-flop. We also design a new type of T flip-flop that reduces the number of cells and area compared with existing circuits.

2. Related Work

a. QCA Basic Fundamentals

The QCA circuit consists of quantum cells and wires. Fig. 1 (a) shows the two values of a quantum cell. A quantum cell has two transient electrons that can be tunneled between quantum dots and is always located diagonally due to coulombic repulsion [5]. Fig. 1 (b) shows the wiring connected to the general cell. Each cell in the wire propagates the signal due to the repulsive force of the electrons.

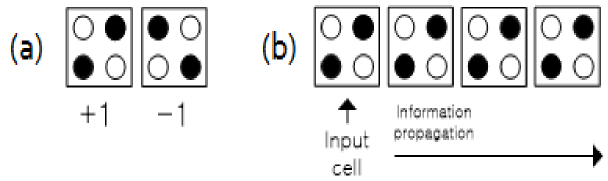

Figure 1. QCA basic concept: QCA basic concept: (a) QCA cell, (b) QCA cell based wire

b. Existing QCA T Flip-Flop

Fig.2 shows the QCA T flip-flop proposed by Bhavani et al [6]. The output value Q is transmitted in both directions to calculate the next input. A total of three majority gate are used, and the circuit design is relatively simple. However, there is no clock pulse as an input so output is not changed by the timing of clock pulse changing. And alsothere is an unnecessary area in the circuit, and a method for efficiently using thespaceof the circuit is needed. In this reason, the circuit is not practical to manufacture.

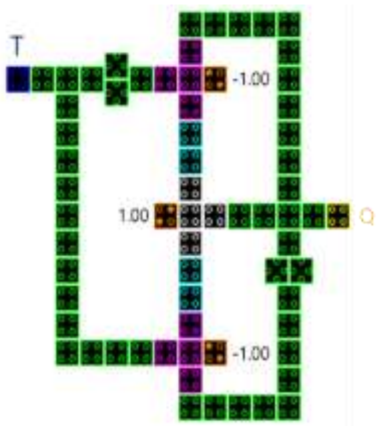

Figure 2. Circuit layout of QCA T flip-flop by Bhavani et al.

3. Proposed QCA Falling-Edge Triggered T Flip Flop

Fig. 3 shows a diagram of the proposed T flip-flop. The T flip-flop uses the principle of the XOR gate, and the state of the output changesaccording to the time when the clock changes by connecting the clock pulse generator. Fig. 4 shows the circuit and simulation results of the proposed falling-edge triggered T flip-flop. We have previously proposed a basic type of T flip-flop [7], and now we proposed a more practical T flip-flop by connecting a clock pulse generator to this circuit. The simulation results show that the state of the output Q is toggled when the clock CP falls.

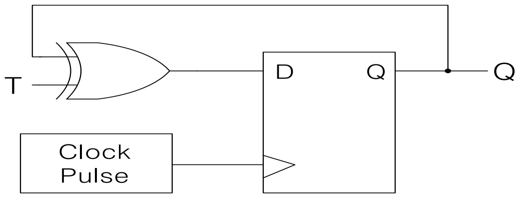

Figure 3:. Block diagram of proposed T Flip Flop

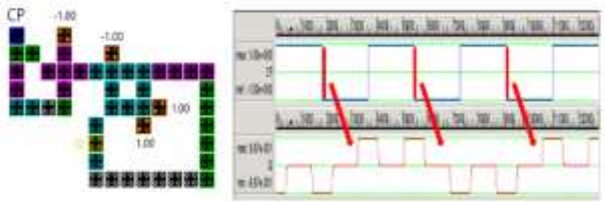

Figure 4:. Proposed QCA falling-edge triggered T Flip-Flop

4. Comparison

Table 1 compares the performance of the proposed circuit with the existing circuit [6]. Conventional circuits consume a lot of cells and area, making circuit design inefficient. The proposed circuit has a total of 47 cells and 57,084nm^2 area, which consumes a smaller area than the conventional circuit. In addition, since the operation of T flip-flop is supplemented by adding a clock pulse generator, the performance of the proposed circuit is superior.

Table 1. Performance comparison of T flip-flops

QCA Circuit	Cell counts	Circuit area (nm^2)
Circuit in [6]	67	82,844
Proposed circuit	47	57,084

4. Conclusion

In this paper, we propose a falling-edge triggered T flip-flop with clock pulse generator. The proposed T flip-flop is designed to have a small area, so it is effective when connecting to other circuits. We will study the counter as a future study, and we will propose a counter with excellent performance using the T flip-flop proposed in this paper.

Acknowledgment

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIP) (NO. NRF-2017R1D1A3B03034346).

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