International Journal of Engineering &Technology, 7 (3.12) (2018) 836 -840

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design of All Digital Phase Locked Loop for Wireless Applications

Swetha R[1], J. Manjula[2], A. Ruhan bevi[3]

[1,2,3]Department of ECE, SRM Institute of Technology,
Kattankulathur, Tamilnadu 603203
**Corresponding Author Email: [1]swetha_ra@srmuniv.edu.in, [2]manjula.j@ktr.srmuniv.ac.in,*
[3]ruhan.b@ktr.srmuniv.ac.in

Abstract

This paper presents a design of All Digital Phase Locked Loop (ADPLL) for wireless applications. It is designed using master and slave Dflipflop for linear phase detector, counter based loop filter and ring oscillator based Digital controlled oscillator(DCO). The programmable divider is used in the feed-back loop which is used has a frequency synthesizer for wireless applications. It is implemented in 180nm CMOS technology in Cadence EDA tool. The proposed ADPLL has locking period of 50ps and the operating frequency range of 4.7GHz and power consumption of 26mW.

Index Terms: *All Digital Phase Locked Loop(ADPLL), Dig-ital Loop Filter, Ring Oscillator, Delay Cells, Programmable divider,Cadence.*

1. Introduction

There are various frequency synthesizers in which one among them is the phase locked loop (PLL) where it plays a vital role in the wireless communications. The PLL has been implemented on single chip which has become more economical and has been produced in large scale in order to full fill the requirement of industry. These integrated chips have been digitally integrated and it has been used as the mixed signals to minimize the power consumption of the system such that they operate with low supply voltages. ADPLL which operates all digitally. This provides the betterment over con-ventional analog PLL. They overcome the issues of accuracy, skew tolerance due to the occurrence in the traditional VCO, jitter and propagation delay. There is a fast locking system in the ADPLL due to the constant operating voltage. Basically it uses the feedback loop in order to detect the lock in time and scalability is achieved. In this proposed gating techniques have been used in order to optimize the power efficiency of the system. The DCO plays a vital role in providing tuning range in place of conventional charge pump. ADPLL which consists of three parts: digital phase detector, digital loop filter and digitally controlled oscillator. DCO uses the gated ring oscillator and the delay cells in order to compare the frequency range and the power consumption. This digital Pll operates in the frequency range of 1.6KHz to 4.7GHz The fractional divider has been placed in the feedback path to synthesize the frequency for the application of wireless communication. All digital phase locked loop is used for generation of fast lock in time which uses the technique called clock gating in order to reduce the power consumption of the system where the leakage power get reduced. Here it consumes more dynamic power due to the delaying time of the counter [1]. The local oscillator which is used in DCO occupies more space where they produce a very good shape of sine wave and have frequency stability. The frequency is not changed whenever DC supply voltage is changed where it occupies more space and the complexity get increases [2]. The digital controlled oscillator with power amplifier uses the transformer of six port where the area of the chip is reduced. Time to digital converter basically consumes more time the optimization of power is not managed properly [3]. By using the less dither in digital controlled oscillator (LC oscillator) is coupled inductively to the varactor diode that maintains the tuning range of the system. The gated oscillator which uses five stage inverter rather than counters that reduces the leakage power of the system. The capacitor based oscillator which produces better resolution and occupies very less area but consumption of power is too high by using ladder based switched capacitor
[4]. Injection based oscillator which is used in the generation of clock avoids the accumulation of jitter due to rising edge of the clock. It improves the performance characteristic of jitter. Though it reduces the jitter characteristic the robustness of spur is increased and the overall efficiency of power is not optimized.Thus the scalability is reduced by the injection of clock in the oscillator. The increment and decrement counter which provides better hold and lock in range where the implementation in software is not highly possible [5]. The delay based digital controlled oscillator consumes less power but the period of locking is comparatively high than the ring oscillator [6].The Architecture consists of all digital parts such as digital phase detector, digital loop filter and digitally controlled oscillator. It is feedback loop where the reference signal is given as input to the phase detector and the vout is taken as output from the DCO and it is feedback to the phase detector until the phase is locked. The following sections are described as follows. Section II describes the proposed block diagram of ADPLL. Section III will be the simulation results of ADPLL. Final Section IV will be the conclusion of power and frequency analysis.

2. Proposed Architecture

The block diagram of frequency synthesizer shown in fig[1] has four components linear digital phase detector, digital loop filter, digital controlled oscillator and programmable divider. These blocks are implemented in transistor level using Cadence EDA tool in 180nm technology. Here the digitally controlled oscillator has compared between ring oscillator and the delay cell, where the delay cell has less operating frequency range and the locking period. So ring oscillator is preferred. The feedback loop consists of programmable divider where the output of the divider has been fed back as the input of the phase detector and it has been compared and the output has taken.

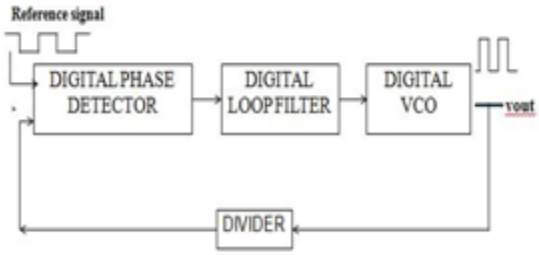

Fig. 1: Block diagram of Proposed ADPLL

A. Digital Phase detector

(DPD) The linear phase detector shown in Fig[2] composed of master and slave Dflipflop which operates with the wide operating frequency. The input signal is of 1.2GHz and the clock frequency is given as input where it produces the error voltage depending on the lead and lag frequency of input signals. The clock frequency given is the negative edge triggered. Here the up signal is produced which is given as input to the digital loop filter. [7].

Errorvoltage = $_2$(s) $_1$(s)
= 200ns 155ns
= 45ns

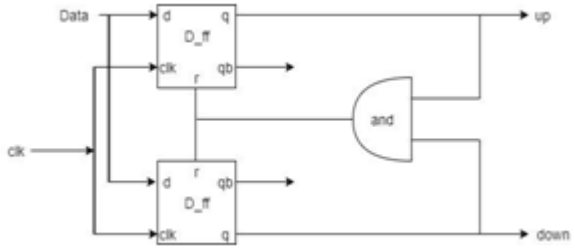

Fig. 2: Block diagram of Linear Phase Detector

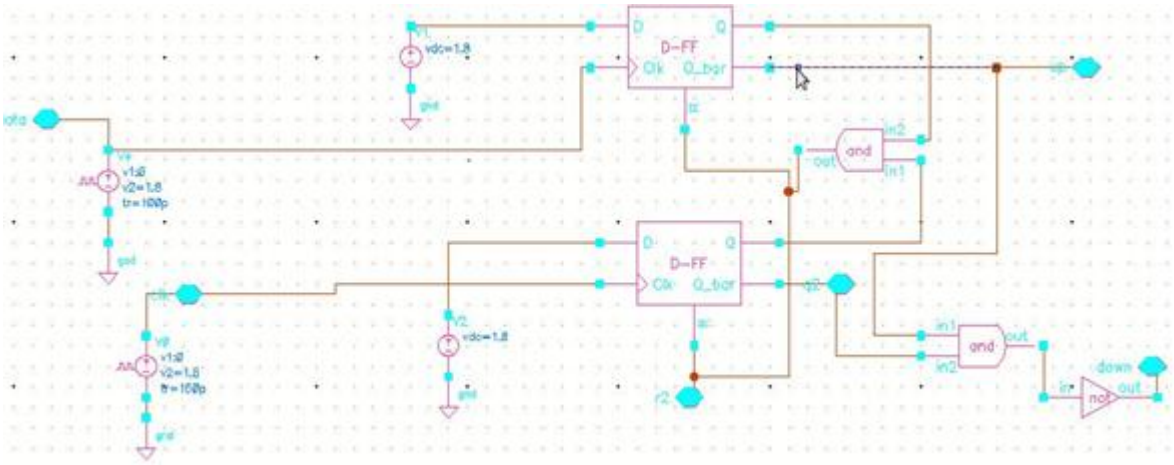

Fig. 3: Schematic view of Linear Phase Detector

B. Digital Loop Filter

(DLF) The basic charge pump has been replaced with the digital loop filter. DLF consist of counter using Dflipflop as shown in Fig[4]. It is composed of 3 bit synchronous counter where the clock frequency of 1.2GHz is given as input to the flipflops. The function of the digital loop filter is that the phase error produced by the phase detector reaches a constant value, so that it makes the transition from unlocking state to locking state.The synchronous counter is used where the clock signals have been fed in order to reduce the delay. This has been gated in order to reduce the leakage current in order to maintain the power efficiency. The input frequency has been given for each and every transition and there is a bit change for each and every transition of frequency.Suppose the bit 2, bit 0, bit 1 are in high state then the bit 3 gets toggled and the transition continues. This produces a stepwise increment and the phase detector and the counter produces a stable DC voltage which has been fed as the input to the DCO [1].

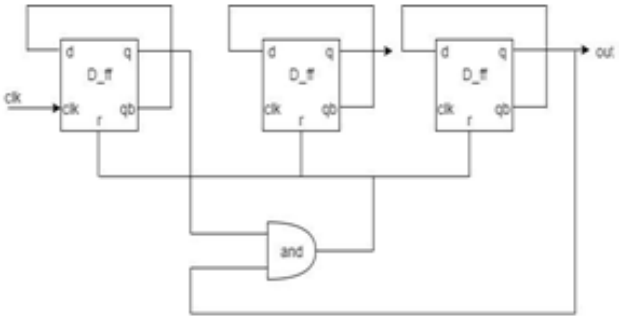

Fig. 4: Block Diagram of Digital Loop Filter

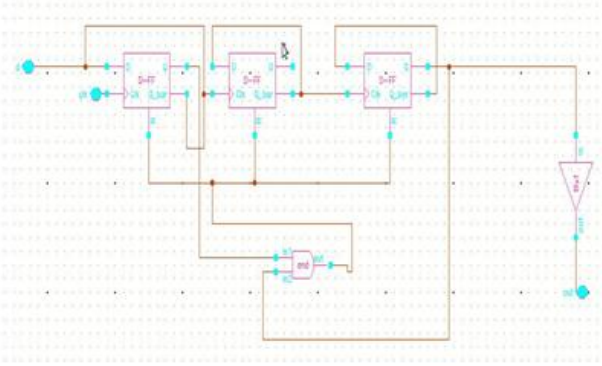

Fig. 5: Schematic view of Digital Loop Filter

C. Digital Controlled Oscillator

(DCO) The DCO is implemented by comparing the ring oscillator and the delay cell. The input to the ring oscillator is from the loop filter. Basically ring oscillator is implemented using stage ratios by changing the width and length as shown in Fig [6] [7] where the ring oscillator has performed by comparing 3 stage and 5 stage ring oscillator between fre-quency and power as in the table[1]. The 3 stage ring oscillator parametric constraints shows better results than the 5 stage ring oscillator.

Table 1. Comparison Between Ring Oscillator And Delay Cell

Parameters	Ring Oscillator	Delay Cell
Locking Period	50ps	50ns
Frequency	4.7GHz	0.5GHz
Power	26.6mW	2.2mW

D. Programmable Divider

Programmable divider used 2/3 cell divider which is in series connection. The prescalar logic and control logic are the parts of the divider. It consists of D Flip flop and the control signal P is given as input to the depending on the modin. Whenever the P=’0’ it divides the input frequency by 2 and when the P=’1’ it divides the input frequency by 3. Depending on the control signals it programmes the circuit and the output modout is taken. This uses less power by the fast division and thus it provides the wide range of logic functions [8].

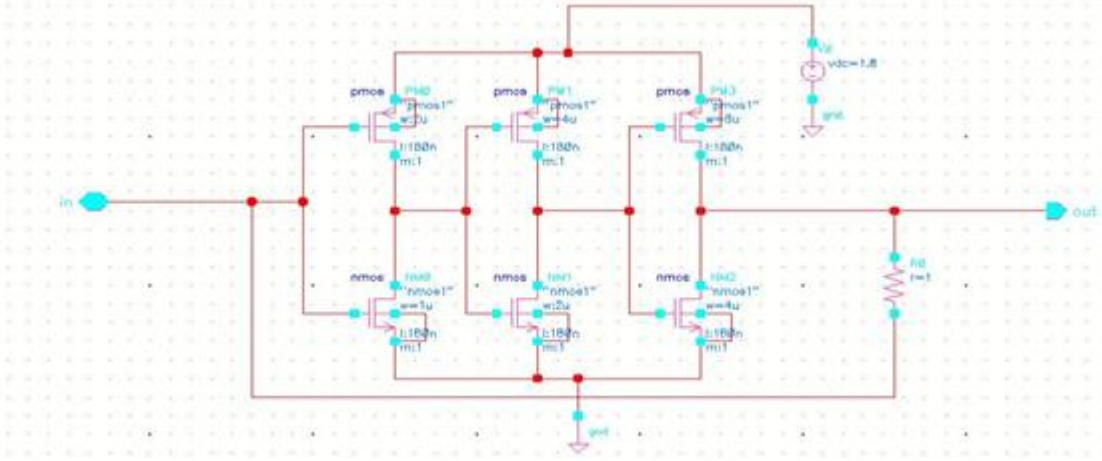

Fig. 6: Schematic view of Ring Oscillator

Table 2 : Comparison Table of Ring Oscillator

Parameters	3 Stage Ring Oscilltor	5 Stage Ring Oscillator
Frequency	4.5GHz	4.98GHz
Power	7.71mW	12.95mW

Delay cells consists of NMOS in series and parallel architec-ture where the initial conditions have been set. Comparatively delay cell consumes less power than the ring oscillator. Basi-cally ring oscillator consists of chain of NOT gates which is placed in the sequel of odd numbers where the width has 1u to 8u stage ratios. The variation in the amplitude leads to jitter analysis. Delay cells have been finely suited for the frequency synthesizer because of the low noise and the delay has been comparatively reduced than the classic ring oscillator. The power consumed is also less of about 2.2mV. The inputs to the delay cell has been given accordingly to the input frequency and the less power consumption [6].

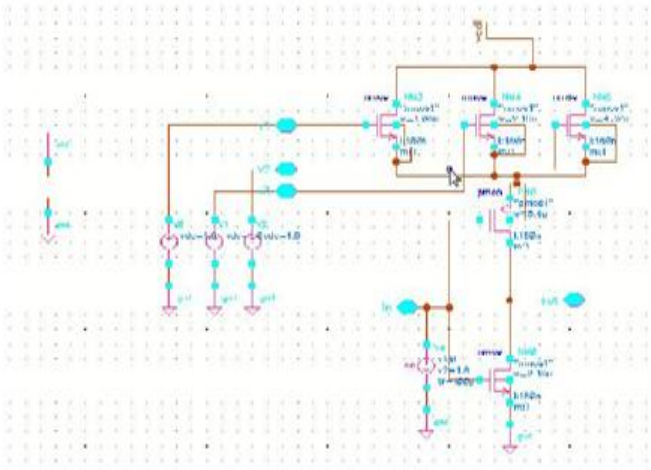

Fig. 7: Schematic view of Delay cell

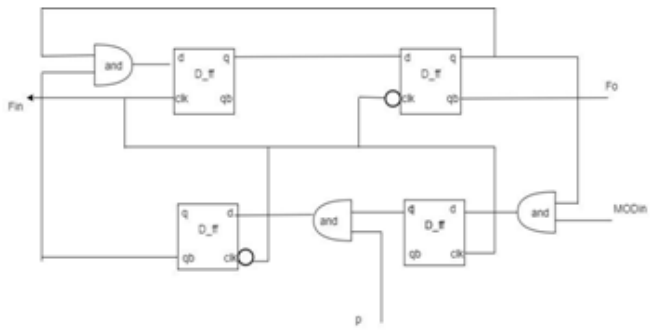

Fig. 8: Block diagram of programmable driver

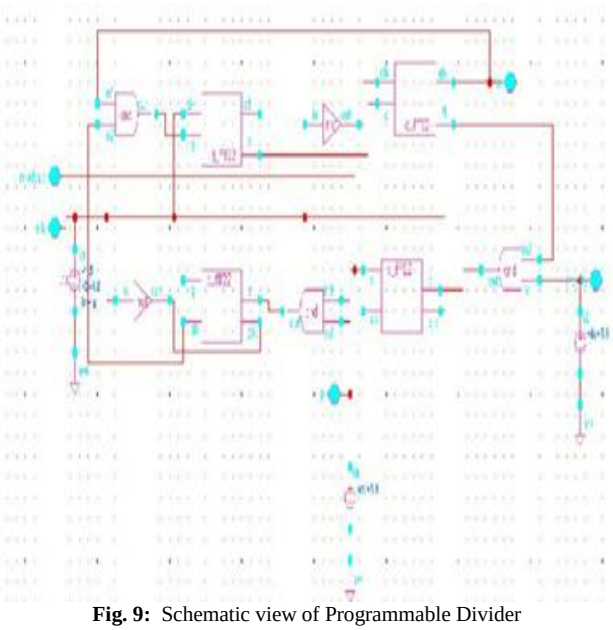

Fig. 9: Schematic view of Programmable Divider

3. Simulation Results

The proposed design is implemented in 180nm CMOS technology using Cadence EDA tool.

A. Digital Phase Detector

Simulation result of phase detector shown in Fig[10] has produced a error voltage of 45ns obtained mathematically by

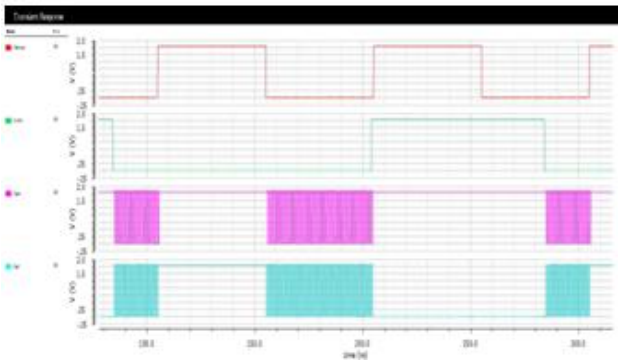

Fig. 10: Simulation Result of Phase Detector

the formula [9] and amplitude of 1.8v for the input frequency of 1.2GHz.

B. Digital Loop Filter

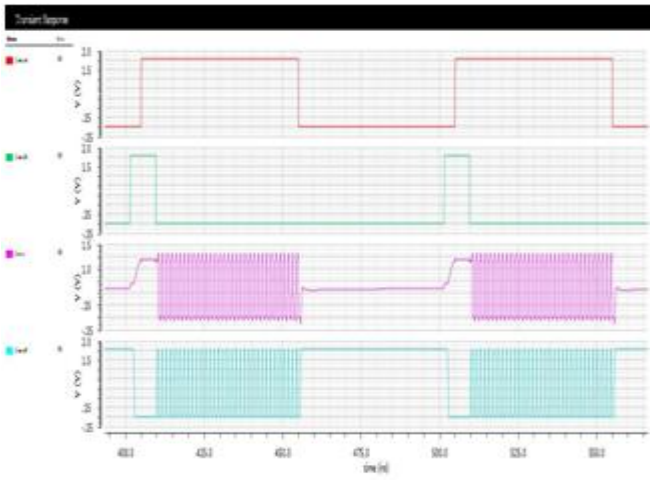

Fig. 11: Simulation Result of digital loop filter

Digital Loop Filter infers three stage synchronous counter as in the Fig[11] where the output of digital loop filter produces a constant value where the up signal is produces due to the input frequency of 1.2GHz and the clock frequency of 0.8GHz.

C. Digital Controlled Oscillator

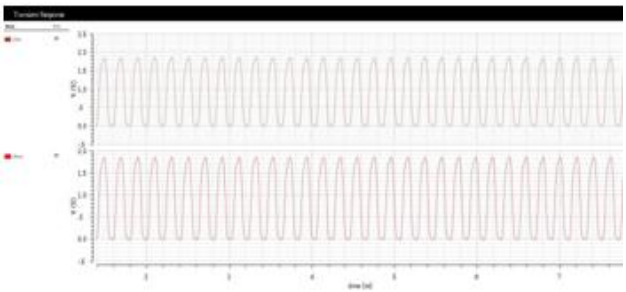

Fig. 12: Simulation Result of DCO using Ring Oscillator

Simulation result of digital controlled oscillator as shown in the Fig[12] produces oscillation frequency of 4.7GHz by the triggering pulse and thus it has the delay of 50ps.

D. Programmable Divider

Programmable divider as shown in the Fig[13] depicts the input frequency of mod 3 when it gets divided by P='1' and the input frequency of mod 2 by P='0' which is programmed as N/N+1.

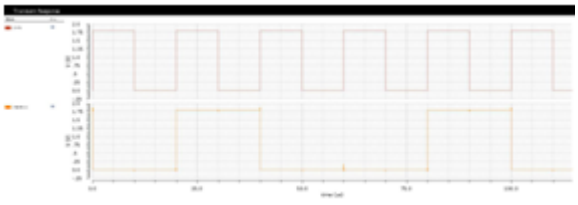

Fig. 13: Simulation Result of Programmable Divider

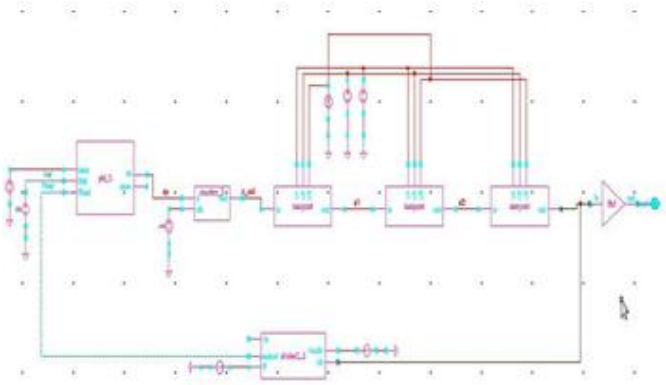

Fig. 14: Schematic view of All Digital Phase Locked Loop

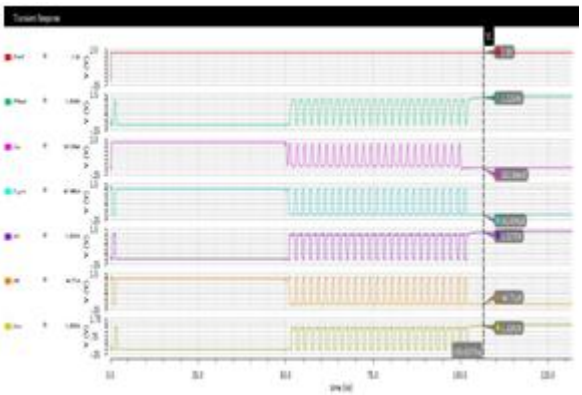

Fig. 15: Simulation Result of ADPLL without Divider

E. All Digital Phase Locked Loop

This infers the All digital phase locked loop in the Fig[14]where it operates at the frequency range of 4.7GHz and the power consumption of 26mw by using the ring oscillator based DCO.

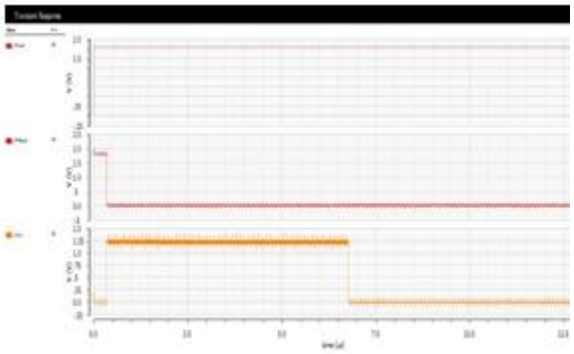

Fig. 16. Simulation Result of ADPLL with Divider

This depicts All digital phase locked loop in the Fig[15] with the programmable divider where the input frequency is divided by mod3 and the output of DCO will be the frequency of 2fin.

4. Conclusion

The Frequency and the power has been compared between the ring oscillator and the delay cells where the delay cell consumes less power than the stage ratio ring oscillator. But by using the ring oscillator the locking period is 50ps and frequency of about 4.7GHz. Thus ring oscillator is more efficient to be used in the DCO and it has been used as the frequency synthesizer.

Table 3: Comparison of My Work With the Reference Paper

Parameters	Reference [1]	This Work
Frequency	0.8GHz	4.7GHz
Lock in Time	3.3us	50ps
Power Consumption	2.3mW	26mW

References

[1] Nitesh Tripathi, Design of Power Efficient All Digital Phase Locked Loop, IEEE Wispnet 2016.

[2] C. Li and A. Liscidini, Class-C PA-VCO cell for FSK and GFSK transmitters, IEEE J. Solid-State Circuits, vol. 51, no. 7, pp. 15371546,Jul. 2016.

[3] A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6 (14.5) System Efciency at 6-dBm (0-dBm) Pout, IEEE 2017.

[4] Zhiqiang Huang and Howard C. Luong, Fellow, Design and Analysis of Millimeter-Wave Digitally Controlled Oscillators With C-2C Exponen-tially Scaling Switched-Capacitor Ladder , IEEE 2017.

[5] Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS Cheng-Ru Ho, Mike Shuo-Wei Chen

[6] Shweta Dabas, A New Design of Digitally Controlled Oscillator for Low Power Applications

[7] Design of High Frequency D Flip Flop Circuit for Phase Detector Application Suraj Kumar Saw1, Preetisudha Meher2 Swarnendu Kumar Chakraborty3

[8] A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35- m CMOS Technology.

[9] T. H. Lee, Chap. 15. Gray and Meyer, 10.4 Clock generation: B. Razavi, Design of Analog CMOS Integrated Circuits, Chap. 15, McGraw-Hill, 2001.