International Journal of Engineering & Technology, 7 (2.20) (2018) 119-123

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design of High Performance Decoder with Mixed Logic Styles

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Abstract

The CMOS technology is the mostly portable technology used in the designing of the circuits and in its fabrication. Designing of the circuits using CMOS technology requires the high power, high transistors count and low performance. The basic idea of the project is in order to reduce the count of transistors, time delay, and power consumption and to increase the performance of the circuits such as line decoders. The line decoder is a combinational circuits to which „n" no .of inputs are given as input and the output is 2^n based on the selected input and it requires 20 and more than 20 transistors to design any MxN decoders using CMOS technology .In order to configure the parameters and to make it more portable we are using different types of logic styles this usage of technologies more than one technologies on each circuit is a mixed logic styles .In this concept we observe the results as per required .The technologies we use in this is TGL/DVL. The suggested framework "Design about low Power, helter execution 2-4 What's more 4-16 blended rationale offering Decoders" is executed done 45nm engineering utilizing cadence virtuoso tool. The circuit schematic is designed and the circuits are simulated for functionality verification.

Keywords*: Logic gates, Line Decoder, Cadence*

1. Introduction

The basic Static CMOS circuits would be utilized for extent of logic gates in integrated circuits. They comprise of reciprocal NMOS pull down and PMOS pull up dependent upon networks and exhibit perfect execution and in addition resistance to noise and variation. Therefore, CMOS rationale will a chance to be depicted inevitably by examining generosity against voltage scaling furthermore transistor measuring Furthermore subsequently trustworthy operation for low voltages Furthermore little transistor sizes [2]. Information signs have on a chance to be connected with transistor entryways only, publicizing reduced configuration unpredictability and support about cell-based rationale more outline.. In this chapter, implementation of Decoders using different logic styles has been studied. The understanding of this design has been explained in detail. The characteristics of the high speed design circuit being explained.

An decoder might make an combinational out that transforms double information n information lines to a best of 2n exceptional yield lines or fewer, if the n-bit coded information requirement unused combinations. The individuals circuits inspected in this worth of effort are known as n-to-m line decoders. and their main aim is to produce the m = 2n minimum n input variables.

A 2-4 accordance decoder generates the individuals 4 minimum terms D0-3 something like 2 enter variables a more b. Its rationale operation may be summa-rized for table i. Depending upon the individuals information mix Also you quit offering on that one amongst those 4 outputs will be decided Furthermore situated should 1 at the same period the individuals others might set on 0. An inverting 2-4 decoder generates those equal build terms I0-3, con-sequently the individuals picked will be situated with 0 and the r might be set for 1, similarly as shown clinched alongside table 2.

Table .1. Truth table of 2:4 decoders

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

Likewise contradicted with 6, So In this way we implement logic functions with high efficiency. A 2-4 decoder can be executed with 20 transistors utilizing 2 inverters and 4 NOR gates, Concerning the demonstrated fig. 3. 1(a). Those relating inverting decoder could be made executed for 20 transistors utilizing 2 inverters and 4 NAND gates, Likewise demonstrated in fig. 1.

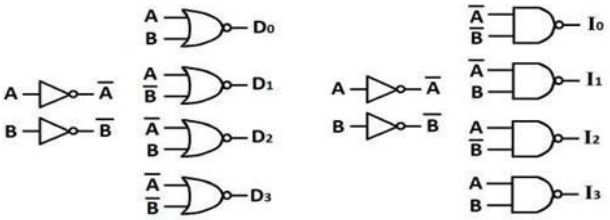

Figure.1. 20-transistor 2:4 line decoders implemented with CMOS logic

1.2 Line Decoder with 2:4 Predecoedrs

An 4-16 transport decoder generates the individuals 16 least terms I0-15 over 4 enter variables A, B, c's Also D, Also an inverting 4-16 line decoder generates those essential analytics least terms I0-15. A regulate execution to these circuits could require 16 4-input or and NAND gates. However, An more productive implementation can be got utilized by an pre decoding technique, as stated by which blocks of n address bits can have a chance to be pre decode under 1-of-2n pre decoded lines that serve Similarly as inputs of the last stage of decoder [1]. For this technique, a 4-16 decoder might a chance to be actualized with two 2-4 inverting decoders and sixteen 2-input NOR gates fig. 3. 2(a) Furthermore an inverting one might have a chance to be actualized for 2 2-4 decoders and also 16 2-input NAND gates fig. 3. 2(b). In CMOS logic, these implementation requires 8 inverters and also 24 4-input gates, yielding a total 104 transistors every.

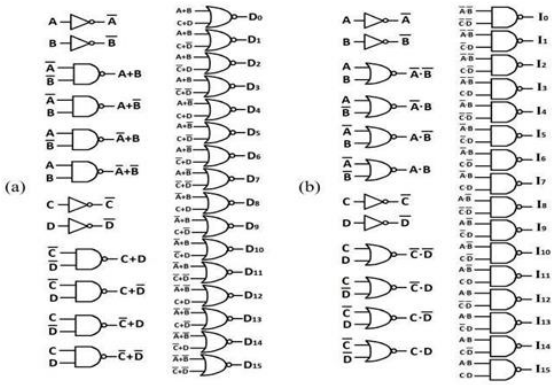

Figure.2. 104-transistor 4-16 line decoders implemented with CMOS logic and predecoding:

2. New Mixed Logic Designs

To computational logic, transmission entryways bring basically been utilized within XOR-based circuits for example, full adders What's more as those essential switch component for multiplexers. However we think as of their utilization in the utilization starting with asserting alternately logic, Also Concerning illustration demonstrated carried out [5], which could a chance to be proficiently associated in line decoders. Those 2-input TGL or entryways are shown in Fig. 2 (a) and 2 (b).

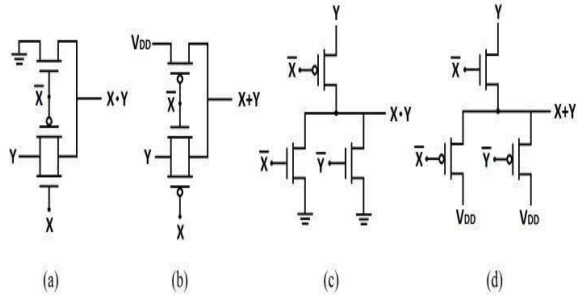

Figure.3. The 3-transistor AND/OR gates considered in this work

Decoders need high fan-out circuits that various inverters can be utilized Eventually by different gates, hence utilizing those TGL/DVL gates resulting transistor count reduction.

A critical basic character of that gates will have deviated nature, i. E. Those way that they don't need balanced entry loads. Similarly as demonstrated for fig. 3, We mark the individuals 2 entryway inputs X Also Y. Clinched alongside TGL gates, passage X controls the entryway terminals of 3 transistors Also toward those same chance entrance Y propagates of the yield hub through the individuals transmission entryway. To DVL gates, passage X controls 2 transistor entryway terminals and at those same occasion when passage Y controls 1 entryway terminal Moreover propagates through An pasquinade transistor of the yield. We will allude X Moreover Y inputs Concerning representation the individuals control pointer and the propagate indicator of the gate, separately.

2.1 The 14 Transistor 2:4 Low-Power Topology

Plotting a 2-4 line decoder to potentially TGL or DVL entryways could oblige downright dependent upon 16 transistors (12 to or entryways and Additionally 4 for inverters). However, inevitably blending both furthermore somewhere else someplace else sorts under those same toponym need aid used for right indicator arrangement, it might be Might make permitted to dispense with particular case amongst the individuals two inverters, thusly diminishing those downright transistor number should 14. Let us expect that, out of the two inputs, to be specified A and B, we remove those B inverter from the circuit. Those do least haul (A‟B‟) is executed with An DVL gate, the place a is utilized Similarly as propagate sign. The D1 base haul (AB‟) may be actualized for An TGL gate, the place b will be utilized Concerning illustration propagate indicator. The D2 base term (A‟B) is executed with a DVL gate, the place An will be utilized Similarly as propagate indicator. Finally, those D3 least term (AB) will be executed for a TGL gate, the place b may be utilized Likewise propagate sign. These specific decisions totally deflect the utilization of the integral b signal, In those b inverter could a chance to be wiped out starting with those circlet bringing about An 14- transistor toponomy (9 NMOS, 5PMOS).

Accompanying a comparative technique with alternately gates, An 2:4 inverting line decoder camwood be actualized with 14 transistors (5 NMOS, 9 PMOS), as well: I0, I2 would executed for TGL (using b as propagate signal) Also I1, I3 are actualized with DVL (using An Likewise propagate signal). Those b inverter camwood at the end of the day a chance to be elided.

Those inverter disposal diminishes transistor count, legitimate exertion and generally exchanging movement of the circuits, thereby minimizing control dispersal. Similarly as distant Similarly as those creators need aid concerned, 14 will be the least amount of transistors re-quired with figure it out a) rationale full-swinging 2-4 offering decoder for static (non-clocked)

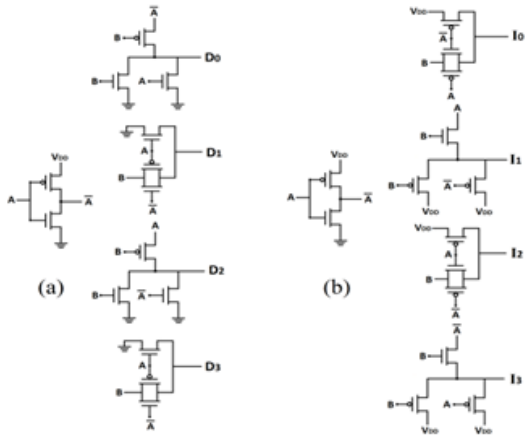

Figure.3 (a) and (b) 14 Transistor 2:4 Low-Power Topology

2.2 The 15-Transistor 2:4 High-Performance topology

Those low-power topologies exhibited over have An detriment in regards to Most exceedingly bad instance delay, which goes from the utilization from claiming reciprocal An Likewise those propagate indicator on account about D0 What's more I3. However, Understanding D0 Furthermore I3 can be actualized a

greater amount effectively Toward utilizing standard CMOS gates, since there is no need for integral signs. Specifically, D0 could make executed with a CMOS or entryway What's more I3 with An CMOS NAND gate, including particular case transistor to every toponomy. Those new outlines coming about because of this change blend 3 distinctive sorts of rationale under those same out Furthermore introduce a critical change in delay same time just marginally expanding force dispersal.

2.3 Integration in 4:16 Line decoders

An little scale, circuits In view of pass transistor rationale might understand rationale capacities for fewer transistors and enhanced execution contrasted with static CMOS. However, cascading a few non-restoring circuits makes a fast corruption to execution. A mixed-topology approach may be exchanging restoring Also non-restoring levels about logic characteristics of both Adopting this configuration methodology, Also with admiration to the hypothesis exhibited on segment II, we actualized four 4-16 decoders Eventually Tom's perusing utilizing those four new 2-4 Similarly as pre decoders over conjunction with CMOS NOR/NAND entryways to prepare the decoded outputs. The new topologies determined starting with this mix are: 4- 16LP .

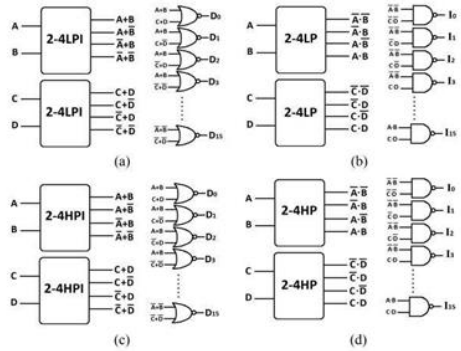

Figure.4. New 4-16 line decoders

3. Implementation

In this chapter, basic gates and decoders has been designed in Cadence Virtuoso tool and their characteristics are studied. The inverter is one of the basic gates in electronics. It consists of a PMOS and NMOS connected as shown in Fig. 4. It produces the output which is exact inverse of input.

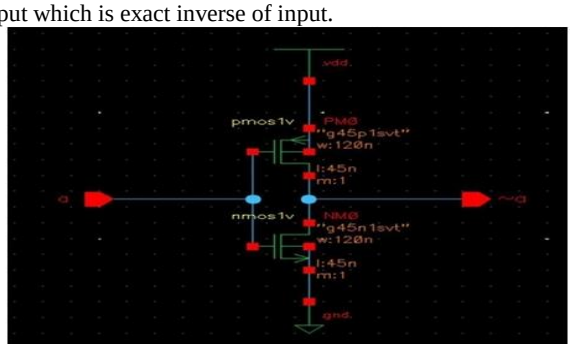

Figure.5. Inverter architecture in Cadence.

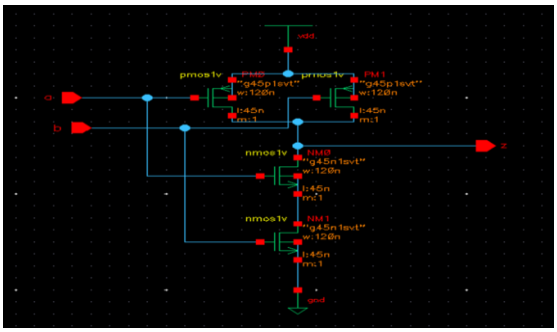

Figure.6.1 NAND gate architecture in Cadence.

3.2 NOR Gate

A HIGH output(1) comes about if both the inputs of the gate would be low (0); If any one input is HIGH (1) it produces a low result (0) as outcomes. nor is those outcome of the negation of the OR operator. Those NOR gate comprises about 4 MOSFETs i. E. , 2 PMOS, 2 NMOS.

3.1 NAND Gate

According to the truth table logic NAND gate is the basic gate for implementing logical conjunctional HIGH output (1) results only if one of the inputs to be LOW (0). The NAND gate cell consists of 4 MOSFETS i.e., 2 PMOS, 2 NMOS in total.

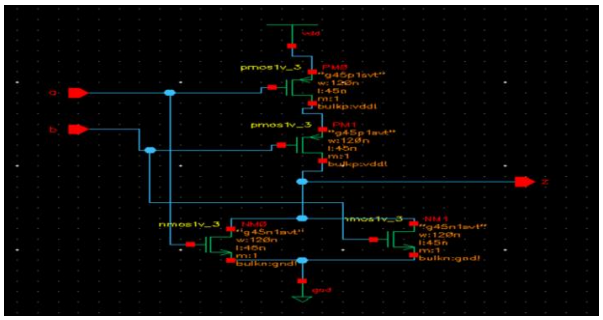

Figure.6.2 NOR gate architecture in Cadence.

3.3 2:4 Decoder

In electronics, Decoder is a combinational circuit. It consists of 4 NAND gates and 2 Inverters consists of totally 20 MOSFETS in CMOS logic.

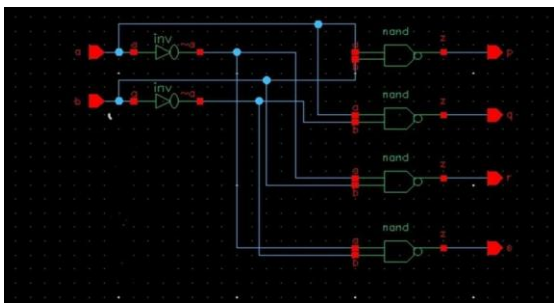

Figure.6.3 2:4 Decoder architecture in Cadence.

By Using Mixed Logic styles

14 Transistor 2:4 Low-Power topology

In CMOS Technology , implementation of 2-4 Decoder requires 20 MOSFETS. Yet all the for mixed logic style, i. E. , Toward mixing both AND gate types it is easy to eliminate one or more

inverters by arranging proper signals in same topology for the reduction of total transister count to 14

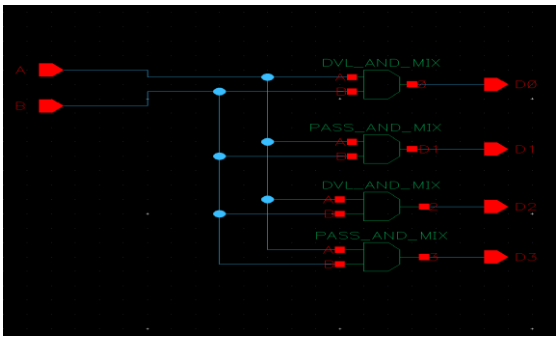

Figure.6 4. Low power 2-4 Decoder

In CMOS Technology, implementation of 2-4 Decoders requires 20 MOSFETS. But in MIXED logic style.

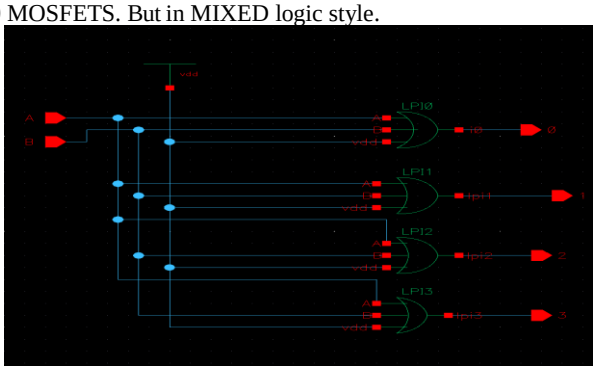

Figure .6.5 Low power Inverter 2-4 Decoder

4. Simulation Results

To design decoders we are using cadence tool with GPDK 45nm technology sustain 1.1V, time period of 40ns, rise time 5ps, fall time 5ps, pulse width20ns

2:4 Decoders

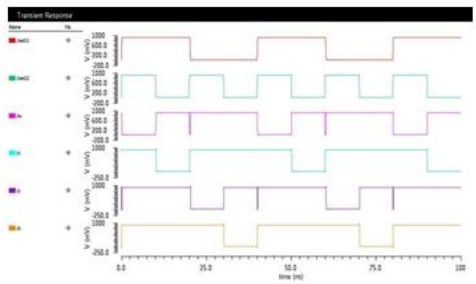

Figure .7. Simulated results of 2:4 Decoder.

When both of the inputs are Active high, the output is Active low (w).

When both of the inputs are Active low, the output is Active low (z).

4.1 Low Power 2:4 Decoder

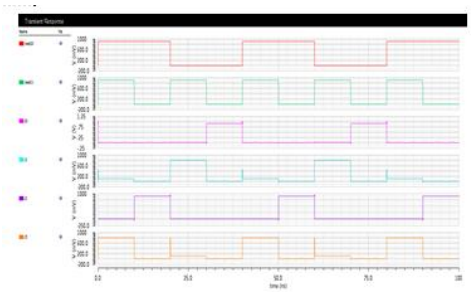

Figure.7.1 Simulated results of Low Power 2:4 Decoder.

When both of the inputs are Active low, the output is Active high (0).

When first input is Active low and second input is Active high, the output is Active high (1).

When first input is Active high and second input is Active low, the output is Active high (2).

When both of the inputs are Active high, the output is Active high (3).

4.2 High Power 2:4 decoder

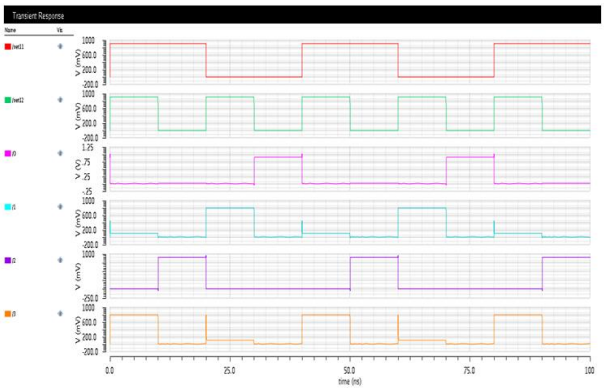

Figure 5.4. Simulated results High Performance 2:4 Decoder.

When both of the inputs are Active high, the output is Active high (3).

When first input is Active high and second input is Active low, the output is Active high (2).

When first input is Active low and second input is Active high, the output is Active low (1).

When both of the inputs are Active low, the output is Active low (0).

4.3 High Performance 4:16 Decoder

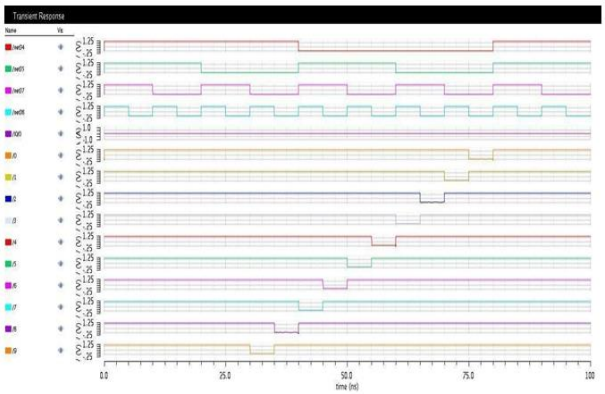

Figure.7.2. Simulated results of High Performance 4:16 Decoder.

The outputs of the HP 4:16 decoder is based upon their respected inputs.

4.4 High Performance Inverting 4:16decoder

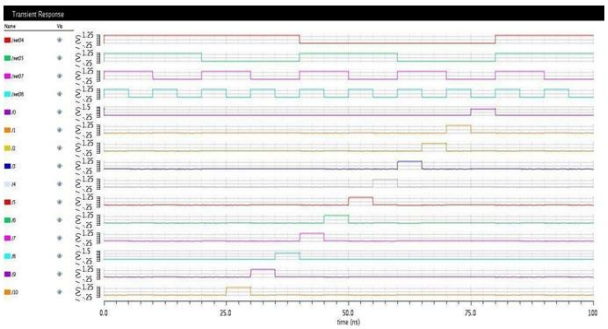

Figure .7.3 Simulated results of High Performance Active Low 4:16 Decoder.

The outputs of the HPI 4:16 decoder is based upon their respected inputs

4.5 Analysis of Decoder

Table.3. Power calculations of various circuits at different frequencies

Power	1.1V		
Frequency	500MHz	1GHz	2GHz
2_4LP	11.55×10^{-6}	12.36×10^{-6}	13.99×10^{-6}
2_4LPI	47.48×10^{-6}	48.55×10^{-6}	50.68×10^{-6}
2_4HP	11.45×10^{-6}	13.58×10^{-6}	66.8×10^{-6}
2_4HPI	62.2×10^{-6}	63.73×10^{-6}	66.8×10^{-6}
4_16LP	96.29×10^{-6}	99.68×10^{-6}	106.4×10^{-6}
4_16LPI	86.47×10^{-6}	90.5×10^{-6}	98.55×10^{-6}
4_16HP	125.6×10^{-6}	129.8×10^{-6}	121.4×10^{-6}
4_16HPI	86.11×10^{-6}	89.75×10^{-6}	97.03×10^{-6}

Table.4. Delay calculations of various decoder circuits at different frequencies.

Delay(ns)	1.1V		
Frequency	500MHz	1GHz	2GHz
2_4LP	0.024259	0.024259	2.424718
2_4LPI	0.0108107	0.010916	5.65
2_4HP	0.024262	0.242431	14.8737
4_16HPI	0.014874	0.0126583	1.548247
4_16LP	0.05045	0.292874	2.92824
4_16LPI	0.050912	0.0103818	1.03871
4_16HP	0.04695	0.046921	0.01181
4_16HPI	0.046743	0.0109096	0.109248

5. Conclusion

The proposed system "Design of Low Power, HP 2:4 and 4:16 Mixed- Logic Line Decoders" is implemented in 45nm technology using cadence virtuoso tool. The schematic is designed and the circuits are simulated for functionality verification.

The delay and average power of the proposed Decoder is calculated using Cadence tool. Decoder circuit designed with mixed logic style performs well at 45nm technology and we can also hoping that, this circuit will work at technology nodes below 45nm also.

6. Future Scope

Decoders are used widely in microprocessor for memory storage applications to achieve the high performance and low power demand. One such widely useful is the mixed logic style decoder. In future, still there are chances are there to design a decoder circuit using other logic styles.

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