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Research paper

Modelling and analysis of a NTVV-SVM based three-level twin-step matrix converter

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Abstract

Recently the tremendous advancement has been seen in the field of matrix converter topology. For high power drive applications, industries often need high power AC-AC converters like three level matrix converter because it is having the ability to generate a set of balanced sine waves for inputs as well as outputs. The three level matrix converters possess better output performance with reduced harmonic contents compared to all two-stage indirect matrix converters. In this matrix converter topology, the idea of neutral-point clamped-VSI is employed to the inversion step of the matrix converter circuitry. To control the power switches the gate signals are produced using NTVV based space vector modulation. To justify the theoretical study a complete model of a three-level twin-step matrix converter has been designed in Matlab/Simulink and its performances are analysed.

Keywords: *Three-Level Matrix Converter; IMC; DMC; Neutral Point Clamped VSI; Near Three Voltage Vector (NTVV) Based SVM*

1. Introduction

In the early days, back-to-back connected rectifier-inverter set was used to drive high power electric motors, but it could not able to drive the load at any arbitrary frequency and voltage. The entire system became heavy and bulky due to the use of the energy storing element. So there was a requirement of direct AC-AC converter specifically matrix converter which provides direct AC-AC conversion at any arbitrary frequency and voltage. The theoretical approach on matrix converter was introduced in 1976 by L. Gyugi and B. Pelly [1] and topological advancement started after the papers published by Venturini and Alesina in 1980 [2], [3]. The matrix converter possesses the following advantages over traditional back-to-back converter

- Ability to produce an output voltage at any arbitrary amplitude and frequency
- Capable of bi-directional power flow due to the use of bi-directional switches
- Generates sinusoidal output current
- Controls input displacement factor irrespective of the load
- Possess tightly packed designing due to non-usage energy storing elements

These glamorous properties of matrix converter have induced researchers to study and work with matrix converter [4], [5], and [19]. Topologically the matrix converters are classified as direct matrix converter (DMC) and indirect matrix converter (IMC). The typical circuitry of DMC and IMC are shown in Fig. 1 & 2. By applying felicitous modulation strategy, like Venturini method [6], Roy's method [7] or space vector modulation [8-10], the DMCs are able to induce high quality sine wave inputs and outputs. As per the figure 2 & 3, the IMC contains a current source AC-DC converter and a two-level VSI. This projected topology is capable to generate input-output waveforms in the same quantity as that of DMC. There are so many literature on protection of Matrix converters [18]

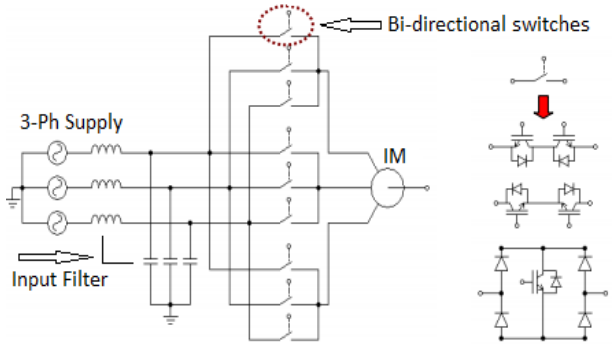


Fig. 1: Typical Circuit of DMC and Bi-Directional Switches.

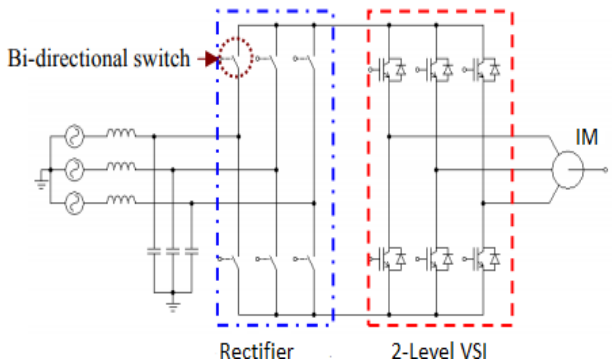


Fig. 2: Typical Circuit of IMC.

In so many applications the IMC are preferred over the DMC because of simple and safe commutation of switching devices.

After all, the MC topologies possess some drawbacks such as the use of more switching devices and voltage transfer ratio restricted to 86.6% of the input voltage.

The three level matrix converters are derived from the IMC topology. In high power AC drive applications, the three level matrix converters often found suitable because it's having the ability of generating a set of balanced sine waves for inputs as well as outputs. The three level matrix converters possess better output performance with reduced harmonic contents compared to all two stage indirect matrix converters [11-17]. In this matrix converter circuitry, the idea of neutral point clamped-VSI [12-20] is employed in the inversion step of the matrix converter circuitry. To control the power switches the gate signals are produced using space vector modulation based on NTVV technique [13]. To justify the theoretical study a complete model of a three-level twin-step matrix converter has been designed in Matlab/Simulink and its performances are analysed.

2. Topology

The typical circuitry of a three-level twin-step matrix converter is pointed out in Fig.3. From this figure it's clear that this matrix converter converts AC-AC power in two different step namely rectification and inversion step. The rectification step resides a 3X2 converter as rectifier like conventional indirect matrix converter to produce a DC- link voltage V_{Pn} for the inversion step. In the inversion step the concept of three-level neutral-point-clamped (NPC) voltage source- inverter (VSI) is applied to produce the desired three phase output voltages. The DC- link mid-point '0 ' and the neutral point of the capacitive input filter is inter-linked to split the DC-link voltage V_{pn} into two voltage supplies, namely V_{po} and V_{no}. These two voltages are then fed to the NPC-VSI to produce the desired three level phase -to - neutral output voltages. By considering DC-link mid-point 'o' as a reference the DC-link voltage V_{Pn} also can be split into three voltage levels such as V_{po}, 0V and V_{no}. Based upon these three DC-link voltages, the inversion step is modulated to produce three level output voltage wave shapes.

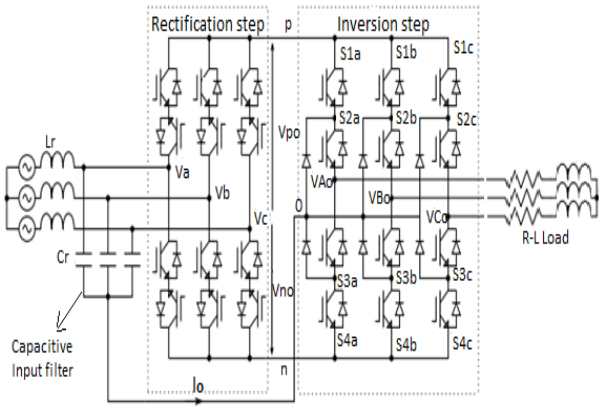


Fig. 3: Typical Circuit of 3-Level Twin-Step Matrix Converter.

At a time, only two bi-directional switches can be turned ON to conduct an input line voltage to DC-link points 'p ' & 'n '. Hence the equivalent circuit of the rectification step can be depicted by two anti-series connected switches, one connects the positive voltage level to DC-link point 'p ' and other connects the negative voltage level to the point 'n ' as elucidated in Fig.4. This figure also claims that the equivalent circuit is quite similar to the traditional NPC-VSI [15].

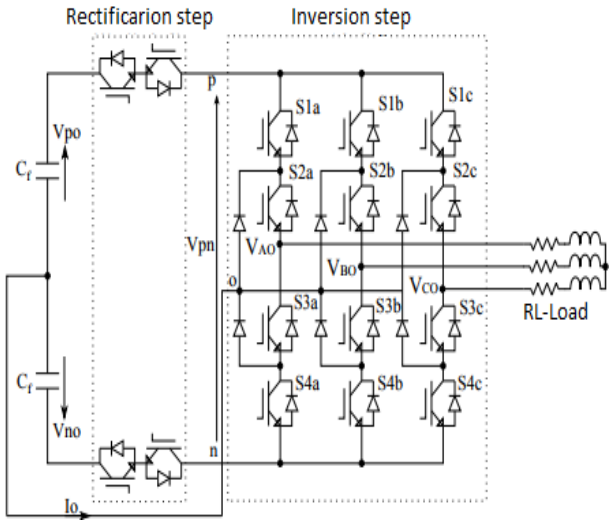


Fig. 4: The Equivalent Circuit of a Three-Level Twin-Step MC.

The switching combinations of the inversion step are shown in the table-I [15]. It is clear that every output terminal voltage $V_{ko}\{k_e(A, B, C)\}$ has three probable voltage levels i.e. $V_{po}, 0V$ and V_{no} which enable the NPC VSI converter to generate three level output voltages.

Table 1: Switching Combinations for Each Phase-Leg of the Inversion Step

S_{1x}	S_{2x}	S_{3x}	S_{4x}	V_{ko}	Switching States
ON	ON	OFF	OFF	V_{po}	P
OFF	ON	ON	OFF	0	0
OFF	OFF	ON	ON	V_{no}	N

As described above, it is clear that this converter can offer all the advantages of the traditional IMC namely controllable input displacement factor, reduce harmonics in input current, capable of regeneration and none use of energy storing elements, hence increases reliability of the converter. However, this converter listed some drawbacks: complicated circuit, number of switches used, and balancing problem of the neutral-point of the NPC-VSI. The neutral point balancing problem can cause distortion in the output voltage. This problem can be avoided by proper control of the neutral point current $\boldsymbol{i_o}$ following through the capacitive input filter.

3. NTVV- SVM modulation

There are several control strategy for controlling the matrix converter like Venturini's algorithm, Roy's Algorithm, space vector modulation and sinusoidal pulse with modulation, etc. To get optimum output for three level matrix converters, the space vector modulation is used. This SVM scheme was proposed in [8]. This control scheme is applied to the rectification and inversion step separately. In every step, a union of command vectors is conceived to incorporate a reference command vector with specified magnitude and phase. Once, the command vectors and their fellow duty ratios are obtained, the modulation pattern of this converter merges with the switching states of both steps, so that an appropriate balance can be obtained between input currents and output voltages over a sampling period. The modulation at rectification step is done based on the concept illustrated in conventional IMC [14], so a short review is presented in this section. The main disparity between the SVM schemes of this converter and that for conventional IMC is allied at inversion step.

3.1. The SVM on rectification step

As the rectification step is supposed as a self-operated current source rectifier. So the DC-link current I_{rec} will be consistent throughout the switching period Ts. Therefore, this combination

with input source can be considered as a DC current source. Hence the current continuity should be represented by the equation (1) [14]

$$S_{Pa} + S_{Pb} + S_{Pc} = \quad (1)$$

Where, if $S_{Pi} = 1$ implies phase connected to P and $S_{Pi} = 0$ implies phase connected to n or not connected.

The input-output voltage and current of the rectification step can be modelled with the help of connection function, as shown in equations (2) and (3)

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = [F_{rec}] \times \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = [F_{rec}]^T \times \begin{bmatrix} I_{rec} \\ -I_{rec} \end{bmatrix} \quad (3)$$

here, two space vectors are specified, one is I_E represent input current and other is V_E represent input voltage and these space vectors represented as below,

$$V_E = \frac{2}{3} \times \left(V_a + V_b e^{+\frac{2\pi i}{3}} + V_c e^{\frac{-2\pi i}{3}} \right) \quad (4)$$

$$I_E = \frac{2}{3} \times \left(I_a + I_b e^{\frac{+2\pi i}{3}} + I_c e^{\frac{-2\pi i}{3}} \right) \quad (5)$$

As per the relation stated above in equation (1), only nine switching combinations are validated for the operation of rectification stage rectifier, these switching combinations are depicted in table-I. The space diagram of the input current vectors of this step is depicted in the Fig.5

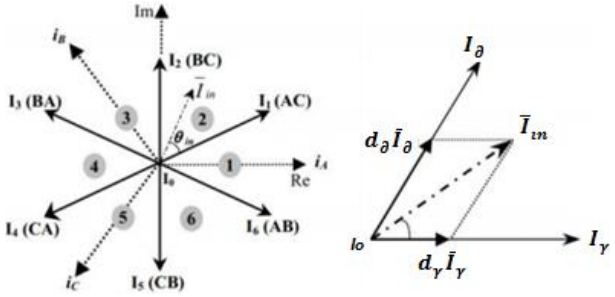


Fig. 5: The Space Diagram of Rectification Stage Current Vectors & Projection of Its Reference Vector.

As per this modulation, the reference vector is integrated using two adjoining space vectors (depicted as I_γ and I_δ) and a zero current vector I_0. The duty cycle of every vector can be defined as presented in equation (6)

$$\left.\begin{aligned} m_\gamma &= m_C . sin(\theta_i) \\ m_\delta &= m_C . sin\left(\frac{\pi}{3} - \theta_i\right) \\ m_0 &= 1 - m_\gamma - m_\delta \\ \text{Here } m_C &= \frac{I_E}{I_{rec}} \text{ and } 0 < \theta_i < \frac{\pi}{3} \end{aligned}\right\} \quad (6)$$

where, m_γ, m_δ and m_0 are representing the duty cycle for the vectors I_γ, I_δ and I_0 respectively. and m_C is the transfer ratio of input currents and for maximum power transfer to the DC-link, it should be taken as 1. After cancelling the zero vectors, the normalized duty cycles for active vectors are represented in (7)

$$\left.\begin{aligned} \acute{m}_\gamma &= \frac{m_\gamma}{m_\gamma + m_\delta} \\ \acute{m}_\delta &= \frac{m_\delta}{m_\gamma + m_\delta} \end{aligned}\right\} \quad (7)$$

3.2. NTVV based modulation on inversion step

Aforementioned that, the inversion step uses a NPC-VSI [16], so modulation of this step, is not like the modulation of the traditional IMC. The electrical connection between the neutral-point of the capacitive input filter and the DC-link mid-point 'o' are necessary to provide a mid-point of 0V and desired two voltage supplies. For proper operation of the converter at three level output voltages, the modulation of this step must provide zero amperes current ($i_o = 0$) through the neutral-point over a switching period.

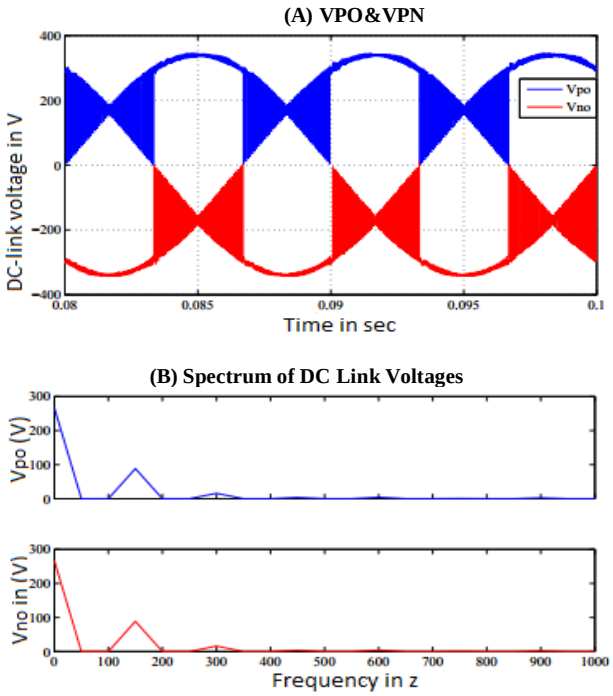


Fig. 6: The DC-Link Voltages (V_{po}, V_{no}) and Its Spectrum.

The unequal charging/discharging of the input capacitive filter can affect the ability of the inversion step to produce three–level outputs and also it will create distortions in the output voltages. This problem is not similar to the balancing problem of neutral-point of the traditional NPC-VSI [16]. The inversion step must use the inconstant DC-link voltages (V_{po} & V_{no}), to produce three-level output voltages.

The DC-link voltage levels (V_{po} & V_{no}) generated by rectification step, are shown in Fig.6. From this figure it's obvious that, these voltage levels are not constant, but however their average values are constant over a switching period. The spectrum of these DC-link voltages consist of third order harmonic and DC components. As the inversion stage consists of 3-phase three-level NPC-VSI, so there are 27 probable switching combinations, representing connections between the output terminals (a, b, c) And the DC-link points (p, o, n). So the inversion step is modulated on the basis of average DC-link voltages i.e. $V_{po,avg}$ and $V_{no,avg}$. In furtherance of explanation, only 27 possible switching states are analysed and listed in table-II [15]. The output voltages produced by every switching combination are resolved using the equations (8) but expressed in respect of $V_{po,avg}$ and $V_{no,avg}$.

$$\left.\begin{aligned} V_{As} &= \frac{1}{3}\{V_{po,avg}(2m_{a1} - m_{b1} - m_{c1}) - V_{on,avg}(2m_{a3} - m_{b3} - m_{c3})\} \\ V_{Bs} &= \frac{1}{3}\{V_{po,avg}(2m_{b1} - m_{a1} - m_{c1}) - V_{on,avg}(2m_{b3} - m_{a3} - m_{c3})\} \\ V_{Cs} &= \frac{1}{3}\{V_{po,avg}(2m_{c1} - m_{a1} - m_{b1}) - V_{on,avg}(2m_{c3} - m_{a3} - m_{b3})\} \end{aligned}\right\} \quad (8)$$

Where m_{x1} and m_{x3} represents the duty ratios of the switching states (S_{1x} & S_{2x}) and (S_{3x} & S_{4x}) for every phase leg. It is considered as '1' while both switches are ON and otherwise '0'.

Table 2: The Space Vectors and Phase Voltages of Output

Switching state			Output-phase voltages			Space vectors of output voltages		
A	B	C	V_{As}	V_{Bs}	V_{Cs}	Vector	Magnitude	Angle
P	P	P	0	0	0	V_0	0V	0
O	O	O	0	0	0			
N	N	N	0	0	0			
P	O	O	$\frac{+2}{3}x$	$\frac{-1}{3}x$	$\frac{-1}{3}x$	V_{S1A}	$\frac{+2}{3}x$	0
O	N	N	$\frac{+2}{3}y$	$\frac{-1}{3}y$	$\frac{-1}{3}y$	V_{S1A}	$\frac{+2}{3}y$	0
P	N	N	$\frac{+2}{3}(x+y)$	$\frac{-1}{3}(x+y)$	$\frac{-1}{3}(x+y)$	V_{L1}	$\frac{+2}{3}(x+y)$	0
P	O	N	$\frac{+1}{3}(2x+y)$	0	$\frac{-1}{3}(x+2y)$	V_{M1}	$\frac{2}{3}\sqrt{(x^2+xy+y^2)}$	$\tan^{-1}(\frac{\sqrt{3}x}{2x+y})$
P	P	O	$\frac{+1}{3}x$	$\frac{+1}{3}x$	$\frac{-2}{3}x$	V_{S2A}	$\frac{+2}{3}x$	$\frac{\pi}{3}$
O	O	N	$\frac{+1}{3}y$	$\frac{+1}{3}y$	$\frac{-2}{3}y$	V_{S2B}	$\frac{+2}{3}y$	$\frac{\pi}{3}$
P	P	N	$\frac{+1}{3}(x+y)$	$\frac{+1}{3}(x+y)$	$\frac{-2}{3}(x+y)$	L_2	$\frac{+2}{3}(x+y)$	$\frac{\pi}{3}$

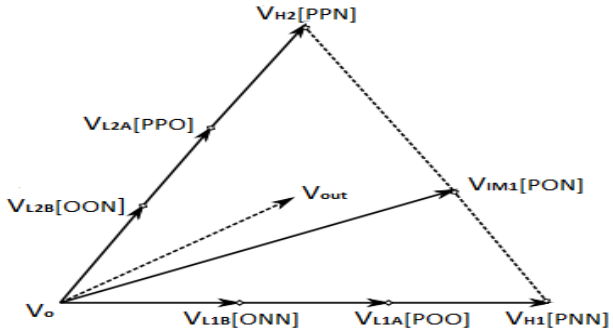


Fig. 7: The Vectors of Unequal DC-Link Voltages For $V_{po'avg} > V_{on'avg}$.

The Fig.7 depicts the space diagram of the voltage vectors for the case of $V_{po'avg} > V_{on'avg}$. From the figure it is obvious that, the low voltage vectors (V_{L1} & V_{L2}) and intermediate voltage vector (V_{IM1}) are overwhelmed by the uneven average DC- link voltages whereas the higher voltage vectors (V_{H1} & V_{H2}) remain unaffected, because of $V_{po'avg} + V_{on'avg} = V_{pn'avg}$. At any instant, each repetitive switching combination of the low voltage vectors produces a contrary voltage vector (V_{S1A} & V_{S1B}) due to the use of distinct DC-link voltages. Other side, the intermediate vector (V_{IM1}) having not only variable amplitude but also variable phase based on $V_{po'avg}$ & $V_{no'avg}$. But this variable amplitude and phase vector (V_{IM}) complicates the synchronizing process of the reference output-voltage vector $\vec{V}$ of the inversion step.

$$V_{out}(t) = \frac{2}{3}\left[V_{As}(t)e^{j0} + V_{Bs}(t)e^{j\frac{2\pi}{3}} + V_{Cs}(t)e^{j\frac{4\pi}{3}}\right] \quad (9)$$

In this step, the concept of NTVV technique [13] is used to produce the desired outputs. This technique can rule the neutral-point balancing difficulty of the traditional NPC-VSI. By using this technique the current ($\boldsymbol{i_0}$) trough neutral-point can be controlled up to zero ampere over a switching period. Thus, it is preventing the deviation of voltage levels of the capacitive input filter against its required levels. The Fig.8 shows the virtual space vectors, obtained by combining linearly the space vectors of voltages. This simplifies the synchronizing process of the reference output-voltage vector $\vec{V}$.

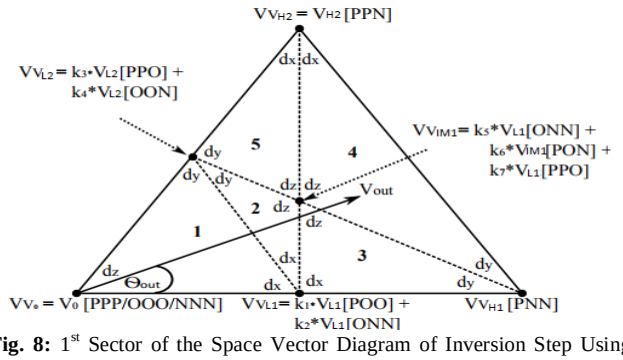


Fig. 8: 1st Sector of the Space Vector Diagram of Inversion Step Using NTVV.

4. Synchronization of switching states of both steps

The synchronization between the switching states of both rectification and inversion steps are required to assure stability between input side currents and output side voltages over a switching interval [15]. Based on the switching pattern of SVM an example for this converter is illustrated in Fig.9.

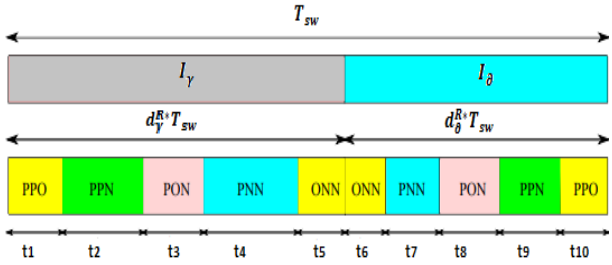


Fig. 9: An Illustration of Synchronization of Both Stages.

5. Simulation and results

The three–level twin-step matrix converter based on NTVV-SVM is designed using Matlab/Simulink software. The simulation parameters are listed in table-III. The input/output waveforms of this converter are analysed for two different modulation indices (mi=0.9 & mi=0.5).

Table 3: Simulation Parameters

Supply	Input filter	Load
230V, 50Hz	Inductor $L_f = .7mH$ Capacitor $C_f = 10\mu F$ Damping resistor $R_d = 10\ ohm$	Resistor $R_L = 20\ ohm$ Inductor $L_{load} = 10\ mH$

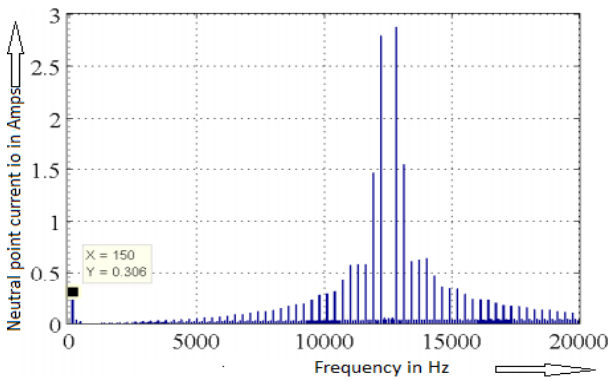


Fig. 10: Spectra Analysis of Neutral Point Current (Ion).

As shown in the Fig.10, it's clear that neutral-point current ($\boldsymbol{i_o}$) includes only the 3rd order harmonics, this confirm that, the voltage levels of the capacitive input filter stay stabilized over a switching interval, as depicted in Fig.11.

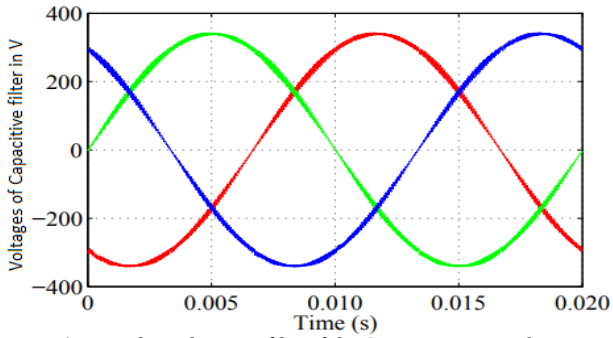


Fig. 11: The Voltage Profiles of the Capacitive Input Filter.

Fig.12 depicts the DC-link voltages obtained from the rectification step, whereas the Fig.12(a) shows the DC- link voltage V_{Pn} and it's split voltages (V_{po} & V_{no}) are shown in Fig.12(b), which are supplied to the inversion stage.

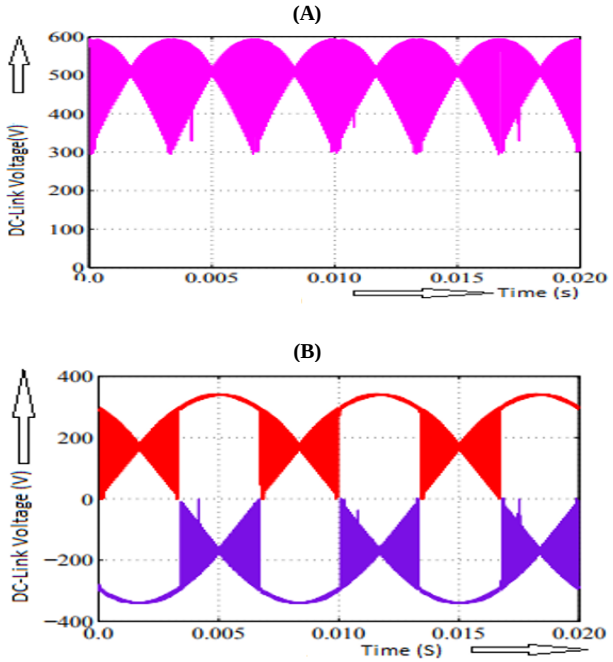
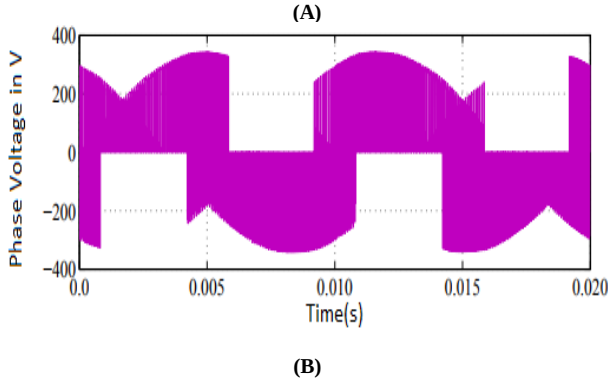


Fig. 12: The DC-Link Voltages and Its Different Levels Produced by Rectification Step.

Fig.13 shows the output waveforms for the modulation indices ($mi = 0.9$) of this converter, that ensure the generation of 3-level outputs.



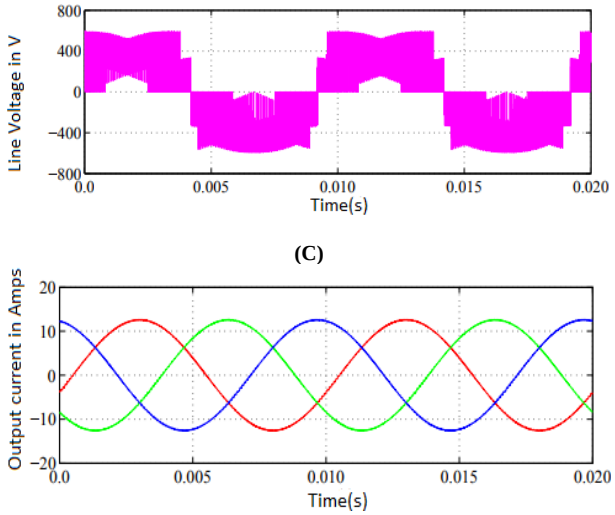


Fig. 13: The Waveforms of Output Voltages for MI=0.9.

Fig.14 shows the output waveforms for modulation index my=0.5 of this converter, which is similar to those of traditional IMC.

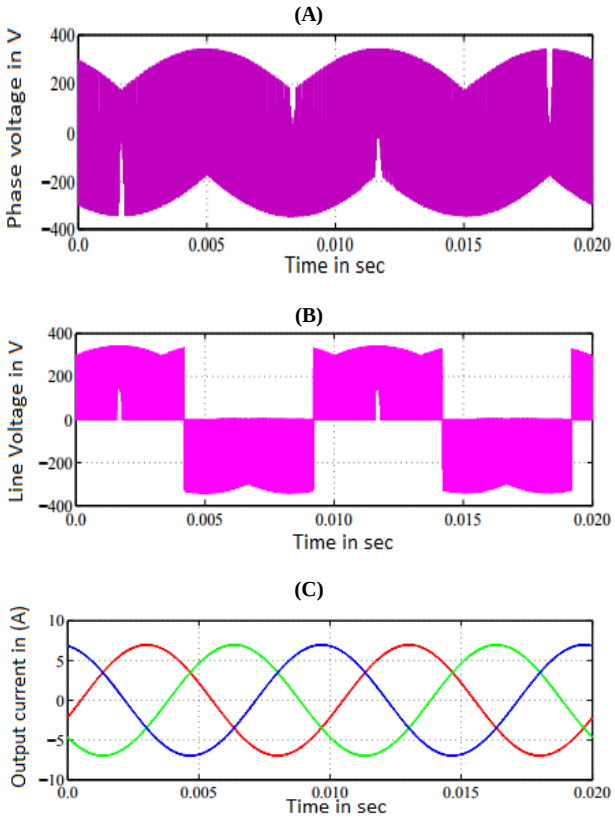


Fig. 14: The Waveforms of Output Voltages for Mi=0.5.

6. Conclusions

The operational principle and control technique SVM based on NTVV for this converter has been illustrated throughout this paper and its simulation results are presented to justify the theoretical studies. The balancing problem of neutral-point of the capacitive input filter has been resolved. The concept of splitting the DC-link voltage (V_{pn}) into two different levels (V_{po}&V_{no}), which is enforced to the inversion step, to ensure generation of three-level output waveforms. The simulation results at different modulation indexes, proves that, at higher modulation index this converter possesses better performance over the traditional IMC.

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