International Journal of Engineering & Technology, 7 (4) (2018) 2569-2574

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET
doi: 10.14419/ijet.v7i4.16061
Research paper

High speed multi-channel data acquisition technique for efficient hardware utilization using quad data rate approach

Priyanka Chauhan [1] *, Dippal Israni [1], Karan Jasani [2], Ashwin Makwana [1]

[1] U and P U Patel Department of Computer Engineering, CSPIT, CHARUSAT
[2] V T. Patel Department of Electronics and Communication Engineering, CSPIT, CHARUSAT
**Corresponding author E-mail: dippalisrani.ce@charusat.ac.in*

Abstract

Data acquisition is the most demanding application for the acquisition and monitoring of various sensor signals. The data received are processed in real-time environment. This paper proposes a novel Data Acquisition (DAQ) technique for better resource utilization with less power consumption. Present work has designed and compared advanced Quad Data Rate (QDR) technique with traditional Dual Data Rate (DDR) technique in terms of resource utilization and power consumption of Field Programmable Gate Array (FPGA) hardware. Xilinx ISE is used to verify results of FPGA resource utilization by QDR with state of the art DDR approach. The paper ratiocinates that QDR technique outperforms traditional DDR technique in terms of FPGA resource utilization.

Keywords: *Data Acquisition System (DAQs); Dual Data Rate (DDR); FPGA; Multi-Channel; Quad Data Rate (QDR).*

1. Introduction

There are certain areas like high speed digital signal processing system, high speed image information conversion, real time processing system as well as radar, communications, chemical, military and medical industry which often requires number of analog signal to be synchronously sampled, so the collected data not only contains simulation signal frequency range of features but also keep the appropriate phase difference between different analog signals [1].To fulfill the requirement of higher and higher accuracy and data rate, data acquisition systems have been developed [2]. Single channel or multichannel signals can be acquired by current data acquisition system. Nowadays, there are a lot of data acquisition systems, some are high-accuracy but not high-speed; some are high-speed but not high-accuracy [3].

This paper proposes a Quad Data Rate (QDR) technique for efficient data acquisition. The QDR effect is advantageous to deliver four bits of data per signal line per clock cycle. QDR is a communication technique where data are transmitted at four points (Two on the rising and falling edges and at two intermediate points between them) in the clock cycle. This intermediate points are defined by a second clock. The second clock is 90° out of phase from the first.

In a quad data rate system, the data lines operate at twice the frequency of the clock signal. This is in contrast to double data rate systems, in which the clock and data lines operate at the same frequency.

This paper is further organized as follows: The next section gives some brief background of researches related to the proposed technique. Section 3 describes the proposed methodology for QDR. The experimental results and discussions of the proposed approach are depicted in Section 4. Finally, conclusions are summarized in Section 5.

2. Literature analysis

Presently, various models are proposed targeting acquisition of data with objective of proper resource utilization of hardware.

2.1. DAQ methods

Data acquisition can be classified as Computer based, Microcontroller based and FPGA based. The computer based data acquisition system uses microprocessor for processing, storing and manipulating the data [1] [2] [4]. The method of embedded microcontroller system has advantages like cheaper cost, better performance and mobility; however fixed architecture is its biggest disadvantage. If any change is required in the system than whole system need to be changed [1] [2] [5] [6]. Last is reconfigurable FPGA. It can be easily understood from its name that it is reconfigurable onboard system. It becomes first choice for any developer because of its high performance and high capacity. It also fulfills all the requirement of data acquisition system like I/O, processing and storage capability [1] [2] [7] [8].

2.2. DAQ protocols

This section describes various protocols used in DAQ system like Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C): UART is a universal asynchronous receive or transmit protocol [1] [9]. To set the synchronized clock information into data stream,

various clock sources are used by sender and receiver [1] [9]. This protocol is used for data communications [1] [9]. SPI allows full duplex synchronous data communication [1] [10 - 12]. It is a synchronous data bus and allows communicating between multiple chips [1] [10 - 12]. SPI protocol has 7 bit address, 8 bit data and 1 bit command. In command instruction "1" indicates SPI write and "0" indicates SPI read. Length of data word is of 8 bits for write access. On receiving falling edge, data write command is given and on receiving rising edge, data read command is given [1] [10 - 12].

I^2C controller bus is a two wire, two direction serial bus [1] [10] [11]. It gives efficient techniques for data communication of short distance multiple devices. It provides better support for communication with slow on –board peripheral devices. It is an easy, low bandwidth, short distance protocol. Because of built in address, it is very easy when used to link multiple devices. Also it is half duplex synchronous interface [1] [11].

2.3. DAQ techniques

In timing diagram, clock signal is having its own importance. Based on type of clock signal whole circuitry takes actions. It is actually having variation between '0' and '1' state. At high frequency operation, clock frequency is having its own limitations. By using two edges of clock, the data signals operate with same clock frequency and data transmission rate is doubled. There are mainly three types of algorithms, Single Data Rate (SDR), DDR and QDR.

SDR is having one common data bus used for read and write action by using one clock [1]. It serves the purpose on rising edge of the signal. Advantage of SDR is that it is very easy to implement and complexity level of SDR is also very low [1]. In addition to that, bandwidth of SDR is lower than DDR. Maximum of one word of data can be transferred per clock cycle by using SDR [1].

DDR is also having one common bus as SDR [7]. It is used for read action as well as write action by using line clock [1] [2] [7] [13]. Data is transferred on both the edges of the clock signal. DDR is most efficient when only one request type is frequently repeated [7]. DDR can be used for Ultra-3 SCSI, microprocessor front side busses, Graphics Accelerator [7]. At high frequency signal integrity limits clock frequency [7]. This can be considered as disadvantage of DDR [7].

QDR uses two different clocks. One is used for read action and another is used for write action, hence it has separate read and write data buses. Moreover it transfers data on both edges of clock signal. Thus it is definitely more efficient than DDR or SDR. Major use of QDR is in high speed communications and networking applications [14]. One thing must be noted that, even though in QDR two clocks are used in compare to DDR but speed is not doubled. Hence using QDR technique resources are less utilized still speed remains same [15].

Various parts of proposed system are as given in Fig. 1.

2.3.1. Command interface

It can be considered as main element of the system. Responsibilities like generation of necessary driving signals for the sensor are given to command Interface [16] [17]. In addition to that, it may be further used to generate clocks required by sensor and other interface, preparation of data for UART interface, Communication with sensor over SPI, Communication with PC or outer world over serial communication interface. Command interface is capable to communicate with data controller for transfer and storage of the data to Static Random Access Memory (SRAM) [18].

While communicating with command interface; acquisition module, SRAM and memory controller plays vital role [18]. Memory controller can be considered as a kind of bridge between SRAM and command interface. For writing and reading purposes, memory controller calculates addresses. P. Chauhan et al. [1. have used all above techniques. However, it uses traditional DDR technique.

All above techniques uses DDR for acquisition of data. This techniques leads to poor resource utilization. There is a need for proper resource utilization by not negotiating with power consumption. This paper proposes a QDR approach which not only solves the resource utilization problem but also maintains the power consumption.

3. System design

Handling data at high data rate and efficient storage mechanism using minimal resources is the main feature of data acquisition [15]. Functional blocks of proposed system are as given in Fig. 1. This chapter describes functionalities of each block present in the proposed system.

Memory controller are used to generate control signal for SRAM like read enable, write enable, DATA, ADDRESS, Control Enable1 (CE1), Control Enable1 (CE2) etc.

3.1. Word alignment

Transmitted signal is actually considered as a series of continuous bits. For receiver, it is very hard to identify between starting and ending bit of first word. Word alignment becomes key feature for such kind of problem. It properly identifies starting and ending bit of the word.

To identify starting and ending bit of the word, continuous pattern monitoring of word transmitted by sensor is necessary. By using SPI command this pattern can be calibrated. It might happen that sampled word is somewhat different than calibrated word. Shifting 1 bit of word can be done while sampling until desired word matches with calibrated word.

3.2. Bit alignment

The use of bit aligner is for placing the sampling point in proper region of stable data in acquisition system [1] [2] [7]. Anyone can sample data using bit aligner [1] [2]. Bit aligner serves its purpose by adding delay in input signal, so data channel moves corresponding clock signal [1] [2].

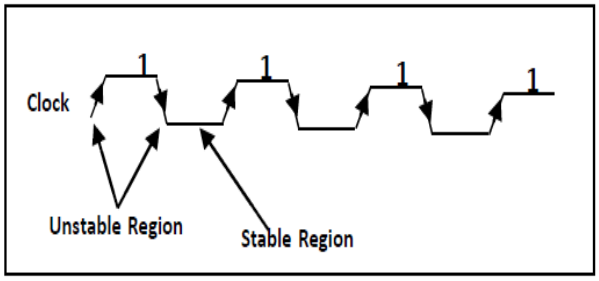

Fig. 2: Bit Alignment.

One bit region contains two characteristics. One is transition region and another is stable region. Movement of clock from 0 to 1 indicates rising edge and movement of clock from 1 to 0 indicates falling edge. These two transition regions are unstable as shown in Fig. 2. Noise and jitter are the reason behind generation of such type of signal in clock. Data collected in unstable region leads to erroneous data sampling. It can be called as stable region if there is no transition in clock. To be assured for correct collected data, collection of data needs to be in stable region.

By calculating two unstable regions, stable regions are found. Between every pair of unstable transitions there is a stable region, so the technique suggests that sampling needs to be continuous for small regions until two regions are sampled.

3.3. FIFO buffer write

FIFO buffer is widely used to compensate the data rate mismatch between two devices [16].

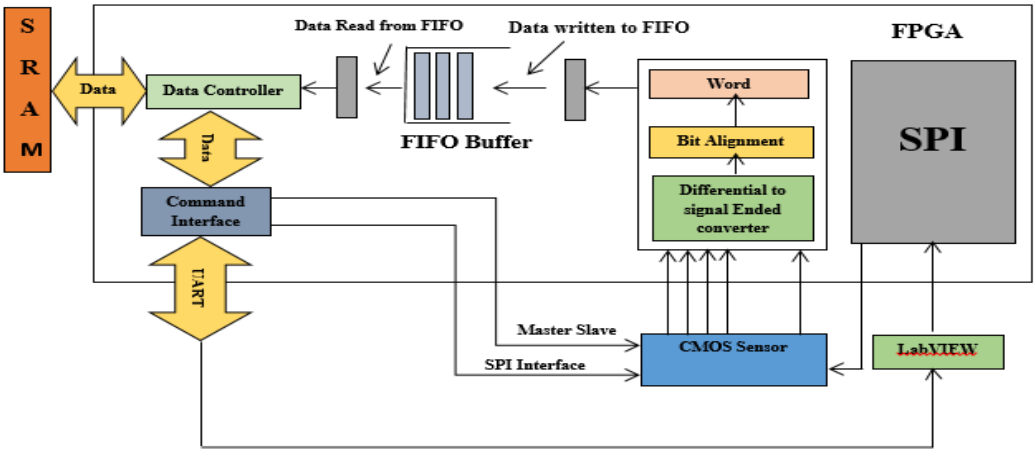

Fig. 1: Proposed System Diagram.

The data rate of data acquisition is most of the times different than data storage rate in to SRAM [16]. So in such conditions FIFO buffer is used. Data needs to be reprocessed before it stored into SRAM in the case of multi-channel [1] [2].

4. Proposed algorithm

This research proposes technique to sample the data. As shown in Fig. 2 for data clock, sampling can be done at rising as well as falling edge.

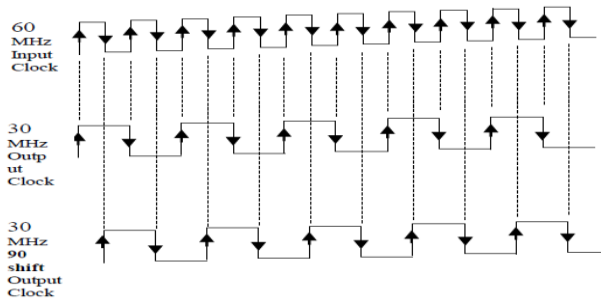

Fig. 3: QDR Clock.

FPGA cannot detect rising and falling edge together in single process. The proposed system rectifies this issue. Input clock is of 60 MHz as shown in Fig. 3. Now to sample the data on rising and falling edge of input signal clock, two different output clocks are generated. First clock is having half the frequency of input clock frequency. So from that clock, rising edge data will be received. Second clock frequency is also of half the input clock frequency but it is 90° shifted from the first clock. So it will receive data from falling edge of input clock. This is how rising and falling edge data from input clock is received by generating two different clocks.

In this algorithm there are four separate processes, one process works on rising edge of the normal_clock, second process works on falling edge of the normal_clock, third process works on rising edge of the shift_clock and last process works on falling edge of the shift_clock.

As shown in Fig. 4, there are six temporary buffers, four unsigned integer counters (i.e. two even counter and two odd counterl and one result vector). Data type of buffers and result are standard logic vector i.e. they will store the series of 0 or 1.

Fig. 4 describes the initialization of temporary buffers and counters. All the buffers are initialized with logical '0' and two even counters and two odd counters are initialized by 0, 1, 2 and 3 respectively.

During first rising edge of clock D0 will be stored in TEMP_BUF1 and even counter will increase by 4. During first rising edge of shift clock D1 will be stored in TEMP_BUF3 and odd counter will increase by 4. During first falling edge of clock, D2 will be stored in TEMP_BUF2 and even counter1 will increase by 4. During first falling edge of shift clock, D3 will be stored in TEMP_BUF4 and odd counter1 will increase by 4.These operation works until last bit D9 is stored.

Final data word is stored into the RX_TEMP_DATA vector by having a logical OR operation between RX_TEMP_EVEN_DATA and RX_TEMP_ODD_DATA. Finally, result would be stored into the FIFO buffer in its respective place.

5. Experimental setup and result analysis

Xilinx Spartan-6 FPGA board is used to make prototype of Data acquisition system. CYPRESS 2 M × 16 static RAM (SRAM) have been used for data storage. For designing purpose ISE 12.4 platform and VHDL have been used. CMOSIS CMV 4000 CMOS image sensor is used as data source. One DC power supply has been used to drive the whole system. For board to PC communication UART have been used with LabVIEW. The block diagram and experimental setup of the system are shown Fig. 1.

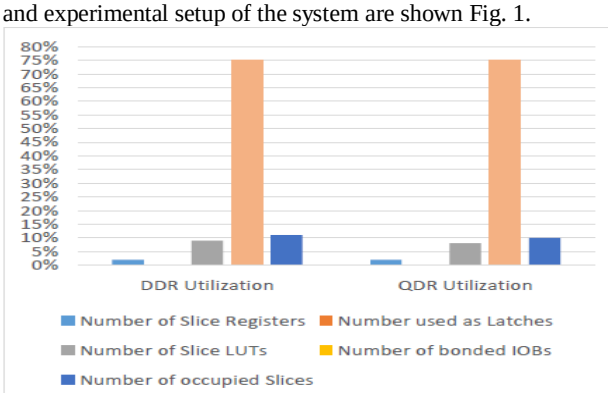

Fig. 5: Device Utilization Summary of DDR and QDR.

Table I shows comparison between DDR and QDR algorithm. While analyzing both algorithms together, number of slice registers utilization in DDR and QDR are same. The same condition is present for number used as latches. However while discussing about number of slice LUTs, the scenario slightly differs. The number of DDR LUTs is higher than QDR. This gives advantages to QDR over DDR. Whereas in terms of number of bonded IOBs, DDR used is same as QDR. While considering number of occupied slices, DDR is higher than QDR which makes QDR more efficient.

In Fig. 6. Comparison of different resource utilization of DDR and QDR algorithm is described. The Numbers used as logic is low in

QDR. Also while considering number with an unused Flip-Flop QDR becomes more efficient than DDR. The number of full used Look up Table – Flip Flops (LUT-FF) pairs are also lesser in QDR than DDR. While discussing about number of LOCed IOBs, QDR and DDR are different. In the case of Number of RAMB8BWERs, Number of BUFIO2/BUFIO2_2CLKs and Number of BUFIO2FB/BUFIO2FB_2CLKs, DDR and QDR are same.

Table 1: Comparison of DDR and QDR

Slice Logic Utilization	DDR Utilization	QDR Utilization
Slice Registers (↓)	2%	2%
Latches(↓)	0%	0%
Slice Look Up Table (LUTs) (↓)	9%	8%
bonded Input Output Blocks (IOBs) (↓)	75%	75%
occupied Slices (↓)	11%	10%

Here, ↓ indicates lower the better.

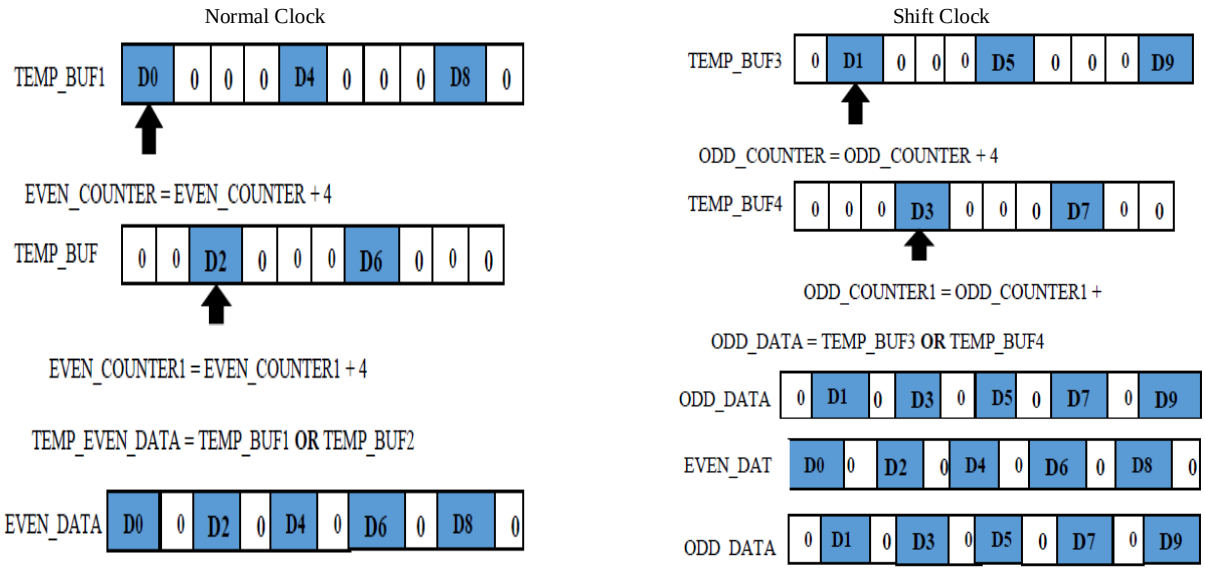

Fig. 4: Algorithm Operation.

However when considering Number of RAMB16BWERs, QDR goes ahead of DDR. Now in Number of DCM/DCM_CLKGENs, DDR is higher than QDR. So QDR is efficient in this case. But when considering Number of PLL_ADVs, QDR is more than DDR. The reason behind this can be justified as to generate shift clocks, more PLL_ADVs are used.

Fig. 7 analyzes power consumed by DDR algorithm. While analyzing it has come to notice that total power consumed while using DDR algorithm is 0.2 watt. Total power consumed is divided in two types. One is dynamic and another is quiescent. Dynamic consumption is 0.112 watt and quiescent is 0.088 watt. The junction temperature is 33.5 °c while using DDR algorithm.

Fig. 8 shows power analysis while using QDR algorithm. Total power consumed while using QDR algorithm 0.2 is Watt. So it is same as DDR algorithm power consumption. But dynamic consumption is 0.061 watt and quiescent consumption is 0.139 watt. The junction temperature is 33.5 °c, which is same as DDR algorithm.

Slice Logic Utilization	**DDR Utilization [2]**	**QDR Utilization**
Number used as logic	9%	8%
Memory Slice	0%	0%
Unused Flip-Flop	51%	43%
Number of full used LUT-FF pairs	43%	50%
LOCed IOBs	62%	61%
RAMB16BWERs	56%	50%
RAMB8BWERs	1%	1%
BUFIO2/BUFIO2_2CLKs	3%	3%
BUFIO2FB/BUFIO2FB_2CLKs	3%	3%
DCM/DCM_CLKGENs	25%	0%
Number of PLL_ADVs	50%	100%

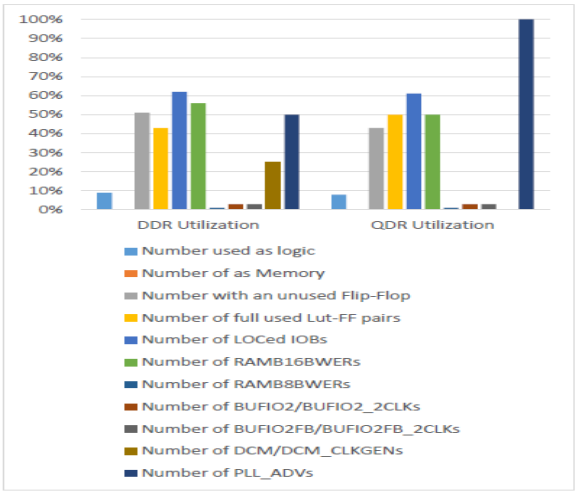

Fig. 6: Device Utilization Summary of DDR and QDR.

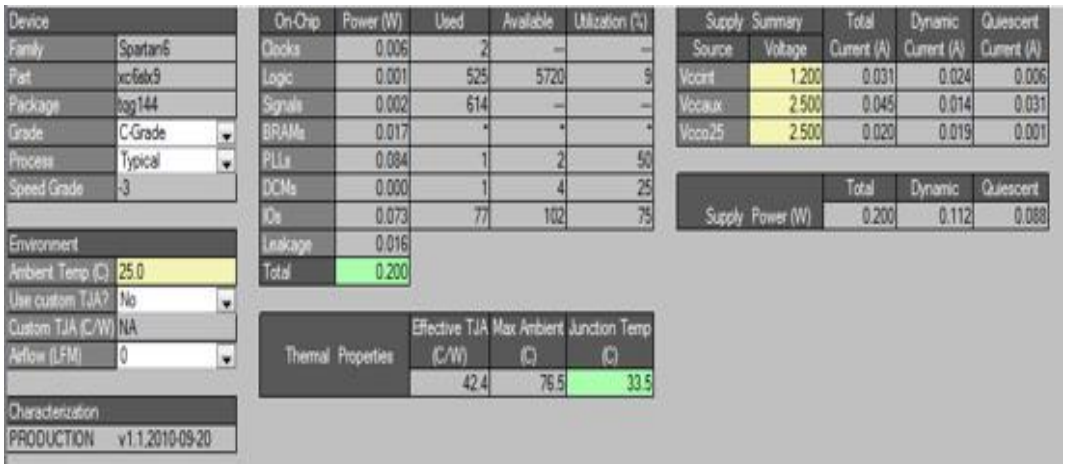

Fig. 7: DDR Algorithm Power Analyzer.

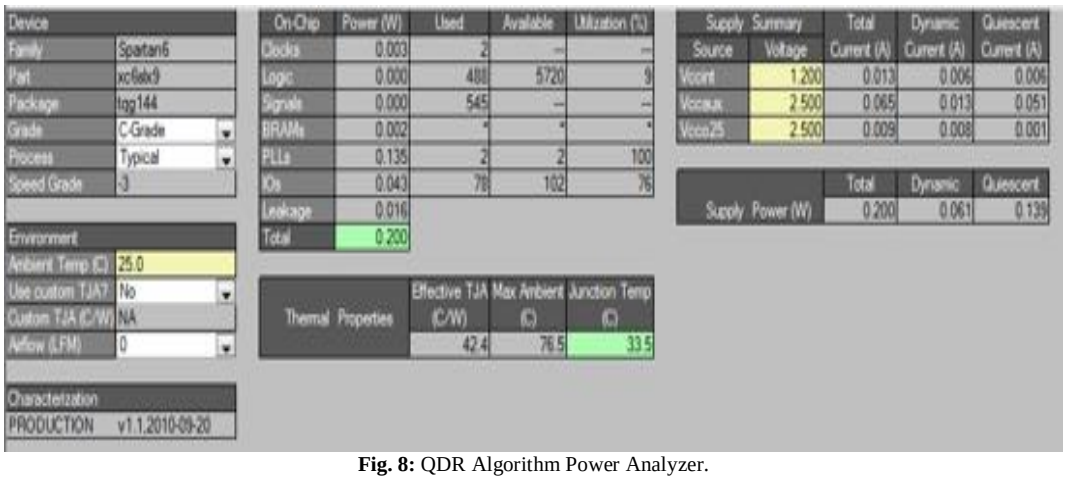

Fig. 8: QDR Algorithm Power Analyzer.

6. Conclusion

This paper proposes a novel method for efficient resource utilization and power consumption of FPGA. This work compares advanced Quad Data Rate (QDR) technique with traditional Dual Data Rate (DDR) technique. With the help of Xilinx IDE, results of FPGA resource utilization by QDR and DDR are discussed. The resource utilization parameters include LUTs, IOB, LUT-FF pairs, Flip-flops. It has been concluded that QDR technique is having more advantages as compared to traditional DDR technique in terms of FPGA resource utilization without compromising power consumption.

Acknowledgement

The authors would like to thank Charusat Space Research and Technology Center (CSRTC) of Chandubhai S. Patel Institute of Technology (CSPIT) for providing required resources to carry out work

References

[1] P. Chauhan, D. Israni, A. Makwana and K. Jasani, "Hardware Design of an Efficient High Speed Multi-Channel Data Acquisition Using DDR", In: *Proc. of IEEE International Conf. for Convergence of technology*, April 2017.

[2] R. Mehta, D. Israni, K. Jasani, A. Shah, "FPGA Realization of Novel Techniques for DDR based Data Acquisition System", In: *Proc. of 2nd International Conf. on Next Generation Computing Technologies*, Dehradun, India, 14-16 October 2016 https://doi.org/10.1109/NGCT.2016.7877469.

[3] C. XiaoQiang, Z. Jun, and X. Xing. "Portable data acquisition system based on FPGA and USB", International Journal of Intelligent Engineering and Systems, Vol. 6, No. 2, 2013.

[4] He Zhiqiang, Zhang Jingzhi and Zeng Wenxian, "Design and implement of a band-pass FIR filter based on FPGA in multi-channel data acquisition system", In: *Proc. of 10th International Conference on Electronic Measurement & Instruments (ICEMI), Chengdu*, pp. 49-52, 2011.

[5] J. R. Payne and B. A. Menz, "High speed PC-based data acquisition systems", In: *Proc. of Industry Applications Conference, Orlando, FL*, pp. 2140-2145 Vol.3, 1995.

[6] S. Arunaganesan, J. Adhavan, G. S. Reddy and M. Venkatesan, "Data acquisition system based on 8051 microcontroller for cutting tool temperature measurement", In: *Proc. of IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), Enathi*, pp. 1-4, 2013. https://doi.org/10.1109/ICCIC.2013.6724154.

[7] A. Tiwari, "A low power high speed dual data rate acquisition system using FPGA", In: *Proc. of Communication, Information and Computing Technology (ICCICT) International Conference on, Mumbai*, pp. 1-4,2012. https://doi.org/10.1109/ICCICT.2012.6398101.

[8] M. Abdallah and O. Elkeelany, "A Survey on Data Acquisition Systems DAQ", In: *Proc. of International Conference on Computing, Engineering and Information*, Fullerton, CA pp. 240-243, 2009.

[9] Y. Y. Fang and X. j. Chen, "Design and Simulation of UART Serial Communication Module Based on VHDL", In *Proc. of 3rd International Workshop on Intelligent Systems and Applications (ISA), Wuhan*, pp. 1-4, 2011. https://doi.org/10.1109/ISA.2011.5873448.

[10] Design, Implementation and Functional Verification of Serial Communication Protocols (SPI and I2C) on FPGAs", *HCTL Open International Journal of Technology Innovations and Research*, Vol. 4, July 2013.

[11] A. K. Oudjida, M. L. Berrandjia, R. Tiar, A. Liacha and K. Tahraoui, "FPGA implementation of I2C & SPI protocols: A comparative study", In: *Proc. of 16th IEEE International Conference on Electronics, Circuits, and Systems, Yasmine Hammamet*, pp. 507-510, 2009.

[12] "Design and implementation of a high speed Serial Peripheral Interface", In: *Proc. of International Conference on Advances in Electrical Engineering (ICAEE), Vellore*, pp. 1-3, 2014.

[13] Liu Junzhi, "Design of a dual channel high-speed wideband synchronous data acquisition system", In: *Proc. of 12th IEEE International Conference on Electronic Measurement & Instruments (ICEMI), Qingdao*, pp. 295-299, 2015.

[14] H. Subramoni, M. Koop and D. K. Panda, "Designing Next Generation Clusters: Evaluation of InfiniBand DDR/QDR on Intel Computing Platforms", In: *Proc. of 17th IEEE Symposium on High Performance Interconnects*, New York, NY, pp. 112-120, 2009. https://doi.org/10.1109/HOTI.2009.24.

[15] S. Shujing and W. Zenggang, "The design of multi -channel data acquisition system based on FPGA", In: *Proc. of International Conference on Consumer Electronics, Communications and Networks (CECNet)*, XianNing, pp. 5361-5364, 2011. https://doi.org/10.1109/CECNET.2011.5768783.

[16] V. Schatz, "Synchronised data acquisition for sensor data fusion in airborne surveying", In: *Proc. of 11th International Conference on Information Fusion*, Cologne, pp. 1-6, 2008.

[17] L. Njejimana , "Design of a Real-Time FPGA-Based Data Acquisition Architecture for the LabPET II: An APD-Based Scanner Dedicated to Small Animal PET Imaging", *IEEE Transactions on Nuclear Science*, Vol. 60, No. 5, pp. 3633-3638, Oct. 2013. https://doi.org/10.1109/TNS.2013.2250307.

[18] S. Velmurugan and C. Rajasekaran, "A reconfigurable on-chip multichannel data acquisition and processing (DAQP) system for multichannel signal processing", In: *Proc. of International Conference on Salem Pattern Recognition Informatics and Mobile Engineering (PRIME)*, pp. 109-114, 2013. https://doi.org/10.1109/ICPRIME.2013.6496456.