Thermal energy aware proportionate scheduler for multiprocessor systems

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Abstract

As per Moore’s law, the power consumption and heat solidity of the multiprocessor systems are increasing proportionately. High temperature increases the leakage power consumption of the processor and thus probably escort to thermal runaway. Efficiently managing the energy consumption of the multiprocessor systems in order to increase the battery lifetime is a major challenge in multiprocessor platforms. This article presents Thermal Energy aware proportionate scheduler (TEAPS) to reduce leakage power consumption. Simulation experiment illustrate that TEAPS reduces 16% of energy consumption with respect to Mixed Proportionate Fair (PFAIR-M) and 36% of energy consumption with respect to Proportionate Fair (PFAIR) Schedulers on the system consisting of 20 processors under full load condition.

Keywords: Multiprocessor Systems; Energy Aware Scheduling; Thermal Runaway; Leakage Awareness; Critical Speed.

1. Introduction

Power density of the multiprocessor systems have doubled for every three years and this rate is expected to increase [1]. The resulting high temperature can lead to reliability issues and increase the cost of packaging and cooling. A 10^6 C to 15^6 C increase in temperature could lead to twice reductions in the lifetime of the device [2] due to the non uniform power distribution of the multiprocessor system. Localized heating climbs much quickly than the entire chip, escorting to non-uniform temperature distribution on the chip with high-temperature hot spots and spatial gradients [3]. In order to control the on-chip temperature conventional methods to utilize enhanced packaging and cooling techniques such as dynamic fan cooling, water nipping and heat pipe. These methods are not appropriate due to space restrictions. Electronic design automation (EDA) flow permits the system to deal with the thermal contact on various on-chip parameters and integrate the consequences of non-uniform thermal profiles during IC design progression. These techniques are not suitable to compact with runtime situations. This article focus on software looms for thermal energy management. These approaches are flexible and eliminate the limitations described above.

In Dynamic Voltage Scaling (DVS) technology, a processor has a set of operating frequencies mapped to the supply voltage [4]. Slowdown approach is used to reduce dynamic power consumption through DVS mechanism. Slowdown techniques are generally categorized as static slowdown based on the off-line investigation and dynamic slowdown based on the on-line investigation of the task set characteristics [5]. This paper offers a thermal energy aware scheduling mechanism to minimize the leakage power consumption in the multiprocessor system.

It assures resource utilization, guaranteed fairness and accuracy. This paper is structured as pursues: Section 2 gives the concise results for ample datasets are offered in Section 4. At very last, Section 5 presents the conclusion.

2. Related works

Dynamic power management (DPM) stays the system components into shutdown/ sleep states whenever they are idle [6]. Bringing back the system components into active state require more energy hence DPM is efficient only when the idle interval is greater than the threshold level. CMOS power consumption mainly depends on the supply voltage and frequency. Wayne wolf suggested that the power consumption of CMOS can be decreased by varying the voltage and frequency by maintain the entailed performance. DVFS (Dynamic Voltage Frequency Scaling) scheduler reduces the power consumption of the system with the help of Wayne wolf principle [7], [8]. Later combination of more than one voltage–frequency is used to reduce the system energy consumption [9]. Amalgamation of DVFS and Power down technologies is represented in [10-13]. It provides better energy savings when compared with DVS alone [14]. Hybrid Power Management (DPM+DVFS) Scheduling offers enhanced performance and energy savings [15]. PFAIR scheduler provides slot based approach. It is optimal for periodic tasks on multiprocessor systems [16]. To improve the quantum boundaries of the PFAIR scheduler two optimal techniques are proposed namely PF [17] and PD [18]. Anderson proposed optimal early release fair scheduler (ERFAIR) and tendered novel algorithm labeled PD2. It is also termed as mixed PFAIR or modified PFAIR (PFAIR-M) [19].
3. TEAPS algorithm

Thermal Energy aware Proportionate scheduler (TEAPS) is proposed in order to increase the battery life time of the multiprocessor systems by minimizing the thermal leakage energy of the system. This work considers independent periodic task set with hard deadlines over homogeneous multiprocessor platform under symmetric shared memory architecture. It integrates the DVFS with PFAIR scheduler. This model adopts global scheduling approach under preemption mechanism.

Generally dissipation of electric energy, heats the device. Temperature rise of device depends on amount of energy dissipation, device heat capacity and heat flow between the device and environment. As per Moore’s law the power consumption and heat solidity are increasing proportionately for the multiprocessor systems. Bar of cross section A, length l, connecting heat source with temperature $T_{source}$ and heat sink with temperature $T_{sink}$. Heat flow $P_{heat}$ across the bar between two bodies can be described as

$$P_{heat} = H_b A \frac{T_{source} - T_{sink}}{t}$$

Here $H_b$ represents bar heat conductivity.

Energy consumption due to thermal leakage ($E_{heat}$) can be represented in terms of $P_{heat}$ as

$$E_{heat} = P_{heat} \times t$$

Here $t$ represents the time period of the processor. It clearly indicates the energy consumption of the system is directly proportional to the power consumption.

Temperature difference between die and environment $\Delta T$ is determined by the power dissipation in the die and thermal conductivity of the package $H_{package}$. Thermal conductivity of the package depends on the package geometry, size and material used. Its value is in between 0.1 and 1W/°C.

$$\Delta T = \frac{P_{die}}{H_{package}}$$

Here $P_{die}$ represents total power dissipated in the die.

3.1. System model

The system consist ‘m’ homogeneous processors $P_1$, $P_2$ ...... $P_m$. It consists of ‘N’ independent periodic tasks {$\tau_1$, $\tau_2$....$\tau_N$} with hard deadlines. The distinctiveness of each task is characterized as $(C_i, p_i, d_i)$ here $C_i$ indicates task worst case execution time, $p_i$ denotes the time period and $d_i$ represents the deadline of the task. The priorities of the tasks are assigned based on their deadlines. It allows preemption mechanism. It tries to schedule tasks such that in t time slots from arrival of task $t_i$, at least $\lfloor \frac{C_i}{p_i} \rfloor$ a unit of execution time is given. The total utilization of the task set

$$U = \sum_{i=1}^{N} \frac{C_i}{p_i} \leq m$$

Here $(C_i/p_i)$ represents weight of the task. The challenge in integrating DVFS with the PFAIR algorithm is that a task’s parameters must change when scale down the task in order to reduce the thermal energy consumption. When a task is scaled down, its execution time changes according to the new frequency and the PFAIR scheduling algorithm needs to modify the weight of a task as per the new frequency. To maintain acceptability of the PFAIR scheduling algorithm and to accommodate the notion of variable weights; TEAPS calculate the lag and characteristic string of a task incrementally. The weight of task $t_i$ in slot t is defined as $w_{t_i}$. The lag of a task at time t is computed incrementally as

$$\text{lag}(\tau_i, t) = \text{lag}(\tau_i, t-1) + w_{t_{i-1}}(5)$$

For all t>0 and its value becomes zero when t=0.

The ideal allocation (id) of a task at a time t is

$$\text{id}_{i} = \text{id}_{i-1} + w_{t_{i-1}}(6)$$

The characteristic string of a task at a time t is

$$\alpha_t(\tau_i) = \text{sign}(\text{id}_{i+1} - \lfloor \text{id}_i \rfloor - 1)$$

3.2. Working principle

TEAPS enables the processors to function with different voltage levels in order to eliminate the temperature emergency to diminish the energy consumption of the system. TEAPS minimizes the execution of the task without defy the timing limitations.

Algorithm 1 describes TEAPS mechanism. Scheduler assigns ready high priority task to the available processor. Initially processor runs under maximum frequency ($f_{max}$) condition. TEAPS periodically computes the predicted temperature of the processor ($T_{pk}$) depend on the current temperature ($T_{ck}$), neighbor processor temperature ($T_i$), power consumption of the processor ($P_k$) and processor floor planning parameters $\alpha$ and $\beta$. TEAPS compares predicted temperature with the threshold temperature of the processor ($T_{th}$).

$$T_{pk} = T_{ck} + \sum_{k=1}^{n-1} \theta_k (T_i - T_{ck}) + \beta_k P_k$$

If the predicted temperature is exceeding the threshold temperature value then the scheduler scale down the speed of the processor to diminish the thermal energy leakage on the processor. TEAPS runs the processor at minimum frequency ($f_{min}$) and it updates the weight of the task as per new frequency is

$$w_t = C_{i,j}^{new} / P_i$$

Here $C_{i,j}^{new}$ is the run time of a task with workload at a frequency ‘$f_{new}$’.

TEAPS always guarantees that the minimization of the speed is not at all located beneath the critical speed. The speed of the processor under minimum frequency condition is called critical speed. To implement the task beneath the critical speed will increases the chances of missing the deadline and it’s not energy efficient. Else the predicted temperature is below the threshold temperature value then the scheduler allows the processor to run under maximum frequency ($f_{max}$) and it updates the weight of the task as per the frequency.

3.3. Processor model

It considers ARM7TDMI based LPC2148 microcontrollers for implementation. The system consists of 20 ARM7TDMSYSTEMS which are connected under symmetric shared memory architecture. It represents homogeneous multiprocessor platform. Operating points of ARM7TDMI are represented in the table 1. ARM7TDMI processors are equipped with thermal sensors to detect the over-heatings on chip. The processors will be throttled if the on-chip temperature exceeds a certain predefined threshold. Thermal sensors produce noise in the data which may result inaccuracy in the final output. Cochran and Reda proposed Nyquist-Shannon sampling technique to estimate temperature characteristics of the whole chip by using [20]. The absolute estimation error of temperature characteristics of the chip is only 0.6%. TEAPS control the high temperature on the processor in order to reduce the leakage power consumption.
Table 1: Operating Points of ARM7TDMI

<table>
<thead>
<tr>
<th>Operating Points</th>
<th>Clock Frequency (MHz)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>f&lt;sub&gt;min&lt;/sub&gt;</td>
<td>12</td>
<td>2.8</td>
</tr>
<tr>
<td>f&lt;sub&gt;+&lt;/sub&gt;</td>
<td>24</td>
<td>3.0</td>
</tr>
<tr>
<td>f&lt;sub&gt;max&lt;/sub&gt;</td>
<td>48</td>
<td>3.1</td>
</tr>
<tr>
<td>f&lt;sub&gt;max&lt;/sub&gt;</td>
<td>60</td>
<td>3.3</td>
</tr>
</tbody>
</table>

Algorithm 1: Sample TEAPS Algorithm

for i=1 to N do
for k=1 to m do
Assign f← f<sub>max</sub>
Calculate T<sub>Pk</sub> = T<sub>c</sub> + ∑<sub>i=1</sub><sup>m</sup>α<sub>k</sub>(T<sub>i</sub> - T<sub>c</sub>) + β<sub>k</sub>P<sub>k</sub>
if (T<sub>Pk</sub> > T<sub>th</sub>) then f<sub>min</sub> ← f<sub>max</sub>
Update weight of task as per new frequency
w<sub>k</sub> = C<sub>P</sub><sub>k</sub>/p<sub>i</sub>
else f<sub>min</sub> ← f<sub>max</sub>
Update weight of task as per new frequency
w<sub>k</sub> = C<sub>P</sub><sub>k</sub>/p<sub>i</sub>
end if
end for
end for

4. Results

Simulation based trials were performed to compare the efficiency of the proposed scheduler with PFAIR and PFAIR-M schedulers. In Proportionate fair (PFAIR) scheduler, each task is performed at an estimated uniform rate by breaking it into a series of quantum length subtasks. Mixed PFAIR (PFAIR-M) algorithm provides task partitioning approach. It reduces overhead and improves the performance of PFAIR scheduler. Both of these algorithms don’t concentrate on thermal leakage energy consumption of the system. The proposed TEAPS algorithm curtails the leakage power due to high temperature conditions in order to exploit the system battery life time.

4.1. Datasets

Randomly produced hypothetical task sets are used for simulations. The weights of the tasks were generated using rand fixed sum method [21]. The period of the tasks was taken from normal distributions with σ = μ/5 here μ = 100 hence σ = 20. Number of tasks was ranging from 10 to 100 and number of processors varying from 2 to 20. Different system load values are considered for simulation. ARM7TDMI processor power model is taken into consideration.

4.2. Simulations

This segment investigates the performance of TEAPS algorithm in comparison to PFAIR-M and PFAIR algorithms. System parameters are processors (m), tasks (N), system load (L) and task period (P). The span of a time slot is 1msec. Results in this segment are standard over 100 runs of the scheduler for 100000 time slots of schedule duration on a structure with 20 processors and 30 tasks.

4.3. Discussions

Figure 1 demonstrates the variation of Energy Consumption with the numbers of processors in the system by maintaining number of tasks as 30 and system load as 80%. The average period of a task in the experiment is taken as 500 msec. From the plot it can be seen that the TEAPS algorithm illustrates a linear increase in the energy consumption as the number of processors increases.

The average task weight increases with the processors due to this the execution requirements of single task increases, which cause the increases in the energy consumption of the TEAPS, PFAIR-M and PFAIR algorithms.
4.4. Correctness of TEAPS

TEAPS is correct in the wisdom that no task missed its deadline due to task reweighting mechanism. Basically, PFAIR was developed with static task weights throughout their life time. Task reweighting was modelled as a combination of join and leave properties. The task with current weight leaves the system when the task period. Results illustrate better performance of TEAPS scheduler compared to PFAIR-M and PFAIR algorithms. From the plots it can be noticed that the TEAPS minimizes the thermal energy consumption of the system in order to increase the system battery life time. It reduces 16% of energy consumption compare to PFAIR-M and 36% of energy consumption compare to PFAIR algorithm for the system consisting of 20 processors.

5. Conclusion

In this effort, we offered a novel energy-efficient TEAPS scheduling algorithm to curtail the leakage power due to high temperature. This strategy is applicable in dynamic scenarios. It increases the battery life time of the multiprocessor systems. TEAPS reduces the energy consumption of 16% with PFAIR-M and 36% with PFAIR scheduler on the system consisting of 20 processors under full load. It is feasible and optimal for periodic task sets on multiprocessor systems. It is recommended to enable multiple frequency operating conditions for minimizing the power consumption of multiprocessor systems further more without violating the timing constraints.

Competing interests

The authors declare that they don’t have the competing interests.

References

