DA Based Systematic Approach Using Speculative Addition for High Speed DSP Applications

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Abstract

In recent years Parallel-prefix topologies has been emerged to offer a high-speed solution for many DSP applications. Here in this paper carrier approximation is introduced to incorporate speculation in Han Carlson prefix method. And overall latency is considerably reduced using single Brent-Kung addition as a pre and post processing unit. In order to improve the reliability error detection network is combined with the approximated adder and it is assert the error correction unit whenever speculation fails during carries propagation from LSB segment to MSB unit. The proposed speculative adder based on Han-Carlson parallel-prefix topology attains better latency reduction than variable latency Kogge-Stone topology. Finally, multiplier-accumulation unit (MAC) is designed using serial shift-based accumulation where the proposed speculative adder is used for partial product addition iteratively. The performance merits and latency reduction of proposed adder unit is proved through FPGA hardware synthesis. Obtained results show that proposed MAC unit outperforms both previously proposed speculative architectures and all other high-speed multiplication methods.

Keywords: Parallel-prefix adders, Speculation, MAC, and FPGA design etc.

1. Introduction

Binary addition has been emerged and most widely used in many DSP and wireless applications. It is also basic building blocks in arithmetic’s such as multiplication and division. To reduce the delay and arithmetic complexity of the adder many works has been investigated using various contexts [1]. In most cases, the significant performance degradations happen only because of bit width of the adder. The speculative techniques [3–4] are widely used as countermeasure measures, which can be used to reduce sub-logarithmic delays by reducing critical path of the active input operands. On the other side parallel prefix architectures were used [5] for High speed accumulations in many digital devices. Recently, a numerous techniques are emerged such as Brent-Kung [6], Kogge-Stone [7], Sklansky [8], Han-Carlson [9], Ladner-Fischer [10]. In this paper, speculative prefix structures is presented for Ling carry computation to achieve both simplicity and high speed accumulation. The hardware complexity overhead due to the inclusion of error recovery is negligible as compared to critical path reduction techniques through several pipelined architectures without causing any latency issues. This paper, for the first time, we present speculation with variable latency to link equations via parallel-prefix computation. This work is also permitted to design high-speed and unique MAC hardware structure using single adder unit, thereby making them suitable for any DSP applications. To prove the efficiency of the proposed multiplier unit it is compared with state-of-the-art methods like high speed vedic and high radix booth multipliers.

Moreover, this methodology has several attractive features such as low complexity and high performance. Also, the Distributed arithmetic (DA) technique is used to get high performance for FIR filter design, where all bits of one tap unit are processed within the bounded delay.

2. Hybrid Parallel-Prefix Using Ling Computation

The goal for high-speed parallel architectures with reduced critical path employs a Han-Carlson prefix topology with carry generation using single Brent-Kung in both pre and post processing unit.

A. Speculative Prefix-Processing

The speculative computation is led the major differences in both latency and speed of accumulation compared to conventional prefix architectures. During speculative computation instead of waiting for carry propagation from least significant regions, approximated values are generated and propagated to the most significant sub block regions; in the post processing if approximation is not match with actual carries obtained from LSB block side error correction is asserted with causing any significant increment in critical path delay as shown in Fig 2.
3. Experimental Results

All types of adder unit was described in Verilog HDL and mapped on ALTERA cyclone FPGA, using the QUARTUS II EDA Design Compiler tool. Each adder unit was designed recursively to optimize the critical path with intention of getting minimum possible delay as shown in Fig 3. The generated net lists (.edif file) as shown in Fig 4 were forwarded to timing analyzer tool in order to compute the speed after post-routing of the design. All the speed constraints (operating conditions), such as temperature, paths of global clock, scaling level of positive edge to negative edges were held constant for all adder architecture.

A. Speed and Area Trade Off Performance

Here both speed and hardware utilization rate is totally depends on the number of bits used in the input operands and the re-configuration rate, and the key sizes used in each stage of hierarchical matching steps. The performance measure of accumulation units with various categories are shown in Table 1 performance metrics evaluated through shift based accumulation for multiplication is shown in Table 2.

Table 1: Performance Comparison of Various Adder Units.

<table>
<thead>
<tr>
<th>Adder type</th>
<th>Area (LE’s used)</th>
<th>Fmax (operating frequency)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carry select adder</td>
<td>81</td>
<td>196.39 MHz</td>
</tr>
<tr>
<td>Carry look ahead adder</td>
<td>133</td>
<td>241.95 MHz</td>
</tr>
<tr>
<td>Kogge-stone adder</td>
<td>79</td>
<td>306.0 MHz</td>
</tr>
<tr>
<td>Proposed speculative adder</td>
<td>88</td>
<td>1111.11 MHz</td>
</tr>
</tbody>
</table>

Table 2: State-Of-The-Art Comparison Of Multiplier Units

<table>
<thead>
<tr>
<th>Multiplier type</th>
<th>Area (LE’s used)</th>
<th>Fmax(operating frequency)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vedic</td>
<td>182</td>
<td>239.35 MHz</td>
</tr>
<tr>
<td>Booth radix-8</td>
<td>213</td>
<td>111.99 MHz</td>
</tr>
<tr>
<td>Proposed model</td>
<td>143</td>
<td>737.46 MHz</td>
</tr>
</tbody>
</table>

4. State of the Art Comparison

As this paper is the first attempt to include speculation in the prefix computation for modified carry propagation over traditional definition of carry equations. Though the precise error correction unit considerably reduces the overall performance, than all other methods, proposed method attains high speed with negotiable hardware complexity overhead. Moreover, multiplication through speculative adder exhibits a better quality metrics than adder one. It is incorporated as follows: in speculative computation all the
carries are computed identically and irrelevant to each other, instead in all other parallel prefix computation methods, only 50% of the carries are computed through hierarchical tree based architecture.

Here through exhaustive test bench simulation functionality is verified as shown in Figure 3 and hardware synthesis is carried out using QUARTUS II FPGA synthesizer and its hardware RTL schematic and maximum operating clock speed shown is in Figure 4 and Figure 5. The proposed speculative approach reported with the speed of about more than one time faster than conventional prefix based architecture. Moreover, hardware complexity overhead is also reduced considerably better than the most recent advance prefix implementation.

5. Conclusion

In this paper variable latency speculative addition is proposed for high-speed DSP applications. Hybrid error detection network is incorporated to assert the error signal to minimize the error probability. An extensive MAC unit is proposed using speculative technology shows that proposed MAC unit outperforms all other state-of-the-art multiplication methods. Compared with traditional speculative methods, our method shows sensible improvements in overall latency reduction. The proposed MAC unit preserves all the benefits of high speed arithmetic units, while providing optimized low latency. Hence, high-speed DSP applications can be easily achieved by adopting the proposed adder architecture.

References