Crosstalk noise minimization in novel through silicon via structures

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Abstract

In recent trends, through silicon via (TSV) is essential Technologies for 3-D IC integration because of its short interconnects length and high interconnect density. Beyond the existing structure of TSV, this paper provides a novel structure to investigate the crosstalk effect and same is simulated by using a SPICE simulator and 3-D field solver. The structure of the TSV comprises of copper surrounding by insulating liner, and silicon substrate. In existing structures, silicon dioxide (SiO2) is used as insulating liner because of its material compatibility with silicon substrate. Several researches provide the problem of using SiO2 is due to its high dielectric constant; as a consequence delay will increase. Therefore, SiO2 is not appropriate for high performance applications. In this work, a novel TSV structure is reported to improve the TSV performance which uses poly-propylene polymer liner instead of oxide liner. Signal TSV is enclosed by using a poly-proplylene liner and amid the analysis with doping region is created around the ground TSV. For comparison purposes, conventional and proposed TSV structures are simulated. The proposed TSV’s structure simulation results in 30% decrease in crosstalk over existing TSV structures.

Keywords: Through Silicon via (TSV); Poly-Propylene Liner; Polymer Capacitance; Depletion Capacitance; Crosstalk.

1. Introduction

In recent days, through silicon via (TSV) interconnects are playing a major role in 3-D IC integration. The advantages of TSV interconnects are low power consumption, smaller form factor, better performance, and higher functional density. TSVs are the vertical interconnects used to enable the vertical stacking of Integrated circuit (IC) chips. The structure of the TSV [1] composed of Cu surrounded with insulating liner and silicon substrate. The usage of insulating liner is to avoid the signal leakage from the metal (Cu) to silicon substrate. In the traditional TSV structures, silicon dioxide (SiO2) is used as insulating liner [2] because of its material compatibility with the silicon substrate. SiO2 liner has small thickness which is roughly equivalent to 0.01µm and it has large dielectric constant which is approximately equal to 3.9. Because of high dielectric constant, SiO2 liner develops a large insulating capacitance which impacts on degradation of TSV performance [3]. Hence, SiO2 liner is not appropriate for high performance applications. In addition to that few authors were provided the problems of SiO2 liner. They accounted the problem of deposition of uniform thin layer on the sidewalls of deep reactive ion etching (DRIE) etched vias. Because of the inherent scallops on the sidewalls of TSVs, stress concentration at the scallop edges brings about failure of ultra-thin barrier layers, current spillage and deterioration of electrical performance. To enhance the TSV performance and mitigate the insulating capacitance, low dielectric constant liners are used instead of SiO2 liners. In general, polymer liner has low dielectric constant, elastic modulus and large thickness. Due to the low dielectric constant of polymer, it develops a less insulating capacitance between metal and silicon substrate that results in decreasing of delay. Hence, polymer liners are well appropriate for high performance applications. Additionally, Current spillage is avoided by eliminating the discontinuity of barriers using a large and uniform thickness of polymer liners. Moreover, due to low elastic modulus, polymer liner can also act as a barrier layer in between the silicon substrate and metal to avoid the thermal stresses. In the proposed model, a novel TSV structure is constructed with polypropylene polymer liner as insulating liner.

The TSVs with polymer liners to be fabricated with a completely different method [4] which is contrasting to TSVs with silicon dioxide layers deposited by plasma-enhanced chemical vapor deposition (PECVD). It is possible to fill polymer into a narrow trench using spin-coating or dispensing techniques. Instead of using circular vias hollow-cylinder polymer is completely filled by using annular trenches and coated thin polymer layers. The large and uniform thickness polymer liners surrounding to Cu metal is possible with the annular trench based fabrication. The rest of the paper is organized as follows: The electrical modeling of TSV with analytical equations is reported in section 2. The results and discussions based on the parameter variations of TSV is reported in section 3. Finally, section 4 concludes the work.
2. Electrical modeling of TSV with analytic equations

The proposed TSV structure comprises of three cylindrical signal-ground-signal pattern with height 100 µm and radius 10 µm as shown in Fig. 1. The first and third cylinder is designed with copper surrounded by polypropylene liner thickness 0.1 µm and heavily doped silicon MOS depletion layer width 0.68 µm. The middle cylinder is designed with copper and surrounded by doping layer thickness 0.1 µm. The dielectric constant ($\varepsilon_r$) of polypropylene liner, $\text{SiO}_2$, silicon, copper is 2.3, 3.9, 11.9 and 1.0, respectively.

In this section, analytic RLGC components of the proposed equivalent circuit model of a TSV are proposed and electrically modeled with analytic equations which are functions of material properties, structural parameters, frequency, and etc. The proposed equivalent circuit model Fig. 2 is acquired based on the physical structure of a TSV. Among various TSV parasitic, the capacitance of a TSV is the most vital component which governs the overall electrical behavior of a TSV.

Each of the RLGC components corresponds to a structure of a TSV. The analytic RLGC equations are derived from the physical structure with the design parameters [5], [6]. Therefore, each RLGC equation is a function of the variables from the design parameters. The resistance and inductance of the TSV is analytically modeled as in (1) and (2), respectively.

\[
R_{TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times \left(\frac{d_{TSV}}{2}\right)^2}
\]

(1)

\[
L_{TSV} = \frac{1}{2} \left[ \frac{\mu_0 h_{TSV}}{2\pi} \times h_{TSV} \times \ln \left( \frac{\rho_{TSV}}{TSV} \right) \right]
\]

(2)

Where $h_{TSV}$, $d_{TSV}$, $r_{TSV}$ are the length, diameter, radius of the TSV.

The TSV is surrounded by insulating liner to separate it from the conductive silicon substrate. Due to this insulation layer, there is an insulator capacitance represented by $C_{\text{polymer}}$. The depletion capacitance is also considered in series to the polymer capacitance because the substrate is fully biased to the ground [7], [8]. The polymer capacitance and depletion capacitance can be calculated as

\[
C_{\text{polymer}} = \frac{1}{2} \times 2\pi \times \epsilon_0 \varepsilon_{r,\text{poly}} \times \ln \left( \frac{h_{TSV}}{TSV} \right)
\]

(3)
The metal-silicon contact depends on the metal used for the TSV and silicon substrate dopant density. An ohmic contact and Schottky contact can be formed depends on the doping concentration of silicon. The ohmic contact is a less resistance junction and it can be formed for highly doped silicon. Preferably, the metal-silicon contact resistance must be low. The metal-silicon contact resistance increases, when lower doping concentrations are used. Therefore, the contact resistance needs to be taken into account. The contact resistance and doping region resistance both contribute to give the total resistance.

\[ R_{\text{Total}} = \frac{1}{\pi \varepsilon \sigma_{\text{eq}}} \ln \left( \frac{r_0 + t}{r_0} \right) \]

Since the doping region contains dielectric, it is needed to consider the doping capacitance. It is calculated as

\[ C_{\text{doping}} = \frac{\varepsilon \mu}{\ln \left( 1 + \frac{r}{r_0} \right)} \]

We considered the ground TSV as the reference ground, the unit-length and mutual-inductances of signal TSV can be evaluated as

\[ L_{ij} = \frac{\mu_0}{2\pi} \ln \left( \frac{l}{R_{ij}} \right) (i = j) \]

\[ L_{ij} = \frac{\mu_0}{2\pi} \ln \left( \frac{l}{R_{ij}} \right) \quad (i \neq j) \]

The coupled capacitance and inductance, C12 and G12 between signal TSVs can be obtained from the following 2x2 C and G matrix as

\[ C = \mu_0 \varepsilon_0 \frac{h_{\text{TSV}}}{\varepsilon_{\text{sub}}} L^{-1} \quad G = \mu_0 \sigma_0 \frac{h_{\text{TSV}}}{\varepsilon_{\text{sub}}} L^{-1} \]

Where \( \varepsilon_0 \) and \( \sigma_0 \) are the dielectric constant and conductivity of silicon substrate and \( h_{\text{r}} \) is the TSV height. There is a capacitance and conductance between the signal and ground TSVs because silicon is a semiconductor [9]. \( C_{\text{Si-sub}} \) is expressed as a function of \( d_{\text{TSV}}, p_{\text{TSV}}, \) and \( h_{\text{r}} \). The \( h_{\text{r}} \) term indicates the height where the electric fields are formed between the signal and ground TSVs in the silicon substrate. The relative permittivity of the silicon substrate, \( \varepsilon_{\text{rel}} \) is additionally a variable of \( C_{\text{Si-sub}} \).

\[ C_{\text{Si-Sub}} = \frac{\pi \times \varepsilon_0 \sigma_0}{\cosh^{-1} \left( \frac{p_{\text{TSV}}}{d_{\text{TSV}}} \right)} \times h_{\text{r}} \]

The physical origin of the \( G_{\text{Si-Sub}} \) is the silicon conductivity, \( \sigma_0 \), which is determined by the majority carrier concentration. Therefore, \( G_{\text{Si-Sub}} \) is expressed as

\[ G_{\text{Si-Sub}} = \frac{\pi \times \varepsilon_0 \sigma_0}{\cosh^{-1} \left( \frac{p_{\text{TSV}}}{d_{\text{TSV}}} \right)} \times h_{\text{r}} \]
constant. Due to the reduction in polymer capacitance it leads to decrease in the crosstalk effect. Therefore, the crosstalk in proposed TSV structure is decreased nearly 25% compared to conventional TSV structure.

Similarly, the conventional and proposed TSV structure is validated with \( r_{TSV} \) variation as shown in Fig. 5.

**Fig. 5:** Comparison of Proposed TSV Structure Simulation with the Conventional TSV Structure with \( r_{TSV} \) Variation. (A) \( r_{TSV} = 5 \) µm (B) \( r_{TSV} = 10 \) µm (C) \( r_{TSV} = 20 \) µm.

Impact of changing the radius of TSV (\( r_{TSV} \)) will result in varying of insulating capacitance. Changing of \( r_{TSV} \) will also effect in the depletion capacitance, doping capacitance of signal and ground TSV. In conventional TSV structure, there is depletion capacitance also for ground TSV. On the other hand, doping capacitance for the ground TSV is considered in proposed TSV structure. Compared to depletion capacitance, doping capacitance for ground TSV is negligibly small. Therefore, the crosstalk is reduced in proposed TSV structure. The proposed and conventional TSV structure with \( h_{TSV} \) variation is also validated as shown in Fig. 6.

**Fig. 6:** Comparison of Proposed TSV Structure Simulation with the Conventional TSV Structure with \( h_{TSV} \) Variation. (A) \( h_{TSV} = 100 \) µm (B) \( h_{TSV} = 50 \) µm (C) \( h_{TSV} = 150 \) µm.

Further, it is observed that the TSV parasitic like resistance, inductance, and capacitance are changing with respect to design parameters of TSV like \( h_{TSV} \) and \( r_{TSV} \). For comparison purposes conventional TSV structure is also simulated. For both conventional and proposed TSV structures, variation in resistance and inductance is same. The only varying parameter is capacitance because of difference in dielectric constant of oxide and polypropylene polymer liners.

The capacitance value is gradually decreasing in proposed TSV structure compared to conventional TSV structure is shown in Fig. 7.
In addition to that the proposed TSV structure is simulated with 3-D field solver, HFSS of a soft. Among many design parameters $r_{TSV}$, $h_{TSV}$ and $\rho_{TSV}$ are swept to validate the proposed TSV structure up to 20 GHz. The results obtained with this a soft HFSS simulation tool are shown in Fig. 7.

Fig. 7: Variation In $R$, $L$, $C$ Parasitic with Respect to Design Parameters of TSV (A) Resistance and Inductance with Respect to $H_{TSV}$ for Both Conventional and Proposed TSV Structure (B) Capacitance with Respect to $H_{TSV}$ for Conventional and Proposed TSV Structure (C) Resistance and Inductance with Respect to $R_{TSV}$ for Both Conventional and Proposed TSV Structure (D) Capacitance with Respect to $R_{TSV}$ for Conventional and Proposed TSV Structure.
A novel TSV structure is proposed to investigate crosstalk effect induced in TSVs. The proposed TSV structure that uses polypropylene polymer liner as insulating liner because of its low dielectric constant. This work contribute to analyze the impact of insulating capacitance on crosstalk noise. Impact of changing the parameters like TSV radius, height and oxide liner thickness on insulating capacitance on crosstalk noise. The proposed TSV structure was also simulated by using 3-D field solver and compared with conventional TSV structures. The results indicates that return loss will be less in proposed TSV structure compared to traditional TSV structure. From these simulation results, crosstalk in proposed TSV structure could be decreased nearly equal to 15% and leading to better performance.

References


Fig. 8: Simulation Results of Proposed TSV Structure Using 3-D Field Solver.

From Fig. 8, the crosstalk, return loss, and insertion loss in the proposed TSV structure is presented. Fig. 8(a) & 8(b) shows the crosstalk comparison for both conventional and proposed TSV structure. The crosstalk could be decreased in proposed TSV structure because of poly-propylene polymer liner is used. In the proposed TSV structure, reduction in crosstalk was observed which is nearly equal to 15%. Fig. 8(c) & 8(d) shows the return loss in proposed and conventional TSV structure. The results dedicates that return loss will be less in proposed TSV structure compared to traditional TSV structure. Fig. 8(e) & 8(f) shows the insertion loss in proposed and conventional TSV structures.


