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Research paper



Modelling and Analysis of Novel Topology for Multilevel Inverter With Reduce Number of Switches

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Abstract

The demand of quality power is increasing continuously. The problem of global warming and rate of decrease of non-renewable energy sources are increasing day by day. Hence renewable energy sources such as fuel cell, solar, Magneto hydro Dynamic (MHD), geothermal are the best alternatives to solve the problem of environmental issue and increasing demand of energy. The output of these resources is dc, therefore to connect these resources to the grid, multilevel inverter is the key device. But the output of multilevel inverter has power quality issues such as harmonic generation and notching due to conversion of dc to ac and high number of switch. Hence, this paper deals with harmonic elimination using Genetic Algorithm based Selective Harmonic Elimination (GA-SHE) techniques for asymmetric and symmetric topology of MLI. In the present study, comparative study among the 5-level, 7-level, 9-level, 11-level and 15-level multilevel inverters with reduced number of switches topologies has been discussed. A novel topology of 15-level inverter which consists least number of switches has been designed for a desired voltage level. Also, the comparison of Total harmonic distortion developed in the output voltage generated by different topology at different levels with the proposed 15-level inverter topology are discussed.

Keywords: *Multilevel Inverter(MLI), Selective Harmonic Elimination(SHE),*

1. Introduction

The power quality and the rate of decrease in non-renewable energy sources are the major issues of present time [1]. Therefore, fuel cell, solar energy, Magneto hydro Dynamic (MHD), geothermal are the best alternatives to solve the problem of environmental issue. The flexibility of connecting renewable energy sources with grid is due to multilevel inverter [1]. Now in recent days MLI has drawn large interest in high power industry [2]. The multilevel VSI allows to achieve high voltages with the less harmonics without using series connected synchronized switching devices or transformers [3][4]. Generally multilevel which is used for industrial application are classified as: Diode clamped, Flying capacitor, Cascaded H-bridge. Flying capacitor and diode-clamped inverter suffered from the problem of capacitor voltage balancing and this problem is resolved in cascaded H-bridge inverter [4][5][6][7]. Cascaded H-bridge MLI has a combination of switches with dc sources to create a one cell and then a lot of number of cells are connected in series for increasing voltage level [8]. The cascaded H- bridge multilevel inverter can be classified as symmetric or asymmetric. The asymmetric topologies use the unequal dc voltage sources on the other hand symmetric topologies have equal voltage sources [9]. Number of switches and dc voltage sources required in asymmetric topology is less as compared with symmetric topologies [8]. But main limitation with cascaded H-bridge MLI is the requirement of separate dc voltage sources for every H- bridge [8]. Hence, cascaded H- bridge is bulkier in size and costly. In last few decade, different types of multilevel inverter topologies have been researched. These topologies provide the output voltage with lot of number of switches which leads to higher switching losses and notching. In this paper such type of topologies which had been researched in recent year are discussed. A novel topology which is presented in this paper is simplest and gives high power quality output voltage. This novel topology has less number of switches in comparison with conventional H-bridge and other topologies which are discussed in this paper. This novel topology follows IEEE519 standard according to which the total harmonic distortion of the output voltage is less than 5% [1]. The general optimization technique Genetic algorithm (GA) is used to determine the firing angle of switches of proposed topology.

2. Existing Topologies

2.1 Seven Level Nine Switch MLI Topology

This topology is proposed in [8]. This topology is developed with five switches and 3 dc voltage sources along with one H-bridge having 4 switches which is used for reversal of polarity to generate 3 positives(+ve) and 3 negative(-ve) and one zero-voltage level [10]. This topology is known as sub-multilevel inverter topology. This topology consists of both, bidirectional and unidirectional switches. Bidirectional switch can be designed by connecting two IGBTs back to back with antiparallel diode [6][8]. Various voltage levels can be obtained by adding voltage source and switches. A sub-multilevel inverter cell:
No. of switches driver = $N_{drive,sub}$
No. of switch =$N_{switch,sub}$
No. of IGBT=$N_{IGBT,sub}$
Output level= N_{Level}

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Output levels are calculated as[8]:

$$Nswitch, sub = \begin{cases} 2, & \text{for } n = 1 \\ (n+2), & \text{for } n \geq 2 \end{cases} \quad (1)$$

$$N_{IGBT,sub} = 2n \quad (2)$$

$$N_{Level} = 2mn+1 \quad (3)$$

This topology as shown in Fig.1(a). The switching opertaions for getting desired output voltage level in this topology are shown in Table.1

2.2 Seven Level Eight Switch MLI Topology

This topology is proposed in [11]. This topology is developed with four switches and 3 dc voltage sources along with one H-bridge having 4 switches which is used for reversal of polarity to generate 3 +ve and 3 -ve and one zero -voltage levels [10]. Different voltage levels can be achieved by adding voltage sources and switches [12]. This topology is known as Prior H-bridge cell based MLI. This topology as shown in Fig.1(b). The different switching opertaion for getting seven level output voltage using this topology are shown in Table.2

2.3 Fifteen Level Eighteen Switch MLI Topology

This topology is proposed in [13]. This topology is developed with fourteen switches and seven dc voltage sources having one H-bridge which is having 4 switches which are used for reversal of polarity to generate 7 +ve and 7 -ve and one zero voltage level [8]. This topology as shown in Fig.1(c). Required switching opertaion for getting fiften level output voltage using this topology is shown in Table.3

3. Proposed Topology

Fig.6 represents proposed topology. It is obtained by seven dc voltage sources which may be unequal or equal in value. For equal voltage step, equal voltage sources are used and for unequal voltage step, unequal voltage sources are used [8]. This topology is obtained by unidirectional and bidirectional switches both. This topology consists of bidirectional switches which are required to oppose +ve and -ve voltage when load is inductive in nature.
The desired levels of output voltage from this topology is obtained by this equation,

$$N_{level} = 2n+1 \quad (4)$$

Where, n denotes the number of dc voltage source. The number of switches which is required in this topology except bridge switch can be obtained from the following equation.

$$N_{switch} = n \quad (5)$$

This topology is designed for the 15-level output voltage. The 15-level output is developed with seven switches and seven dc voltage sources having 1-H-bridge which is having 4 switches which are used for reversal of polarity to generate seven +ve and seven -ve and 1 zero-voltage level. This topology as shown in Fig.1(d). The switching opertaion for getting fifteen level output voltage using this topology is shown in Table.4

4. Genatic Algorithm - Selective Harmonic Elimnation

Fig.1(es) shows a stepped voltage waveform generated by a (2N+1) –level inverter, where N is considered as number of voltage sources. The proposed topology is having 7 sources. In this paper 15-level inverter is simulated and analyzed using Fourier series for the harmonic reduction [14].
Proposed multilevel inverter topology is represented as:

$$V_n = \frac{4V_{dc}}{n\pi} \sum_{m=1}^{N} \cos(n\theta_m) \quad (6)$$

Where, N is equal to 7 for 15-level inverter.
Where n= 1,3,5,7,9,11…….
$\mathbf{V_{dcN}}$ is the maximum dc voltage of the multilevel inverter. The firing angles Θ_1, Θ_2, Θ_3, Θ_4, Θ_5, Θ_6, Θ_7 must fulfill the following limits [10].

$$0 < \theta_1 \leq \theta_2 \leq \theta_3 \leq \theta_4 \leq \theta_5 \leq \theta_6 \leq \theta_7 < \frac{\pi}{2} \quad (7)$$

The main objective of selective harmonic elimination techniqueis to find the firing angles Θ_1, Θ_2, Θ_3, Θ_4, Θ_5, Θ_6, Θ_7. So that fundamental component of output is adjusted to desired amplitude and non-triple odd harmonic components can be eliminated. There are no triple order harmonics in 3-phase system. Mathematically, for a 3-phase system with symmetrical topology following set of different order harmonics equations are formulated [14].

$$\sum_{m=1}^{N} \cos(\theta_m) - NM = 0 \quad (8)$$

$$\sum_{m=1}^{N} \cos(5\theta_m) = 0 \quad (9)$$

$$\sum_{m=1}^{N} \cos(7\theta_m) = 0 \quad (10)$$

$$\sum_{m=1}^{N} \cos(11\theta_m) = 0 \quad (11)$$

$$\sum_{m=1}^{N} \cos(13\theta_m) = 0 \quad (12)$$

Where M is known as modulation index which is formulated as:

$$M = \frac{V_1}{4N\frac{V_{dc}}{\pi}} \qquad (0 < M \leq 1) \quad (14)$$

To determine the firing angles, the eq. (8) to eq. (12) are solved by using GA.

4.1 Genetic Algorithm

In the field of Artificial intelligence (AI), Genetic Algorithm is an evolutionary algorithm which can provide an optimized solution of a problem in which objective function may be continuous, discontinuous, Non-linear or stochastic in nature.
First, it selects individual heuristically from the initial population, who act as parents to generate offspring for next generation. A new population is generated after each iteration through crossover and mutation [14]. The process is continuously run till the point they are fulfilled end condition. In this paper, the problem of Selective Harmonic Elimination (SHE) has been solved using Genetic Algorithm. All the lower order harmonic such as 5^{th},7^{th},11^{th},13^{th} are eliminated using GA.

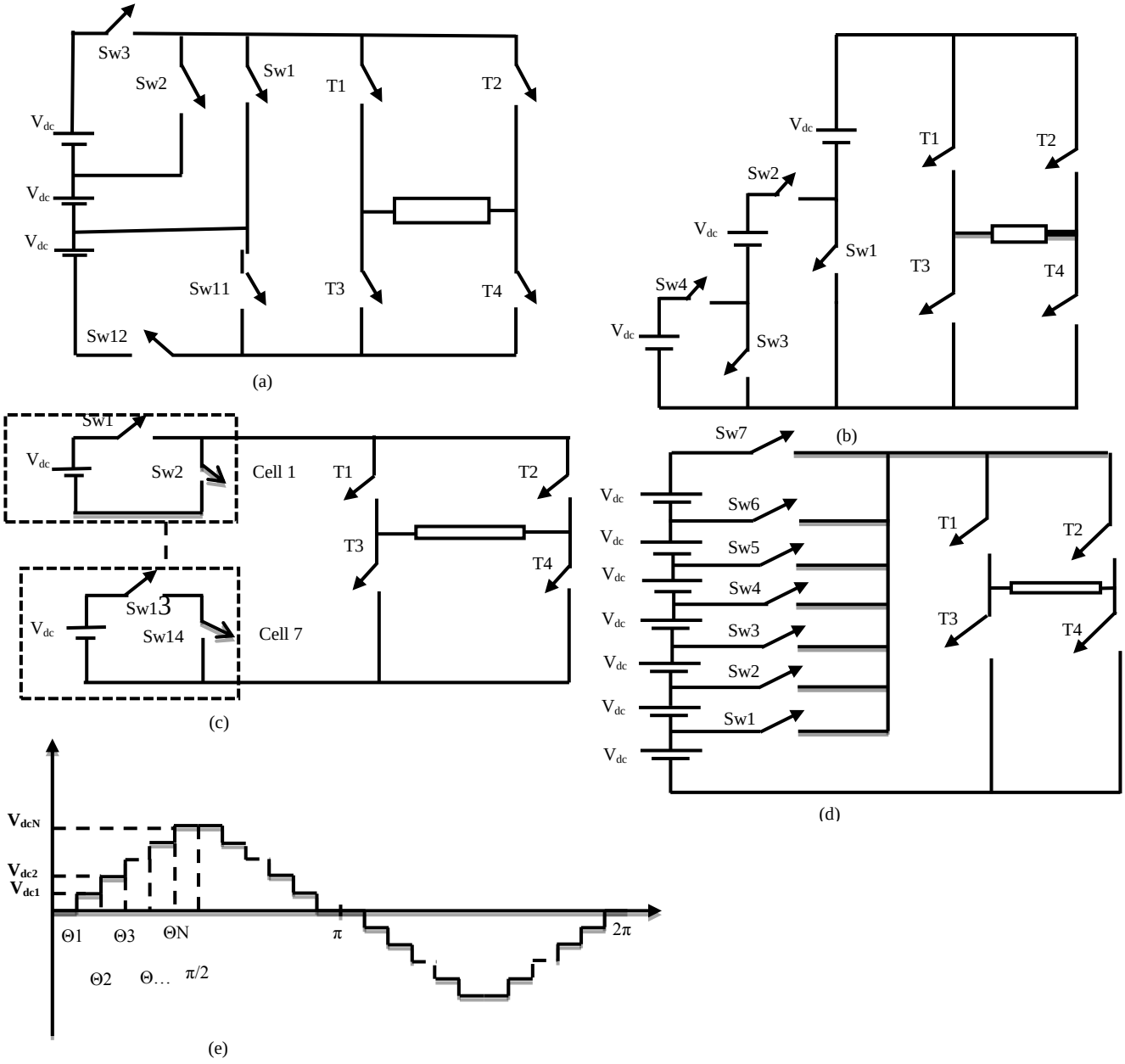


Fig.1: (a) Sub-multilevel Inverter,(b) Prior H-bridge cell MLI, (c) Fifteen Level Eighteen Switch Topology, d) Proposed Topology,(e) (2N+1)-Level Output Voltage Waveform

5. Simulink Model

The simulation and the analogues harmonics analysis for the existing topology and proposed topology are designed in MATLAB/SIMULINK [15].

5.1 Proposed Topology Simulink Model

A novel topology is presented in this paper. Detailed configuration and switching sequence of this topology are explained in section III and Table.6 respectively. A single – phase MATLAB/SIMULINK model of this topology is presented in Fig.2(a). This model consists of seven equal voltage source. This MATLAB/SIMULINK model is design with 11 number of switch. In which four switch used for H-Bridge formation. It is an important point that switches S1- S6 are bidirectional switch [9]. The firing angles Θ_1, Θ_2, Θ_3, Θ_4, Θ_5, Θ_6, Θ_7 for discussed Simulink model are obtained using GA-SHE [1]. The optimal firing angles in radians determined by solving the MATLAB script file at 0.9 modulation index are: Θ_1= 0.126, Θ_2=0.228, Θ_3=0.364, Θ_4=0.484, Θ_5=0.683, Θ_6=0.952, Θ_7=1.095. These optimal firing angles are used to generate the pulses for trigging of switches. This SIMULINK model is developed for symmetrical topology. Various modulation techniques can be used in MLI. Fundamental frequency modulation technique is used in this paper [9].

6. Simulation Result

This section shows the simulation result of the different topologies discussed in section V [17]. The result of proposed topology is obtained from SIMULINK the model which is shown in Fig.2(a). Output voltage and Total Harmonic distortion result is compared with the result of another topology.

Table 1: Output voltage for different states of switchs

State	Sw_1	Sw_{11}	Sw_2	Sw_{12}	Sw_3	T_1, T_4	T_2, T_3	V_L
1	1	1	0	0	0	1	0	0
2	0	1	0	0	0	1	0	$1*V_{dc}$
3	0	0	1	1	0	1	0	$2*V_{dc}$
4	0	0	0	1	1	1	0	$3*V_{dc}$
5	0	1	1	0	0	0	1	$-1*V_{dc}$
6	0	0	1	1	0	0	1	$-2*V_{dc}$
7	0	0	0	1	1	0	1	$-3*V_{dc}$

Table 2: Switches State in PHCMLI

Vout	Switch State							
	T1	T4	T2	T3	Sw1	Sw2	Sw3	Sw4
0	0	0	1	1	0	0	0	0
1*Vdc	0	0	1	1	1	0	0	0
2*Vdc	0	0	1	1	0	1	1	0
3*Vdc	0	0	1	1	0	1	1	0
2*Vdc	0	0	1	1	0	1	1	0
1*Vdc	0	0	1	1	1	0	0	0
0	1	1	0	0	0	0	0	0
-1*Vdc	1	1	0	0	0	0	0	0
-2*Vdc	1	1	0	0	1	1	1	0
-3*Vdc	1	1	0	0	1	1	0	1
-2*Vdc	1	1	0	0	1	1	1	0
-1*Vdc	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table. 3: Switches State in [13]

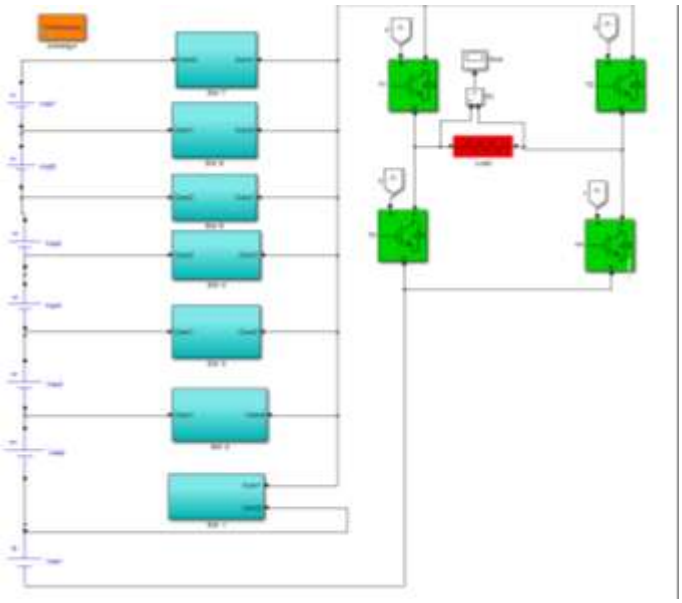
Switch	0	$1*V_{dc}$	$2*V_{dc}$	$3*V_{dc}$	$4*V_{dc}$	$5*V_{dc}$	$6*V_{dc}$	$7*V_{dc}$
SW_1	0	1	1	1	1	1	1	1
SW_2	1	0	0	0	0	0	0	0
SW_3	0	0	1	1	1	1	1	1
SW_4	1	1	0	0	0	0	0	0
SW_5	0	0	0	1	1	1	1	1
SW_6	1	1	1	0	0	0	0	0
SW_7	0	0	0	0	1	1	1	1
SW_8	1	1	1	1	0	0	0	0
SW_9	0	0	0	0	0	1	1	1
SW_{10}	1	1	1	1	1	0	0	0
SW_{11}	0	0	0	0	0	0	1	1
SW_{12}	1	1	1	1	1	1	0	0
SW_{13}	0	0	0	0	0	0	0	1
SW_{14}	1	1	1	1	1	1	1	0

Table. 4: Switches State in Proposed MLI

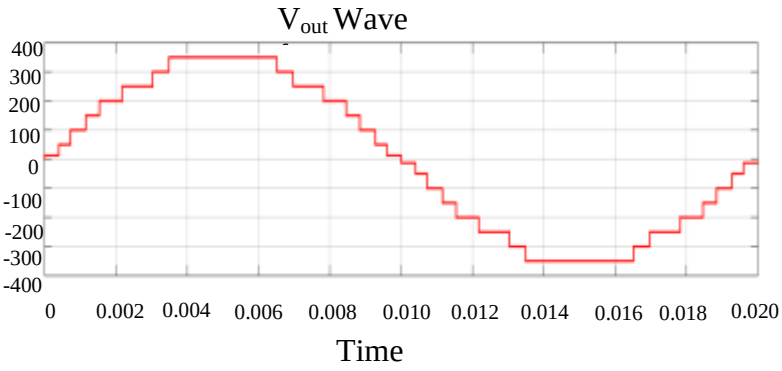
Switch	0	$1*V_{dc}$	$2*V_{dc}$	$3*V_{dc}$	$4*V_{dc}$	$5*V_{dc}$	$6*V_{dc}$	$7*V_{dc}$
SW_1	0	1	0	0	0	0	0	0
SW_2	0	0	1	0	0	0	0	0
SW_3	0	0	0	1	0	0	0	0
SW_4	0	0	0	0	1	0	0	0
SW_5	0	0	0	0	0	1	0	0
SW_6	0	0	0	0	0	0	1	0
SW_7	0	0	0	0	0	0	0	1

6.1 Proposed Topology Simulink Result

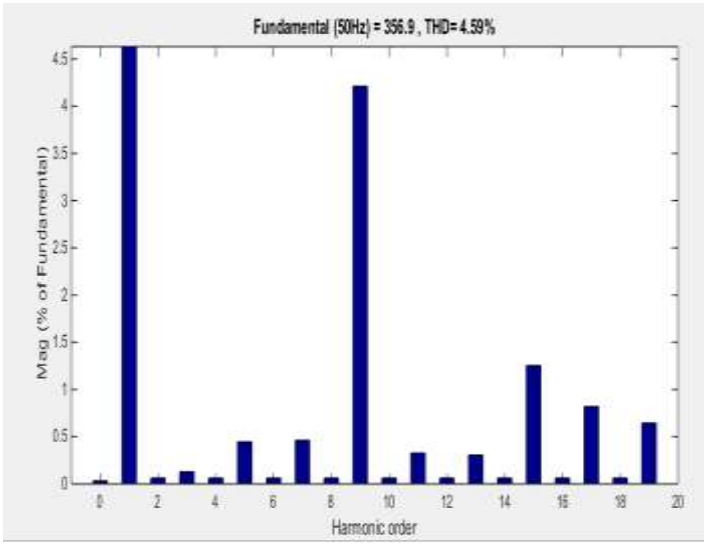
The results of proposed topology is obtained by GA-SHE algorithm in SIMULINK model. In the proposed topology the optimal firing angles are determined by MATLAB script file at 0.9 modulation index, Ɵ 1 = 0.126, Ɵ 2 =0.228, Ɵ 3 =0.364, Ɵ 4 =0.484, Ɵ 5 =0.683, Ɵ 6 =0.952, Ɵ 7 =1.095. Fig.2(b) shows the waveform of single phase output voltage of the proposed topology. MATLAB Fast Fourier Transform(FFT) tool box is used for calculate the harmonic spectrum of proposed topology. Total harmonic distortion(THD) in proposed topology is shown in Fig.2(c). 4.59% Total harmonic distortion(THD) is found in proposed topology is found 4.59% which is very less as compared to other discussed topology.



(a)



(b)



(c)

Fig.2:. (a) Simulink Model of Proposed Topology (b) Single Phase Voltage of Proposed Topology (c) Phase Voltage THD in Proposed Topology

7. Comparision Between Different Topology

Table.5 gives the comparison between proposed topology and existing topologies on the behalf of THD, Number of switch, Methodology and switching frequency.

Table 5: Comparison of Power Quality Improve

Ref. No	Level	No. of Switch	THD %	Lower Order Harmonics %			Methodology	Switching Frequency
				3^{rd}	5^{th}	7^{th}		
[21]	5	8	9.79	-	-	-	Soft Switching	Low
[16]	5	15	9.32	0.02	3.97	2.29	Fundamental SHE	Low
[8]	7	9	7.84	-	0.15	0.27	SHE	High
[8]	7	9	8.84	-	5.20	0.77	NLC	High
[22]	7	12	17.97	-	-	-	Soft Switching	Low
[11]	7	8	<5	-	-	-	PWM	High
[25]	7	12	6.21	-	-	-	GA-MTHD	High
[20]	11	11	9.07	-	-	-	PWM	High
[23]	9	16	15.2	0.452	0.767	1.289	TPWM	High
[23]	9	16	12.94	0.295	0.400	1.381	SPWM	High
[12]	15	12	7.25	-	-	-	Fundamental SHE	Low
[9]	15	12	7.6	-	-	-	Fundamental SHE	Low
[20]	15	14	6.80				PWM	High
[24]	15	18	6.31	-	-	-	SPWM	High
Proposed	15	11	4.59	0.13	0.45	0.46	GA-SHE	Low

8. Conclusion

This study proposes the MATLAB/SIMULINK design of a single phase fifteen level inverter with a novel topology. The proposed topology consists of less number of switch. For a 15-level MLI, proposed topology has only 11- switch compare to other topology discussed in [8], [11], [12], [9], [13], [19], [20] which used 13,16,12,12,16,16,14 switches. T_{on} (switch ON time) is less in this topology. Due to this, switching losses are reduced. Also the switching frequency is less thus the notching problem is overcome by this topology. SHE technique has been used for the removal of the lower order harmonics. This paper highlights that the THD in given topology is 4.85% (≤5%) according to the IEEE519 standard with the help of GA-SHE technique [18]. Hence GA-SHE technique gives better results. With the help of this inverter high quality power can be obtained.

Base on the observations, the proposed topology provides a lot of number of advantage such as: reduced THD, minimum computational complexity, simple design and less cost.

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