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***Research paper***



# Low Power and Low Area Junction-less Tunnel FET Design

**U Ragavendran & M Ramachandran**

MPSTME, NMIMS (Deemed to be University), India 425 405.
**Corresponding author E-mail :druragavendran@gmail.com*

**Abstract**

We present Junction less Tunnel FET with Si:SiGe, Si:AlGaAs and Si:InGaAsP and investigate their DC characteristics. The proposed structures present tremendous performance at a very low supply voltage. The key idea is to study device performance, which can be exploited as a digital switching device for 22 nm technology. Comparison of different heterostructures numerical simulations indicates that ION increases from 0.0024345 to 0.006532 A/μm, when Si:SiGe is replaced with Si:InGaAsP for 22nm channel with supply voltage of 0.5V at a temperature of 300K.

*Keyword: TFET, Flip-flop, Low power design, low-power integrated circuits; Junctionless FET*

## 1. Introduction

MOSFET have been first designed in the year 1933 by J.E.Lilienfeld and since then they have been undergoing constant scaling and optimization in accordance to the Moore's Law. Today, the researches on MOSFET devices have reached to an edge beyond which the switching mechanism need to be changed to achieve an efficient structure with the desirable transistor characteristics and optimized output. The Tunnel Field Effect transistor (TFET) is a type of transistor that uses Quantum Tunneling for transistor switching purposes [11]. It is a promising candidate with faster switching speed, low powered, energy efficient, lower threshold voltage and low leakage current [3]. The major shortcoming of TFET is the low ON current, which is lower than MOSFET causing hindrance in commercialization of TFETs at a wider scale. Though, TFET in today's world finds its applications in ultra-low power switching application which can be implemented. It needs modifications in its structure to increase the value of on current, so that it can replace the use of MOSFET. The Junctionless TFET works on the principle of charge plasma effect and quantum tunneling. The charge plasma effect is created at the source; this generates of the charge carriers (Electrons) then help in the flow of current [2]. The electrons then tunnel through the valence band of the source to the conduction band of the channel by the quantum tunneling. Due to the absence of metallurgical junction in junctionless FET there is lesser amount of blockage caused in the tunneling process increasing the tunneling probability across the tunneling barrier [1]. When we supply the control gate voltage the channel gets induced with negative charge and acts as n+ region that easily conducts the electrons that enable further flow of current through the device. The heterostructure helps in increasing the ratio of ON versus OFF current by reducing in the length of the potential barrier. Whereas the homostructure has higher ON current due to the constant vibrations that occur at the band gap, since at the tunneling barrier due to the use of the same material the vibrations remain synchronized, the number of electrons passing through the barrier increases thereby increase in the ON as well as OFF current[1].

## 2. Device Structure

The heterostructure JLTFET consists no doping junction but two different material at the source and channel-drain, with no metallurgical junction between them. The homostructure JLTFET consists of single material throughout the source- channel-drain region with no change in doping concentration. The device has two gates named control gate and the auxiliary gate. The control gate is used to control the channel and the auxiliary gate voltage is used to control the number of charge carriers formed at the source by the charge plasma effect. The structure consists of double gate, that is has gates on either side of the channel and the source respectively. The contacts are given at the source end, drain end, at the control gates and the auxiliary gates. The doping concentration is $1\times10^{19}$ $cm^{-3}$ throughout the source-channel-drain. The hafnium dioxide is used as the gate oxide and silicon dioxide has been used as spacer between the control and the auxiliary gate. The gate metal used at the control gate is aluminum (Work function=4.2 eV) and the auxiliary gate used is the platinum (Work function = 5.2eV).The same structure is then used with same material on source as well as the drain side. The structure thereby formed is known as homostructure JLTFET.

### 2.1 Hetero-Structure JLTFET

The Si:SiGe Heterostructure JLTFET consists of SiGe as source and Silicon as the drain. Similarly we compare this base structure with several other structures such as Si:AlGaAs and Si:InGaAsP in which the source is of AlGaAs and InGaAsP respectively and the drain is of siliconmaterial.

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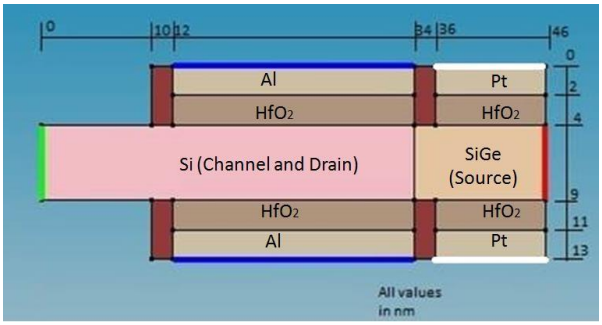



**Figure 1**: Si:SiGe Heterostructure JLTFET

**Table** 1: Parameters

| Parameters | Values |
|---|---|
| Source/channel/drain doping (N) | $1x10^{19}$ $cm^{-3}$ |
| Effective Oxide Thickness($T_{ox}$) | 2 nm |
| Control gate work function(Al) | 4.2 eV |
| Auxiliary gate work function (Pt) | 5.3 eV |
| Gate Length(L) | 22 nm |
| Channel thickness(T) | 5 nm |
| Supply voltage ($V_{dd}$) | 1V |
| Dielectric Constant of Spacer ($SiO_2$) | 3.9 |
| Dielectric Constant of Gate Dielectric ($HfO_2$) | 25 |

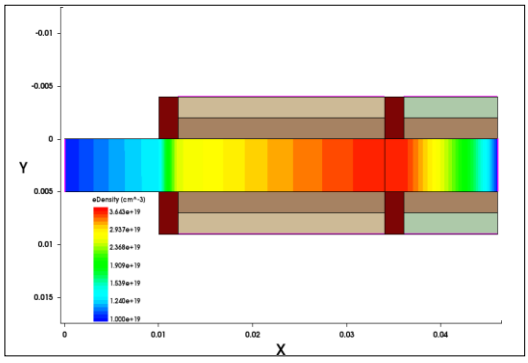
### 2.2 Homostructure JLTFET

The homostructure JLTFET is formed using single material in the source as well as in the drain. We have used Silicon, SiGe, AlGaAs and InGaAsP to check their corresponding performances with respect to heterostructure JLTFET.

## 3. Simulation and Result

The 2-Dimensional structure has been simulated using Synopsis Senators. Since in the TFET structure the tunneling current flow depends on the band structure of the materials, Band to band tunneling model has been implemented. Shockley-Read-Hall is used to model traps and defects. Trap Assist tunneling model is used to account for the electron tunneling through the band gap via trap states. Since, the channel is heavily doped the Band Gap narrowing model has been used.

### 3.1 Electron Density of Si:SiGe Heterostucture JLTFET




**In Figure 2**: Electron Density

above structure electron density is highest at intrinsic region and the interface of source-channel which is due to the fact that tunneling takes place at this interface hence an accumulation of electrons. It's higher at source side than drain because electrons are being injected from source that results in higher electron density. Among Hetero-structure JLTFET models shows overall better results with higher $I_{ON}$, optimally lower $I_{OFF}$, lower threshold voltage and higher value of trans- conductance

### 3.2 Comparison between Heterostructure JLTFET

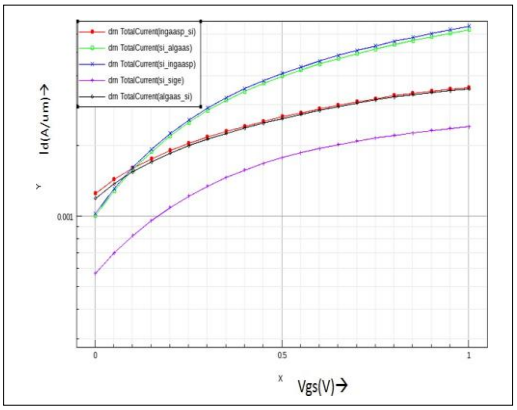



**Figure** 2: Comparison between all the heterostucture JLTFET

### 3.3 Comparison between Heterostructure and Homo-structure JLTFET

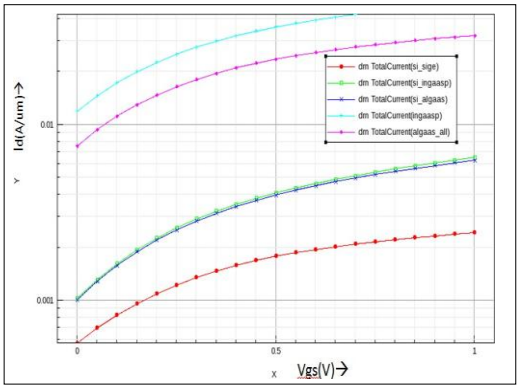



**Figure** 3: Comparision between all the heterostucture and homostructure JLTFET

On comparing Hetero-structure JLTFET models with that of Homo-structure JLTFET models, the homo-structure models show higher Ion but this gain is offset by higher Ioff giving a lower Ion/Ioff ratio than hetero-structure models and a higher threshold voltage than hetero-structure models , thus making case for H-JLTFET models.

## 4. Conclusion

We conducted simulations of Heterostructure-JLTFET using various materials namely Si, SiGe, AlGaAs and InGaAsP. For the experiment we varied drain voltage, control gate voltage and auxiliary gate voltage, also in order to form an experimental basis for comparison we performed simulations with Homostructure-JLTFET of above mentioned materials. Simulations showed that an increase in auxiliary gate voltage although leading to an increase in ON current also increases OFF current making a case for optimally lower auxiliary gate voltage. Materials with higher band-gap energy show higher ON current and better device parameters including lower threshold voltage. The models showed strong current and good even at low voltages i.e., 0.5V. Comparing with output data of Homostructure-JLTFET, Heterostructure -JLTFET shows optimized output which is far ahead in performance. We can conclude that H-JLTTFET with exceptional results for small geometric size exhibits tremendous possibilities for low power applications.

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