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Research Paper

Frequency Domain based Digital Down Conversion Architecture for Software Defined Radio and Cognitive Radio

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Abstract

This paper presents a sampling rate digital down converter that is totally based on frequency domain processing. The proposed DDC is targeted for Software Defined Radio and Cognitive Radio architectures. The proposed architecture is based on replacement of the complex multiplication with direct rotation of the spectrum. Different aspects of frequency domain filtering are also discussed. The Xilinx Virtex-6 family FPGA, XC6VLX240T is used for the implementation and synthesis of the proposed FFT-IFFT based architecture. The overlapping in time domain at the output of the IFFT block is avoided using overlap and add method. In terms area, highly optimized implementation is observed in the proposed architecture when compared to the conventional DDC. The synthesis results have shown that the developed core works at a maximum clock rate of 250 MHz and at the same time occupies only 10% of the slices of FPGA.

Keywords: *Frequency Domain Filtering, Digital down conversion (DDC), Sample rate conversion*

1. Introduction

A digital down conversion architecture that is totally based on frequency domain processing is explained in this paper. The DDC designed is suitable for non-cooperative communication systems like military applications. The principle of frequency domain filtering is well established in the literature, [1]-[5] being few samples. But the implementation of DDC using frequency-domain filtering requires few additional blocks which are explored in this work.

The SDR based receivers that are designed to be used in signal intelligence products of military applications requires monitoring of the whole spectrum and dynamic tuning. Such applications require very complex DDC architectures with the following capabilities:

- Must be able to process higher decimation factors (up to 1000).
- Real-time response is required.
- Multi-channel capability is required.
- Must be able to handle simultaneous signals that are spectrally located apart.
- The designed DDC must support the SDR receiver to have a minimized ratio of signal detection time and monitoring time, so that the LPI signals can be captured.
- In order to have portable SDR receivers, the DDC must be realized in such a way that it is suitable for smaller FPGAs.

At present, ICs such as GC4016/5016 kind of basic DDC chips are available in the market that are mainly designed for GSM/CDMA mobiles/base stations. The use of such ICs in the non-cooperative communication systems limits the capability of the whole receivers due to the SRC limitations. The proposed FFT-IFFT based DDC architecture is designed addressing all the above-mentioned problems.

2. Frequency-domain DDC:

2.1. Signal monitoring receiver:

The main aim of the SDR receivers used in non-cooperative systems is to intercept the unknown signals and analyze them. The block diagram of one such signal monitoring receiver is given in fig(1).

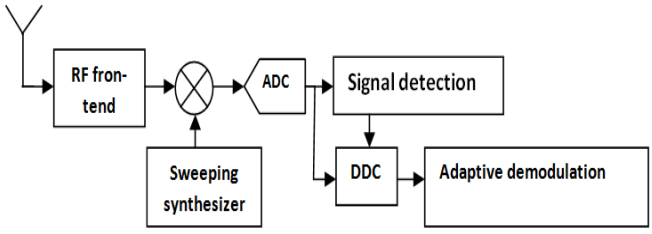


Fig. 1: Signal monitoring receiver architecture

A set of wideband antennas are used for receiving the signals from the entire frequency band. The RF front-end provides required gain and filtering. The technique of superheterodyne receiver is used for frequency conversion of the signal from the band of interest to fixed IF, generated by the sweeping synthesizer. The sweeping synthesizer is named so as it sweeps the whole spectrum of interest in phases of IF bandwidth.

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Suitable ADC with high dynamic range is used next to digitize the signal after IF stage. The rest of the signal processing is realized digitally. The DDC block carries out both frequency shifting and digital down conversion. The signal detection block is used to detect the spectrum peaks and separate the friendly signals from threat signals. Based on the characteristics of the signal detected, like type of modulation, coding, Bandwidth, source/channel coding, the adaptive demodulation block processes the signal.

2.2 Motivation for frequency-domain approach of sampling rate conversion:

The basic idea of frequency-domain based sample rate conversion is explained in [6]. This concept is extended and multi-channel DDC with low area and complete dynamic tuning is proposed in this work. The block diagram of a typical DDC is shown in fig(2).

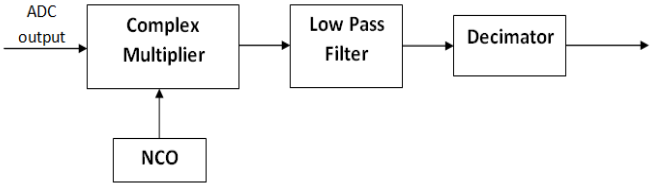


Fig.2: Block Diagram of DDC

The frequency given by the complex digital oscillator, NCO, is decided by the signal detection block. The complex multiplication shifts the signal in the frequency domain, which is accomplished by direct spectrum rotation as shown in fig(3).

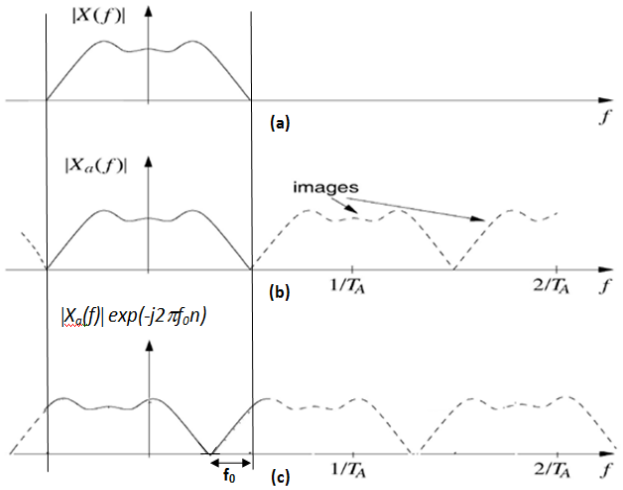


Fig.3: Complex multiplication of the sampled spectrum

Fig(3a) shows the spectrum X(f) of the signal x(t) which is digitized. Fig(3b) gives the spectrum $X_a(f)$ of the sampled digital signal x[n]. the images of X(f) is observed in this figure, which is the result of sampling. Fig(3c) shows the effect on the spectrum after complex multiplication with the negative exponential.

$$X_c(f) = X_a(f)\, e^{-j2\pi f_0 n}$$

It is observed from the fig(3c) that the effect of multiplication can be obtained by just shifting the spectrum to left by f_0, thus avoiding the realization of the complex oscillator that occupies more area on FPGA. Similarly, complex multiplication with positive exponential can be obtained by rotating the entire spectrum to the right.

2.3 Filtering in the frequency-domain:

Filters are used in sample rate converters in order to avoid either imaging (in the case of interpolation) or aliasing (in the case of decimation). Generally, FIR filters, realized with polyphase structures, are used for SDR based SRCs. The input signal in this case is convolved with filter coefficients, followed by sampling rate conversion. The same result can be obtained by multiplying the input signal with the filter coefficients in frequency domain. The IFT of the resultant product gives the output signal in time-domain.

As FFT reduces the computational complexity of DFT from an order of N^2 to an order of $(N.\log_2(N))$, the FFT based architectures are often desirable to perform the processing of digital signals. Several architectures are available in the literature [7]-[13], that provides low area and high speed implementation of the FFT-based architectures. Also, the computational cost of implementing FFT and IFFT on FPGAs is lesser when compared to the conventional methods. Hence an FFT-IFFT based architecture is proposed in this work, which performs the filtering in frequency-domain.

The DFT of a sequence x[n] is nothing but the sampled version of the Fourier Transform of the corresponding continuous signal x(t). Hence multiplication of the DFTs of the input signal and filter coefficients corresponds to the circular convolution, which can be responsible for time-domain aliasing. In order to avoid this time-domain aliasing, linear convolution must be performed, for which it must be ensured that the signal is time-limited. The effect of linear convolution can be obtained from circular convolution by performing overlap-add method, as explained in [14]-[16].

2.4 Linear convolution from circular convolution using overlap-add method:

Consider a signal x[n] with finite length L and a unit impulse response h[n] of length P. The length of the result of linear convolution of both signals, h[n] ⊗ x[n], is L+P-1. In order to avoid aliasing in the time-domain, both the signals have to be zero-padded at least to a length of L+P-1. Then FFT must be performed on both the sequences, followed by the multiplication of the transforms, further followed by IFFT, giving a result of length L+P-1.

In the present architecture, the input signal is of an arbitrarily long length, streamed from the ADC output. The filter in this case has to run 'on the fly'. This can be done by windowing the signal into consecutive blocks, each of length L. The overlap-add algorithm is then performed as follows:

- Pad P-1 zeros to the input signal, x[n] of length L, to obtain a length of L+P-1.
- Pad L-1 zeros to the sample response, h[n] of length P, to obtain a length of L+P-1.
- Perform FFT on both signals.
- Multiply the FFT outputs bin by bin.
- IFFT is implemented on the multiplied output, giving back the time-domain signal.
- As the last P-1 samples of the output overlap with the starting samples of the next block, the overlapping samples should be added in order to get a proper response.

Hence the algorithm is named as overlap-add method.

3. Proposed DDC architecture:

The block diagram of the proposed architecture of DDC implementation in frequency-domain is shown in fig(4).

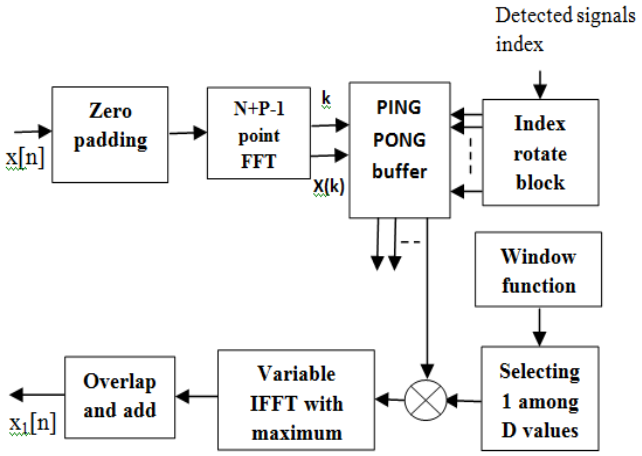


Fig.4: Proposed DDC architecture

Assume that x[n] is the input signal with length N. (P-1) zeros are padded first, followed by (N+P-1) point FFT. For simplicity, the length of the filter is assumed to be N+1 (i.e. P=N+1). The size of FFT now is 2N (N+(N+1)-1). The 2N point FFT is given by the following expression.

$$X[k] = \sum_{n=0}^{2N-1} x[n] e^{-j\frac{2\pi nk}{2N}}$$

The FFT output is next stored in PING-PONG buffer, which is a dual buffer memory. The PING memory block is used to store the output of the FFT, while the PONG memory block is used to read the output of the FFT with necessary shifts, based on the frequency of the detected signal.

The dual buffer system is essential as the reading of the FFT output may start at any address location based on the required FFT rotate-index value, k_i , which is decided by the detected signal's index. Thus the required frequency-shift takes place in the PING-PONG buffer. The output of this buffer is the shifted signal, thus accomplishing the task of complex multiplication.

The FFT rotate-index, k_i , is obtained by changing the value of the address offset, followed by modulo-2N addition with index 'k' of the FFT output as given in the following expression.

$$k_i = MOD_SUM(k + Detected_k_i)$$

The value of k_i thus obtained is used to read the FFT output from the PING-PONG buffer.

The filtering can be done using any one of the windowing techniques in the frequency-domain, the result of which is similar to window-based design of FIR filters. Rectangular window is selected in this case as it consumes less area, because the multiplication is either with 0 or with 1. Let $X_i(k)$ be the output of the i^{th}-channel after required rotation.

This output is multiplied with the window function, resulting in $X_{if}(k)$, given by

$$X_{if}[k] = X_i[k].W[k]$$

The required decimation factor D, given by the signal detection block, is obtained by selecting (2N/D) bins around the zero frequency FFT bin (mid FFT bin). These FFT bins are next streamed into the IFFT core, to obtain IFFT with the length (2N/D).

The output of the IFFT block gives (2N/D) time-domain samples. The overlap-add algorithm is next performed on these samples, resulting in $x_1[n]$, which consists of (N/D) time-domain samples. It is observed that for each set of N-input samples, (N/D)-output samples are obtained, thus resulting in decimation by a factor D.

4. Simulation Results

4.1 Functional verification of the proposed DDC:

The functional verification of the designed architecture is first done in MATLAB, the final output of which is given in fig(5) for a decimation factor of 5.

4.2 Simulation results of the proposed DDC:

The proposed DDC architecture is simulated and synthesized for Virtex-6 family XC6VLX240T FPGA. The architecture is also simulated using ModelSim10.4a simulator, the screen shots of which are given in this section.

The overall decimated outputs of the proposed DDC, in comparison with the input signals are given in fig(6a) in the literal form and fig(6b) in the waveform form, for a decimation factor of 8.

The decimated outputs for a decimation factor of 64 are given in fig(7a) and fig(7b).

4.3 Power and Area Comparisons

The dynamic power comparison between the proposed DDC and typical CIC and polyphase decimators are shown in fig(8). The power calculations are done using the Xilinx14.7 Xpower tool box.

It can be observed from fig(8) that the dynamic power of the proposed DDC is less than that of the polyphase decimator, but more than that of the CIC decimator. The reason being that the CIC implementation is completely multiplier less. But the spectral response of the CIC implementation is poor which has to be compensated using an FIR filter, thus increasing the power and area. CIC decimators are mostly used for high sampling rates and ASICs, whose hardware implementation is fixed.

Fig(9) gives the comparison of the area occupied by the proposed DDC with the polyphase and CIC decimators. Though the number of register, LUT and RAM/FIFO slices taken by the proposed DDC is more than that of the other two counter parts, it can be observed that the number of DSP slices are less due to the reduced MAC operations in frequency domain processing of DDC.

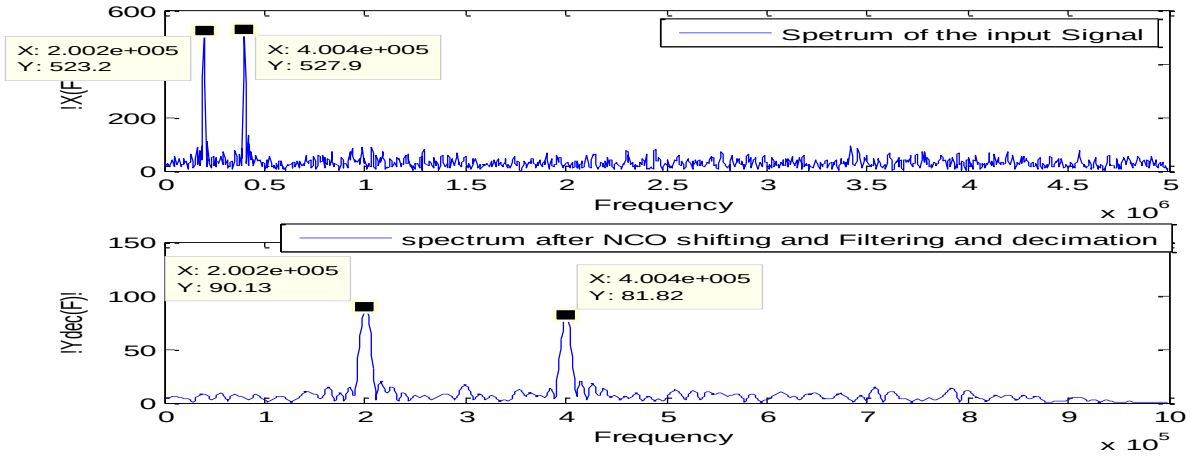


Fig. 5: MATLAB output of DDC

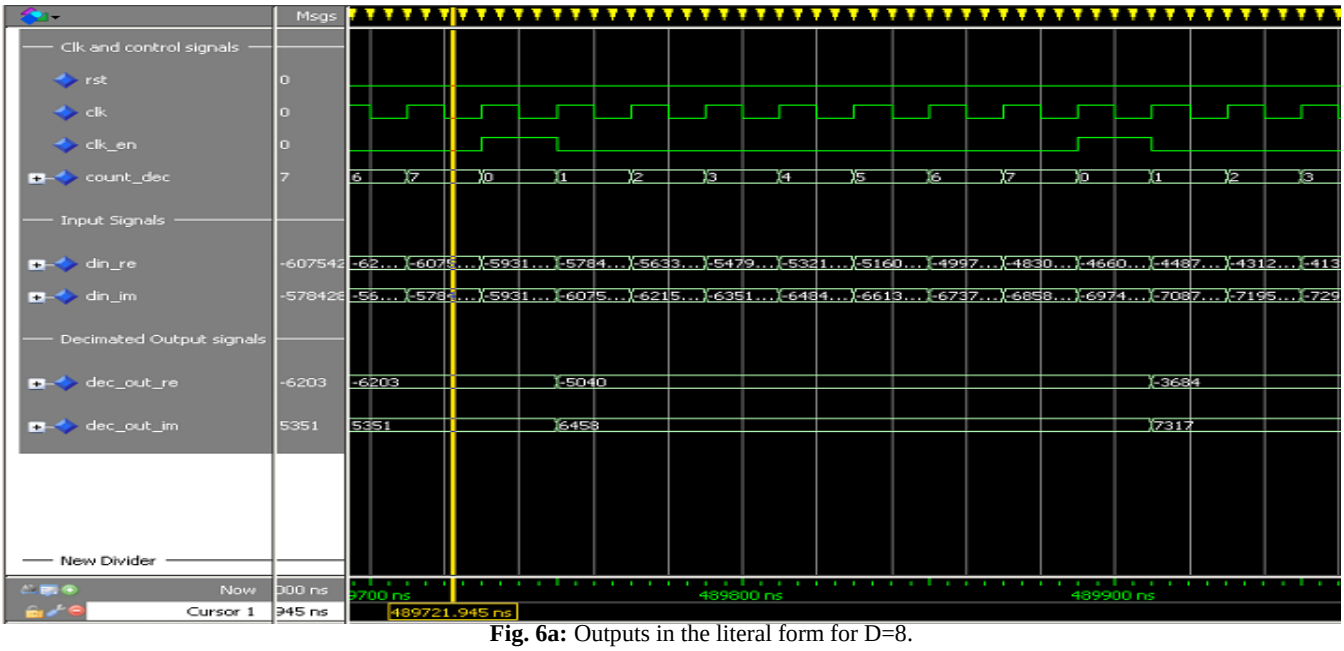


Fig. 6a: Outputs in the literal form for D=8.

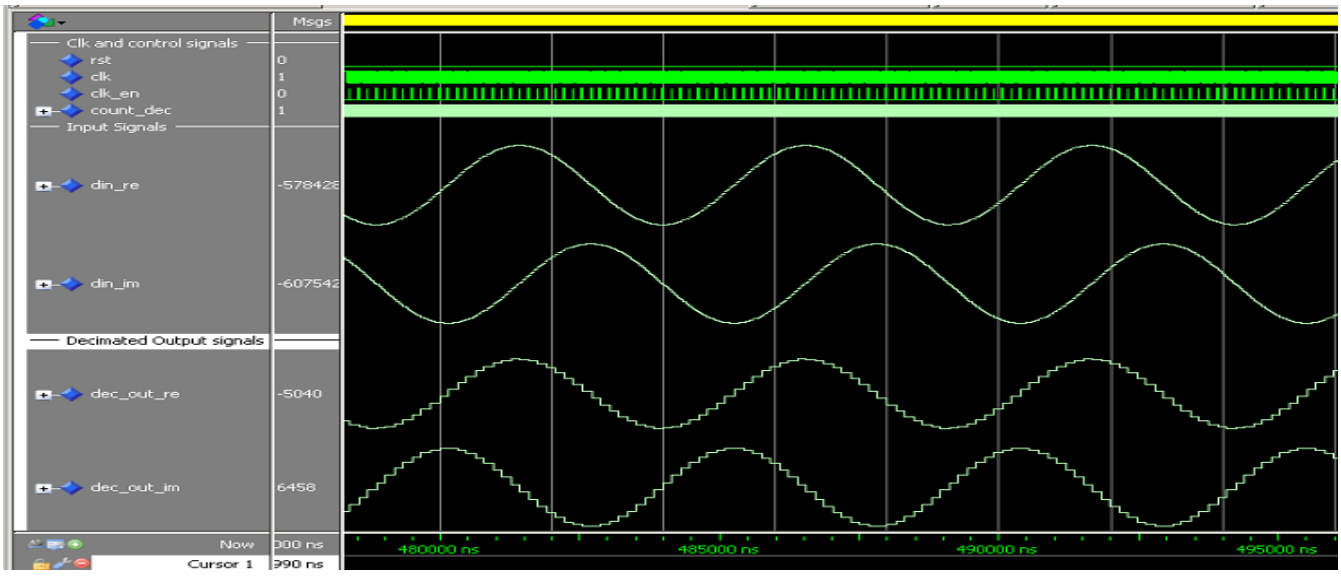


Fig. 6b : Outputs in the waveform mode for D=8.

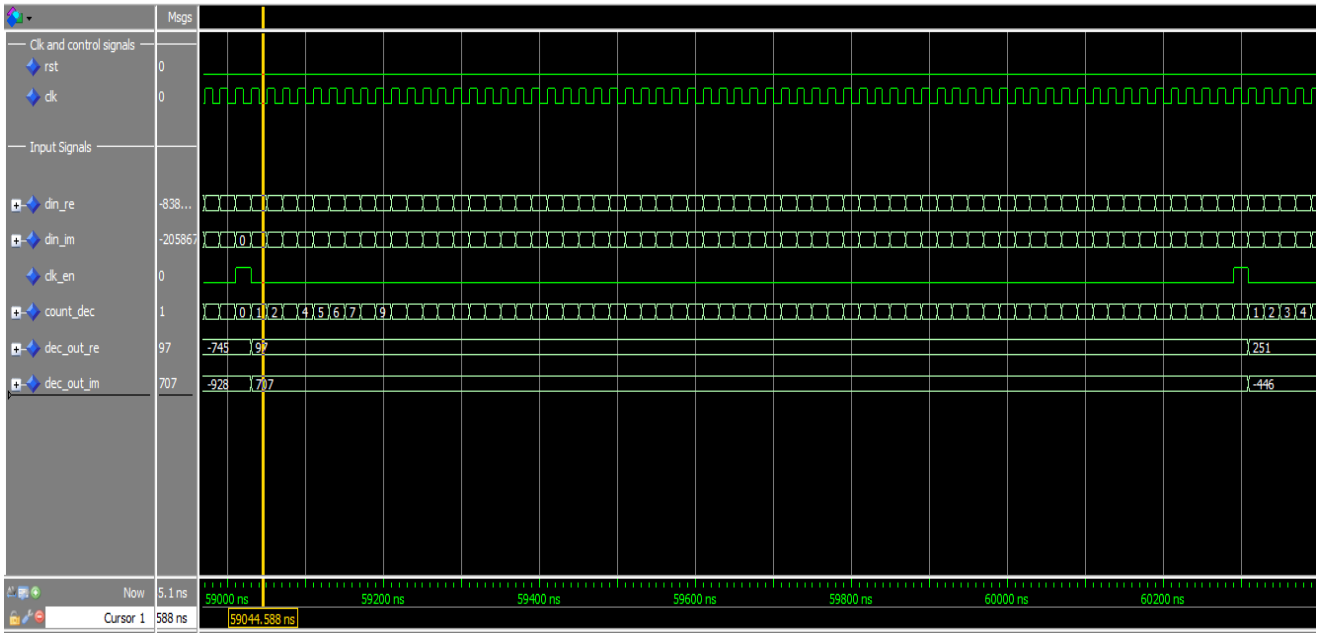


Fig.7a: Outputs in the literal form for D=64.

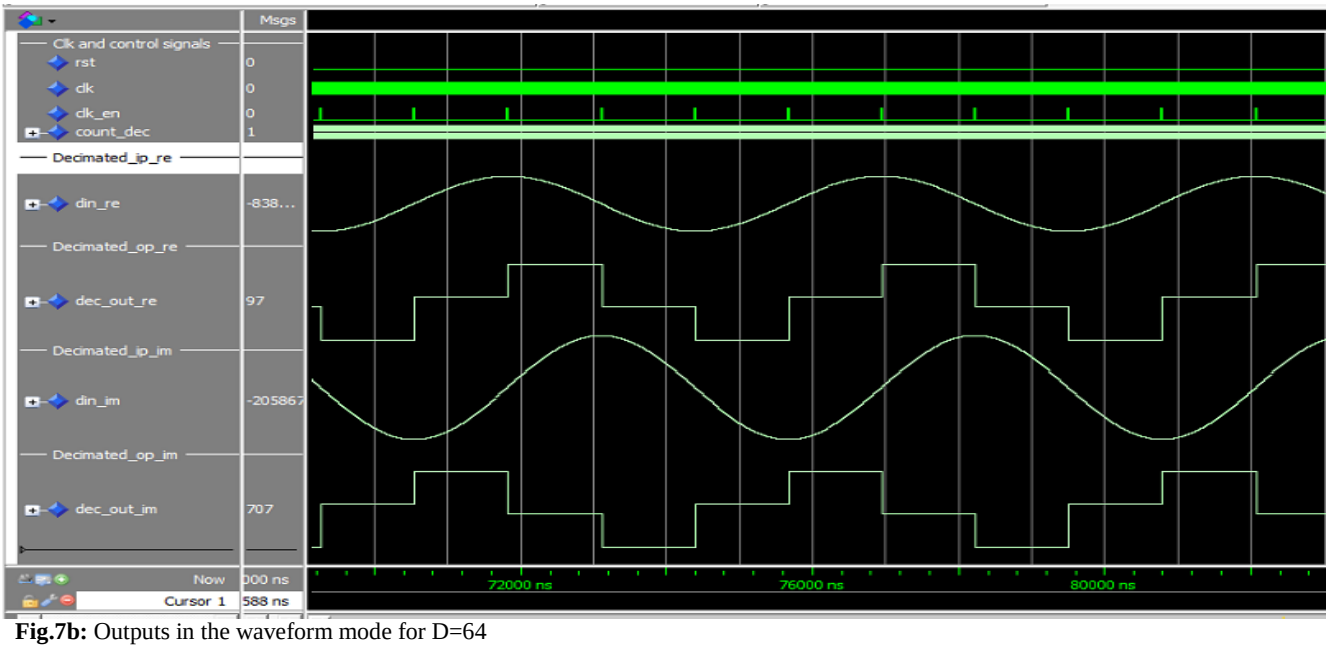


Fig.7b: Outputs in the waveform mode for D=64

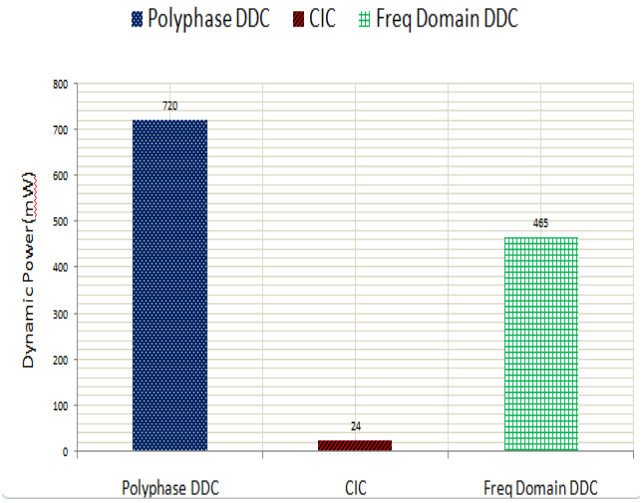


Fig. 8: Dynamic Power Comparison of the proposed DDC with polyphase and CIC architectures.

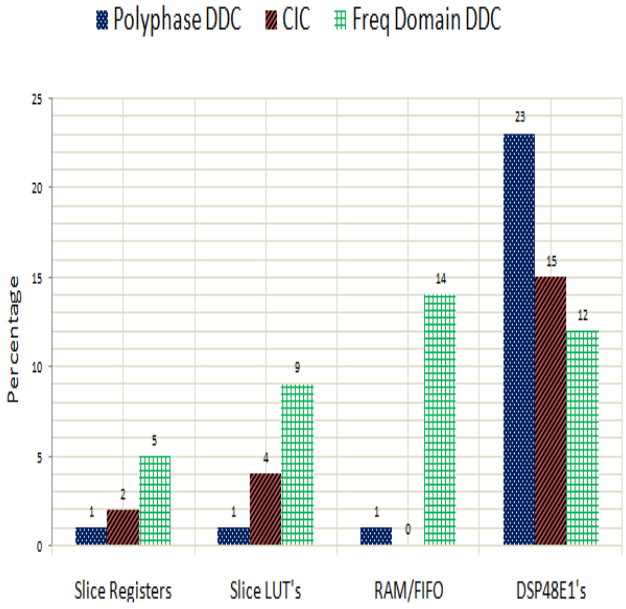


Fig.9: Area comparison of the proposed DDC with polyphase and CIC architectures

5. Conclusion

The work presented in this paper proposed a complete frequency-domain implementation of DDC, suitable for FPGA based SDRs with dynamically varying decimation factor and multi-channel support. The synthesis report (on Virtex-6 family) of the proposed architecture shows an occupancy of just 10% of the slices and an operating frequency of 285MHz.

Performance-wise, the 2N-point FFT used in the architecture is as good as the 2N-tap FIR filter. But the area required in the latter case is more when compared to the former. The DDS block, which is used for complex multiplication, is not required in the architecture as the same task is accomplished by frequency shifting. Thus resulting in further reduction of the area, as shown by the results.

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