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Research paper

An Improved Hybrid PWM Technique for DC Capacitors Voltage Balance of Five Level DCMLI

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Abstract

The innate problem with five-level Diode Clamped Multi Level Inverter (DCMLI) is imbalance in supply DC capacitor voltages. This paper presents a novel Hybrid Pulse Width Modulation (PWM) technique to stabilize the capacitor voltages. The unbalance in capacitor voltages leads to decrement in inverter level, increase in switching stress and distortion in the output voltage. The existing solutions to this problem use either a back to back connection of inverter and rectifier or external dc sources for each capacitor, but there isn't a solution which would inherently balance the capacitor voltages of five levels and above for DCMLI. To rectify this problem a novel hybrid PWM technique which is combination of Carrier based PWM (CBPWM) and Space Vector Modulation (SVM) is proposed. As per this technique conventional CBPWM is applied to meet the load demand and SVM is applied at certain selective intervals to balance the capacitors. The novelty lies in selection of appropriate switching state and the interval at which it must be applied to balance the capacitor voltages. This technique is simple to implement and gives rise to less switching losses.

Keywords: *Capacitor balance; DCMLI; Five-level; High power Drives; Space vector PWM; Switching Stress*

1. Introduction

A Multi-Level Inverter (MLI) is a power electronic converter which converts the pure dc into at most sinusoidal ac with low switching stress, low electromagnetic interference and output with less Total Harmonic Distortion (THD). The three popular topologies [5] of MLI are DCMLI [7] [5], Flying capacitor clamped MLI [5] and Cascaded H Bridge MLI [5].
These topologies have their own advantages and disadvantages. Out of three DCMLI is most popular inverter as it has following advantages.

1) Static voltage equalization among switches.

2) Reduced$\frac{dV}{dt}$.

3) No dynamic voltage sharing problem.

4) Economics of the converter.

The Flying Capacitor Clamped MLI requires more number of capacitors and Cascaded H Bridge MLI requires more number of dc sources. Despite of these advantages five-level DCMLI as shown in Figure 1 suffers from unbalance in capacitor voltages which shift the output voltage level from five to three as shown in the Figure 2 and makes outer two capacitors to share the entire supply voltage and it makes switch to take the stress twice the rated design. The inner two capacitors will completely discharge and become ineffective. The unbalance in capacitor voltages can be attributed to the excess discharge of the inner capacitors (C_2, C_3) as they are in operation for all the levels of the output voltage whereas the Outer capacitors (C_1, C_4) are in operation only during highest levels of the output voltage. The unbalance in the capacitors voltage varies with Load, load Power Factor (PF) and amplitude modulation index (ma). The unbalance is highest at unity PF and high ma .This happens because load voltage and current are in phase and the difference in discharge of capacitors is most.

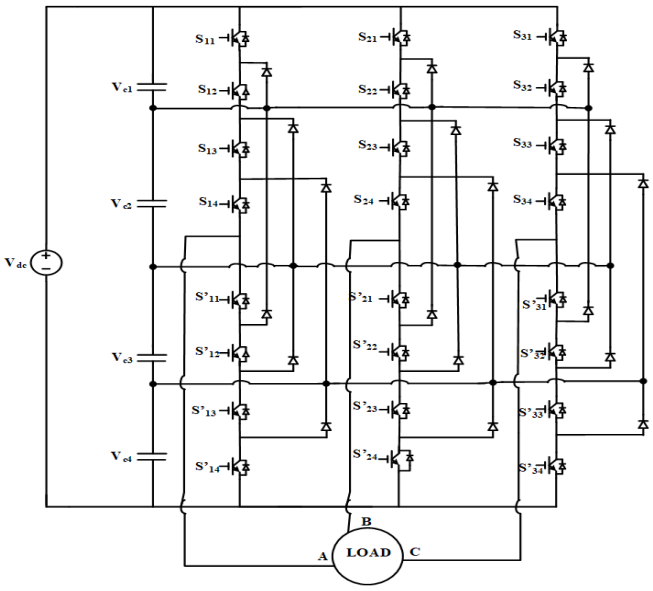


Fig. 1: Schematic of five-level DCMLI

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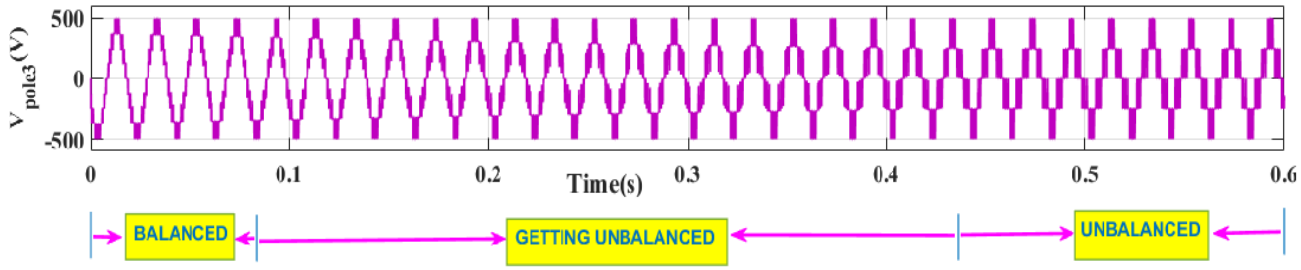


Fig. 2: Transition of DCMLI level from five to three

Similarly, at zero PF difference in discharge and charging of capacitors is least so they maintain balance. To maintain the balance there have been techniques proposed in the literature [2][10]. All these either use 5 level front end rectifier / inverter or use separate dc sources for each capacitor. These techniques require extra components and complex control circuits which increases the cost and complexity. In this paper a novel Hybrid PWM technique which provides self-balance without the usage of extra components is proposed.

2. Existing Techniques

For three-level DCMLI there exists well established techniques to solve neutral point voltage balancing problem. The popular techniques for three level inverters includes: CBPWM technique [4], Non-Near Vector (NNV) PWM technique [8] and hybrid [1], [6] of both the techniques. CBPWM technique fails at high ma and near to unity PF. While NNV SVM works well under these conditions but they have high switching losses due to usage of redundant states which doesn't fall into the same sector as the reference. These problems to certain extent were addressed by hybrid PWM technique. But none of these techniques could solve the problem in 5level inverter. For five-level DCMLI there are different source side [9] techniques available to balance the capacitor voltages like separate dc sources for each capacitor. This technique could solve the problem of balancing, but need extra components which make the circuit bulky and costly and usage of rectifier also injects harmonics into the supply. The other popular technique is back to back 5 level inverter and rectifier connection [2]. This technique is quite complex with many switches and complex control circuitry even though it offers many redundant states to balance the capacitor voltages. It can be noted that none of these techniques provide an inherent control over the capacitor voltage for DCMLI above 5 level. And these high level inverters find lot many applications in medium-high power drives, renewable energy and power quality applications. Thereby this paper proposes a novel hybrid PWM technique which can provide a solution to this problem.

3. Proposed Technique

This paper proposes an improved Hybrid PWM technique which is extension of the technique proposed of 3 Level NPC [3]. This technique is a combination of CBPWM and SVM, where at any given instant either of the techniques is applied as shown in the Figure 3. CBPWM is applied to meet load demand. SVM is applied at certain instants to balance dc capacitor voltages. The duration for which SVM is applied depends on load PF and M_a. Switching states in SVM are selected such that the overcharged capacitors i.e. C_1, C_4 get discharged and undercharged capacitor C_2, C_3 get charged as shown in the Table 1.

The balancing space vectors are applied to provide extra discharge time to the outer capacitors than that is actually provided by the CBPWM. As per the modulation techniques applied to meet the load demand the outer capacitors discharge at +ve and –ve peak levels of pole voltage respectively. Hence the balancing states need to be applied at instants other than +ve,-ve peaks so that extra discharge time can be provided for the outer capacitors. The instants at which balancing switching states are applied can be correlated from switching vector angle as shown in the Table 1.

Switching vector corresponding to ABC switching state:

ABC= [A*(e^ (j*0°)] + [B*(e^ (j*120°)] + [C*(e^ (j*240°)]

The switching vector for 433 switching state is as shown in equation (1):

$$433: V_{dc}\angle 0 + ((3*V_{dc})/4)\ \angle 120 + ((3*V_{dc})/4)\ \angle 240 = (V_{dc}/4)\ \angle 0 \quad (1)$$

The instants where the balancing switching vectors are applied is shown in Table 1. Applying balancing switching states by following the Table 1 results in quarter wave symmetry and all the even harmonics will be eliminated.

The block diagram of the Hybrid PWM technique is shown in the Figure 4 where SVM is applied for every 60° of fundamental cycle with a duration of pw (which depends on the load PF). Thereby the frequency of application of SVM is represented by 6F where F is the output frequency of inverter shown in the Figure 4. For the duration other than pw CBPWM is applied to meet the load requirement as shown in the Figure 3.

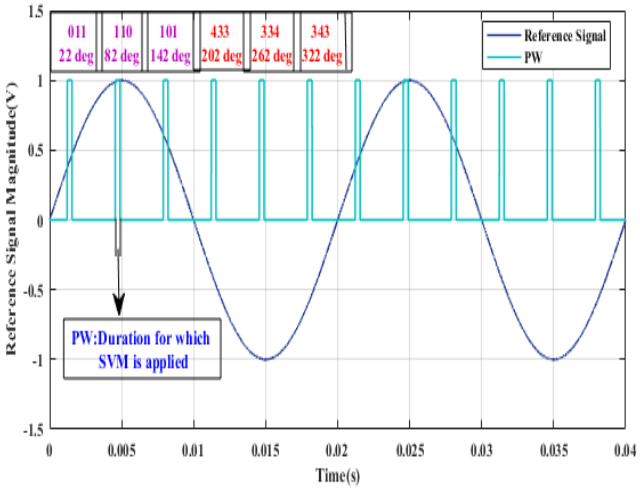


Fig. 3: Hybrid PWM technique

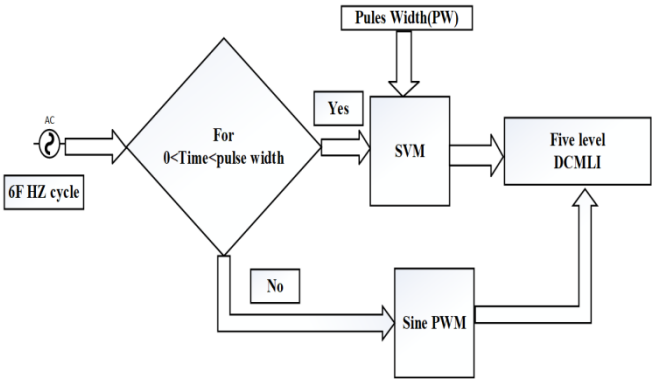


Fig. 4: Block diagram of Hybrid PWM technique

Table 1: Proposed technique SVM Switching States

S.No	SVM switching state	Instant of application (degrees)	Switching vector of Switching state	status of charge (ch) and discharge(dch) of capacitor(C)			
				C1	C2	C3	C4
1	433	202	(Vdc/4) ∟ 0	dch	ch	ch	ch
2	110	82	(Vdc/4) ∟ 60	ch	ch	ch	dch
3	343	322	(Vdc/4) ∟ 120	dch	ch	ch	ch
4	011	22	(Vdc/4) ∟ 180	ch	ch	ch	dch
5	334	262	(Vdc/4) ∟ 240	dch	ch	ch	ch
6	101	142	(Vdc/4) ∟ 300	ch	Ch	Ch	dch

Table 2: pw for various PF's

Figure 5	Load	Power flow		$(R_{ch}-R_{dch})/2=pw$	%Pw w.r.t fundamental frequency		
		Source to load (discharge time-R_{dch})(+P)	load to source (charge time-R_{ch})(-P)		Actual	Applied	Error
(a)	ZPF	0.01sec	0.01sec	0	0	0	0
(b)	UPF	0.02sec	0	0.01sec	50%	54.6%=6*9.1%	4.6%
(c)	0.9 PF lag	0.01712	0.00288	0.00712	35.6%	40.02%=6*6.7%	4.42%
(d)	0.8 PF lag	0.0159	0.0041	0.0059	29.5%	34.2%=6*5.7%	4.7%

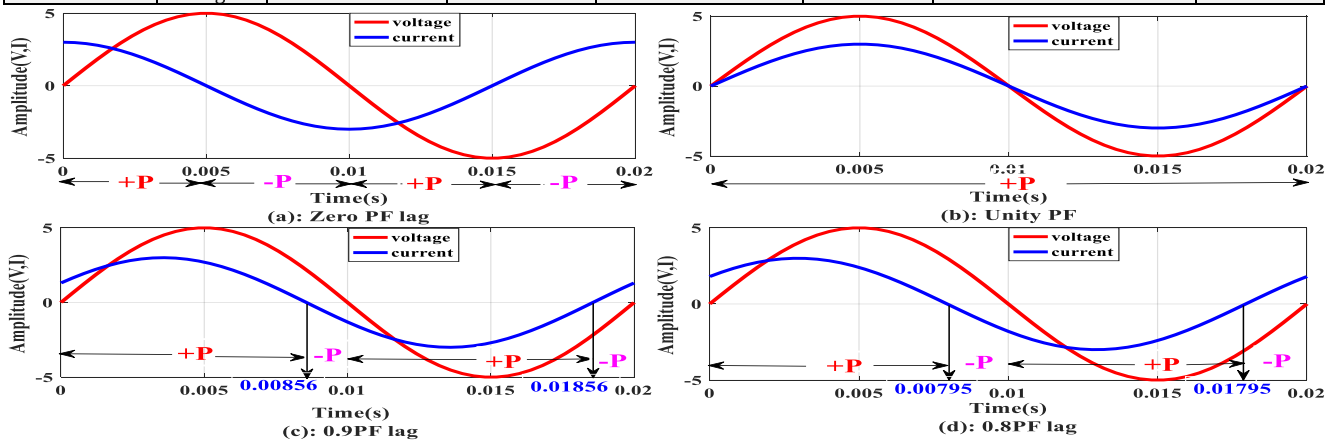


Fig.5: load current and voltages of 5level DCMLI for a) ZPF b) UPF c) 0.9PF lag d) 0.8PF lag

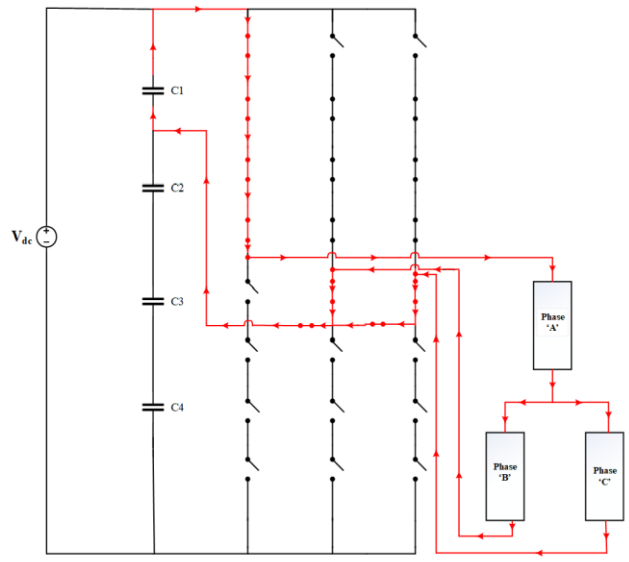


Fig. 6: 433 switching state of 5-level DCMLI

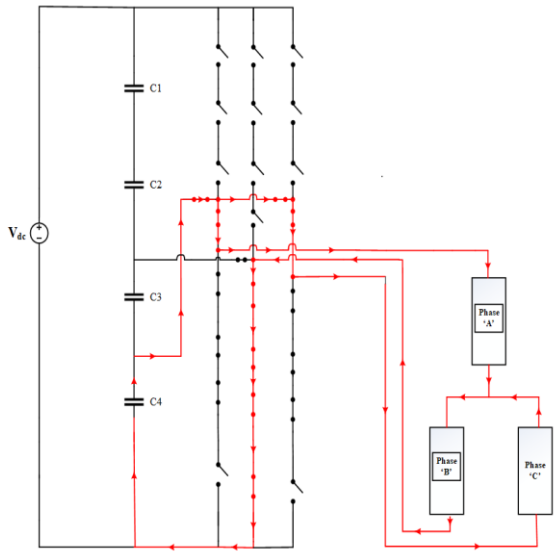


Fig. 7: 101 switching state of 5-level DCMLI

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The SVM states 433, 343 and 334 are selected so that top capacitor (C_1) will discharge as shown in the Figure 6 which results in charging of the other capacitors to maintain the dc bus voltage across the four capacitors as shown in Table 1. Similarly switching states 011,101 and 110 will discharge C_4 as shown in the Figure 7 and charge remaining capacitors. This entire operation takes place six times in every cycle of reference as shown in the Figure 3. Each balancing switching state is applied for a certain percentage of the period of the reference signal i.e. pw as indicated in the Figure 3. As the percentage pw (duration for which SVM is applied of reference period) varies the capacitor balance and the output distortion changes. As pw increases the capacitors get balanced with increased distortion in the output voltage. This distortion in the output voltage is attributed to the application of switching state Inappropriate to load demand and appropriate to capacitor balance.

3.1. PW Calculation

This analysis in calculation of PW is done for 50HZ load frequency.

Condition for capacitor balance:

$$R_{ch} - R_{dch} = 0 \quad (2)$$

If $(R_{ch}-R_{dch})/2=x$; (3)

Subtract x from both sides to get (2) where x=pw.

%pw= (pw/0.02)*100 (4)

Y=number of balancing switching states selected to apply

Applied %pw= (%pw/Y); (5)

The condition for the balance is given by the equation (2). It can be noted from Figure 5(a) that equ.2 is satisfied only for ZPF load. Hence for ZPF load case there is no need of compensation and thereby pw=0 as shown in Table 2.For all the other cases the equ.2 is not satisfied and hence pw need to be applied. The Figures 5(b), 5(c), 5(d) shows the charging and discharging durations for load PF's UPF, 0.9lag, 0.8lag which won't satisfy equation (2). So, some extra discharging rates for outer capacitors need to be provided by applying balancing switching states for pw time at instants shown in the Table 1. The extra discharge time for outer capacitors for pw time is applied based on the load PF which can be calculated by equations (2),(3),(4)(5) and calculated pw can be observed from table 2. The pw is applied to the inverter with a tolerance band of +5%. Thus, balancing of capacitor voltages for different PF's with appropriate pw can be determined by following the above mentioned procedure.

4. Results and Discussion

To evaluate the proposed technique a 5 level DCMLI with Supply Voltage V_{dc}=500v is considered. The dc capacitor voltage balancing of this inverter is tested for the two load PF's 0.8 and 0.9 for ma=1.0 as itis the extreme cause for imbalance. Its performance is evaluated in comparison with the conventional CBPWM technique.

4.1. CBPWM with ma=1.0

When CBPWM technique is applied to a 5 level DCMLI with load PF's 0.8 and 0.9 it can be observed from the Figure 8 that the outer two capacitors (C_1, C_4) each will get charged to half the supply voltage and inner two capacitors (C_2, C_3) will discharge completely within certain duration depending on load PF. When the load PF is high discharge rate of inner capacitors is very high. It can be verified from the Figure 8(a) and (b) that inner capacitor discharge of the five DCMLI with 0.8PF is slower than that with 0.9PF lag load. In CBPWM the capacitors imbalance leads to decrement of the level of the inverter from five to three, at instant where the inner capacitors completely discharge which can be witnessed from the load voltage waveforms shown in the Figure 9 (b) and (d). As shown in Figure 9(a) and (c) when operated with 0.8PF and 0.9PF lagging load the level of the inverter starts its transition. It can be observed from Figure 9(a) and (c) all the five levels are present at 0.2s. But with lower magnitudes for middle levels and constant magnitudes for peak levels compared to the first cycle which causes the distortion as shown in Figure 9(a) and (c). The THD's after transition from five to three level can be observed from the Figure 12(e) and (f).

4.2. Proposed Hybrid PWM technique with ma=1.0

The proposed Hybrid PWM technique is applied to 5 level DCMLI by following the block diagram as shown in Figure 4. It can be Observed from the Figure 10(a) and (b) that the capacitor voltages get balanced for both the PF's with different pw which leads to maintaining the level of the inverter as five as shown in the Figure 11.The level of the inverter is maintained for 0.8PF lag load with pw=5.7% as shown in the Figure 11(a) and (b) and their respective THD's are shown in the Figure 12(a) and (b), and for 0.9PF lag load with pw=6.7% as shown in the Figure 11(c) and (d) and their respective THD's are shown in the Figure 12(c) and (d).Figure 9 and Figure 11 shows the load voltage waveforms of conventional CBPWM and the proposed PWM technique it can be clearly observed that the five levels are restored with a nominal increase in THD. Thereby employing proposed hybrid PWM technique yields good results in balancing capacitor voltages for different PFs and will improve the performance of five level DCMLI. The effect of the proposed PWM technique for various PF's with corresponding pw adjustment to optimize the balance between the capacitor voltage balance and output power quality is shown in Table 3.

Table 3: Capacitor voltages and THD's for different load PF's at ma=1.0

Load	Pw (%)	C1	C2	C3	C4	THD (%)
R=10 ohms (**UPF**)	9.1	125V	125V	125V	125V	82.66
R=100 ohms L=0.2388H (**0.8PF**)	5.7	125V	125V	125V	125V	54.91
R=100 ohms L=0.4244H (**0.6PF**)	4.8	125V	125V	125V	125V	47.95
R=100 ohms L=0.7293H (**0.4PF**)	4.1	125V	125V	125V	125V	43.29
R=100 ohms L=1.5594H (**0.2PF**)	2.8	125V	125V	125V	125V	33.80

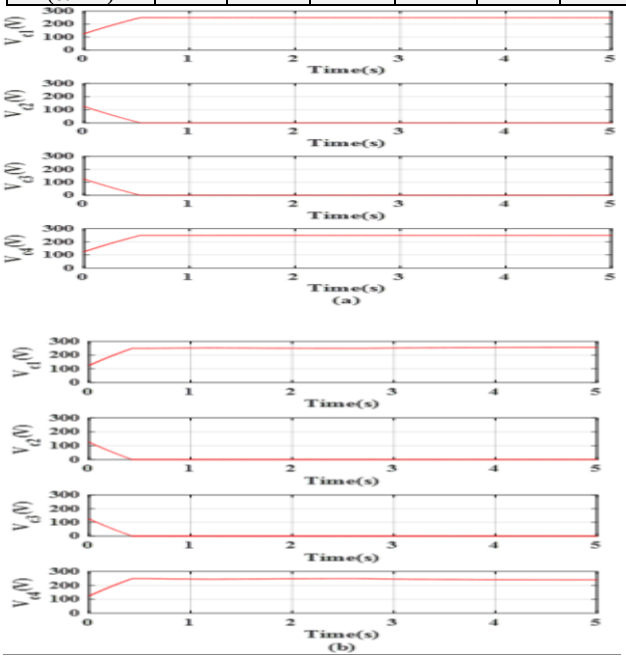


Fig. 8: Capacitor voltages of CBPWM technique (a) for 0.8PF lag load with Ma=1.0(b) for 0.9PF lag load with Ma=1.0

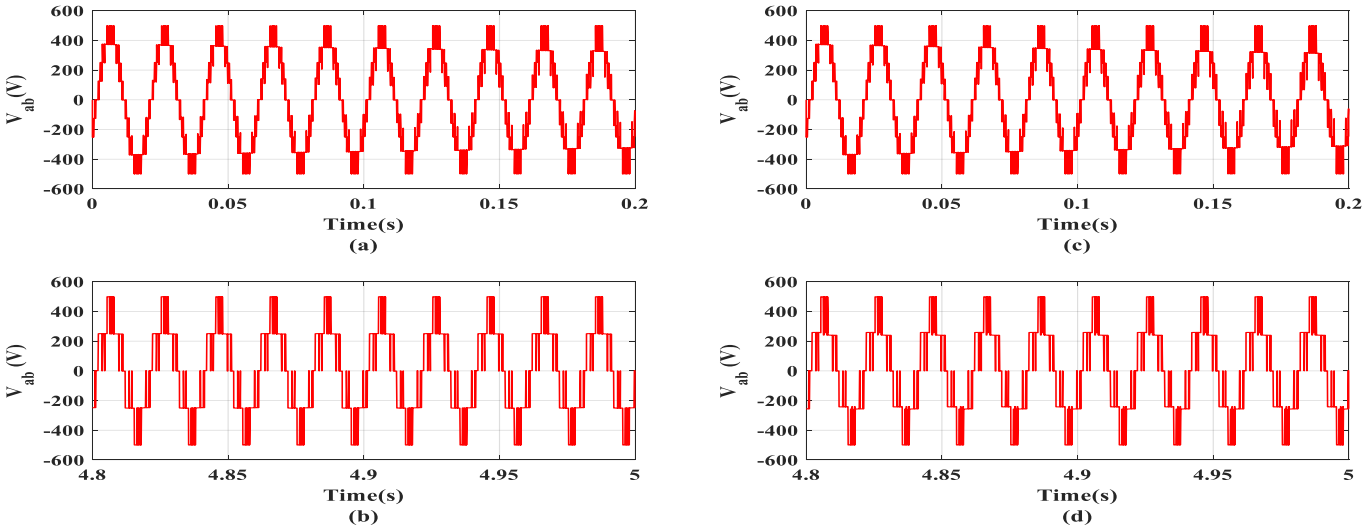


Fig. 9: Line Voltages of CBPWM technique with Ma=1.0 for 0.8PF lag load (a) Initial cycles (b) final cycles For 0.9PF lag load(c)initial cycles(d) final cycles

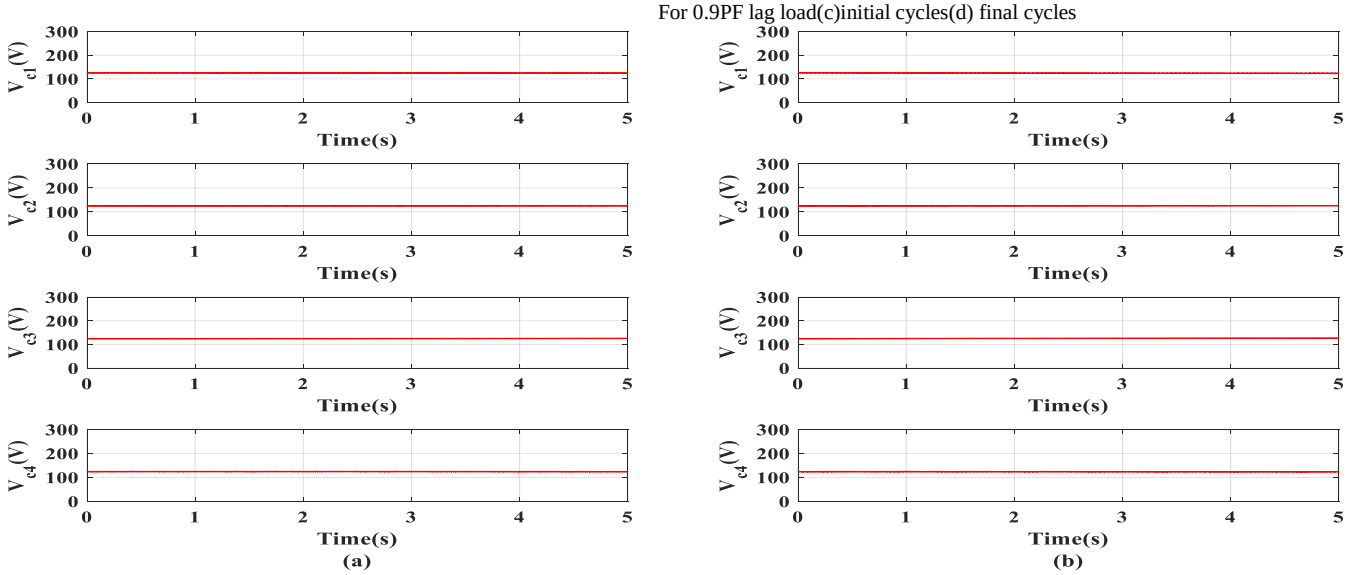


Fig. 10: Capacitor Voltages of Hybrid PWM technique for (a) 0.8PF lag load with Ma=1.0, pw=5.7% (b) for 0.9PF lag load with Ma=1.0, pw=6.7%

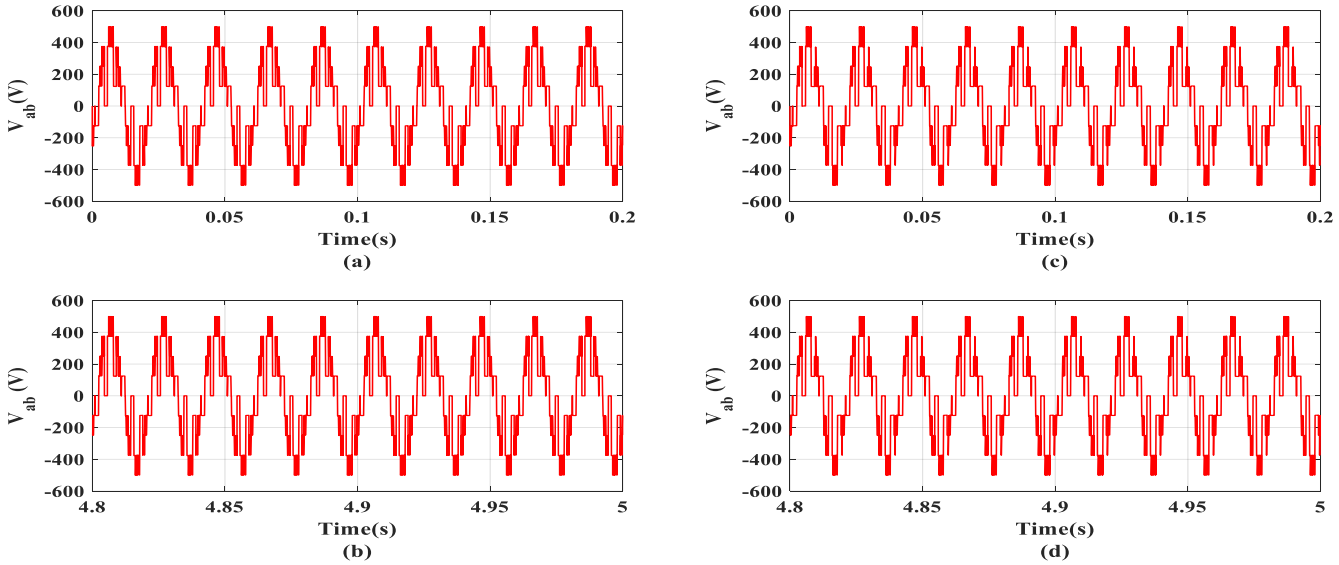


Fig. 11: Line Voltages of Hybrid PWM technique with Ma=1.0 for 0.8PF lag load, pw=5.7% (a) Initial cycles (b) final cycles For 0.9PF lag load pw=6.7% (c) initial cycles (d) final cycles

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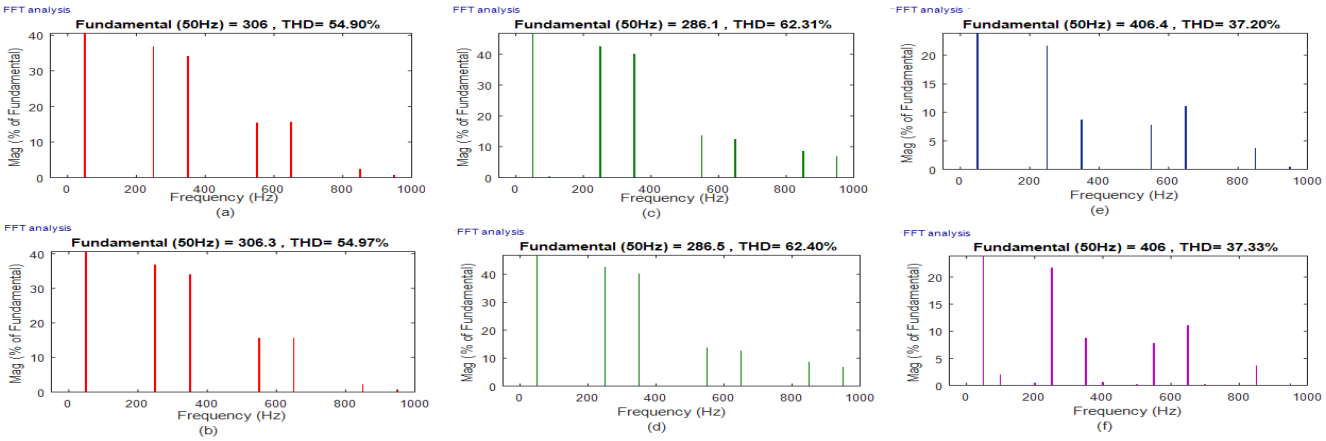


Fig. 12: THD for PF=0.8lag (a) initial cycles of Hybrid PWM (b) final cycles of Hybrid PWM (e) final cycles of SPWM for PF=0.9lag (c) initial cycles of Hybrid PWM (d) final cycles of Hybrid PWM (f) final cycles of SPWM

5. Conclusion

By applying Hybrid PWM for higher PF's with high pw and ma the capacitor voltages get stabilized at a cost of increased THD as shown in the Table 3 in the load voltages. Applying Hybrid PWM with low pw and high ma the capacitor voltages approach CBPWM condition with some delay and the load voltages has low THD. So, there is a compromise between the balancing of the capacitors and the output voltage distortion. By balancing we are achieving all five levels and capacitors have equal voltages and each switch undergoes a maximum stress of $V_{dc}/4$ and low electromagnetic interference which satisfies all properties of multilevel inverter. This inverter can be used in industrial heating applications as it is with high THD but if we increase THD for increased heating which leads to opposite unbalance i.e. inner two capacitors (C_2, C_3) overcharges and outer two capacitors (C_1, C_4) under charges which again the same problem. So, the fixed value of pw should be applied to for a given PF load to balance capacitor voltages. This technique gives less THD at lower PF's as pw under this case is very less and it maintains balance even at higher PF. This is best suited modulation technique for 5-level DCMLI for the inherent balance of the capacitor voltages in the five level DCMLI.

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