

Design of low power 10GS/s 6-Bit DAC using CMOS technology

P.Ramakrishna ¹, K Hari Kishore ²

¹Research Scholar, Department of ECE, Koneru Lakshmaiah Educational Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India 522502

²Professor, Department of ECE, Koneru Lakshmaiah Educational Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India 522502

*Corresponding author E-mail: Prk.cvsr@gmail.com

Abstract

A Low power 6-bit R-2R ladder Digital to Analog Converter is presented in this paper. Here the R-2R network designed using resistors with only two values-R and 2xR and the switch is designed by using both NMOS and PMOS Transistors. This Digital to Analog Converters operated with low voltage, by applying dynamic threshold MOSFET (DTMOS) logic. This design achieved less INL and DNL which is 0.3 and 0.06 respectively. Power supply required to operate this device is only 1V with 10GHz conversion rate. This design is implemented by using 0.18µm CMOS technology.

Index Terms: R-2R ladder network, high-speed logic, current steering DAC, DTMOS, CMOS technology.

1. Introduction

Due to rapid change in bandwidth of communications with giant speed, increases the need of data converters with high-speed are more, especially for mobile communications. If we need to handle the multipart signal processing more efficiently in the digital domain, the data conversion and interface which is analog to digital is required in the direction of the antenna. When compare with other high frequency generator designs or synthesizers within analog domains, the direct digital Frequency synthesizer (DDFS) is playing more vital role in the mobile communications because of only its controlling procedure is simple than other designs. While going to design DDFS the Digital to Analog Converter (DAC) as a front end device in those systems is most important component. The Digital to Analog Converter (DAC) with high sampling rate, medium resolution (6-8 Bits) are more and more required for high speed data links such as optical communication systems, radar communication systems or satellite communication systems. Another forthcoming and very advanced application of Digital to analog converters with a high-speed, less power consumption is 5G mobile communication systems [8]. A DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter is presented in [2]. So that the medium resolution, high sampling rate i.e. in several GHz and low power are the key parameters for this application. Here we proposed a design which is having low power and medium resolution Digital to analog converter with 10GS/s sampling rate to overcome the above mentioned applications.

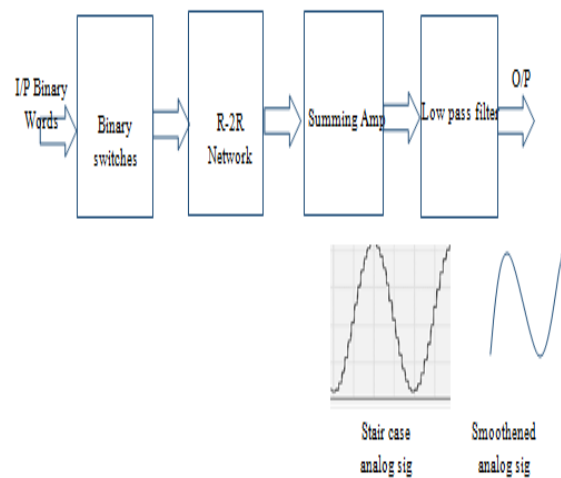


Fig. 1: Block diagram of 6-bit DAC

2. Architecture of DAC

The R-2R ladder architecture gives architecture appropriate for strategies, which is applied by using highly linear resistors. Those DACs encompass a shape of resistors, that is having values may be closely matched [14]. This topology is binary weighted and may provide a better resolution as compared to its in simple terms binary weighted counterpart. a completely popular architecture for D/A converters are R-2R ladders. The R-2R ladder structure is proven in parent four. The cutting-edge resources are all equally large, and the switches are managed with the aid of the digital enter, $X = (x_{N-1} \dots x_0)$, in which N is the quantity of bits and is x_{N-1} the MSB. Due to consisting of slices which include a much

less r_{on} switch, a $2xR$ resistor, and an R resistor, we will make a bendy format and suit the components nicely. The resistors are, however, often nonlinear and contains signal-dependent capacitances, which yield distortion. Glitches will be generated due to the on and off times between the MSB and LSB switches. In the R-2R ladder architecture shown in Figure 4, in this architecture all the switches passes same amount of current through them due to this reason the complexity of switch design is reduced and make it easily. However the internal voltage nodes are

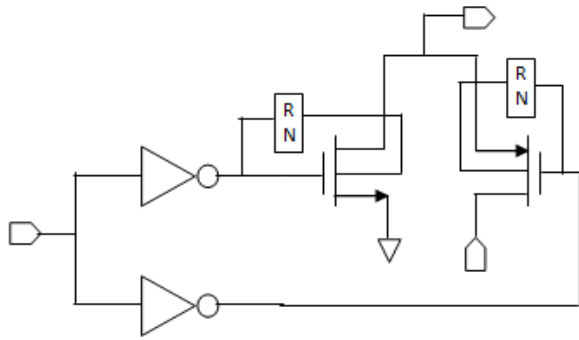


Fig. 2: Circuit diagram of Switch

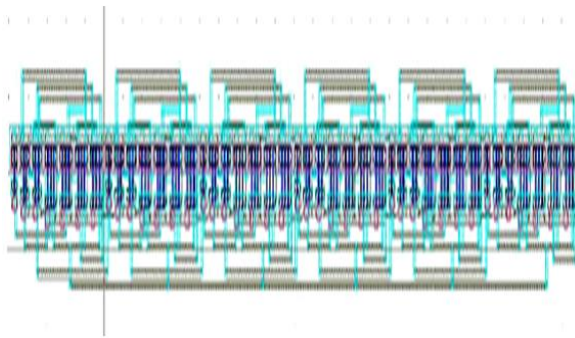


Fig. 3: Layout of 6-bit Counter

Changing along with time so the terminal voltages of current sources are varying, due to this cause nonlinearity and distortion is increased. In this high-speed R-2R ladder DAC architecture, the dynamic characteristics of the switch enact the important design constraints. The main parameters such as timing alignment of the switches, current mismatch, output impedance of the switches are influenced these dynamics.

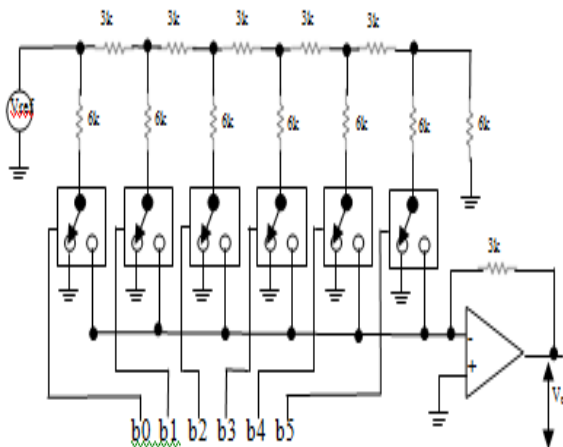


Fig. 4: A 6-bit R-2R ladder DAC

3. Circuit implementation

The proposed design is developed by using CMOS technology with UMC0.18 μ m. Here the resistive circuit is designed by using poly resistors. The first rate gain with the proposed DAC is the so-called R/2R DAC, which uses fewer precise resistor values. Manufacture can be simplified if there are fewer one of a kind resistor values to make. At the output node of the switches having the same low resistive load. When we looking from the output can observe that the input impedance is always $2R$. At the leftmost slice the impedance is given by two resistors in series and the input impedance is $2R$. At the next section the same applies since we have a $2R$ resistance in parallel with the two series R resistances. The contemporary resources are assumed to have infinite output impedance. Ultimately, the output impedance of the overall DAC is $2R$. a very popular architecture for virtual to Analog Converters is R-2R ladders. Those ladders are useful for understanding binary-weighted currents with a small range of components and with a resistance ratio of only 2, unbiased of the variety of bits, N . As an end result, this R-2R technique typically gives each a smaller length and better accuracy than different procedures. Recollect the R-2R ladder approach proven in under figure4. The circuit is run off of 1 volt. The Circuit consists of 6 digital inputs, while giving binary inputs can to get output as analog signal between 0 and 1 volt. The 6 digital inputs namely b_0 - b_5 , and the output name is V_o . The expected maximum frequency is 10GHz and expected that the step size will be nearly linear. The expected power dissipation is 1.5mw. To obtain a reasonable output range, the resistor values should vary. The resistor values are calculated for the design to get best results. Calculated values of resistors are:

$$R = 3K \Omega, 2R = 6K \Omega, R_f = 3K \Omega$$

From the figure 4, when a binary input is logic 1 the reference voltage is connected throughth resistor to the virtual ground of the op-amp, otherwise, it is connected to the ground. Therefore, we have

$$V_{out} = -V_{ref} \sum_{i=0}^n b_i \frac{1}{2^{i+1}}$$

$$INL = \frac{I_{unit} R_L^2 N^2}{4R_S}$$

Where

R_L - The load resistance

R_S - The output impedance of the switch

N - The number of bits

I_{unit} - The LSB current

The above equation shows a connection between integral nonlinearity (INL) and the output impedance of switch. Here the proposed DAC has 6bits.

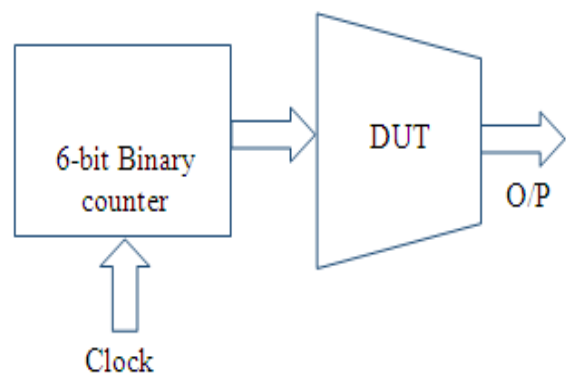


Fig. 6: Block diagram of Test setup.

Next and most important device in this proposed DAC is SWITCH, which is designed by using CMOS transistors [14]. Here a low power technique is applied to the switch which is

Dynamic Threshold Metal Oxide Semiconductor logic (DTMOS) [15]. By using the DTMOS logic we can alter the threshold voltage that is decreasing the threshold voltage can decrease the power supply voltage. If the gate of the transistor is hooked up to the frame, see Figure2, a Dynamic Threshold Transistor (DTMOS) additionally referred to as body managed MOS and Variable Threshold MOS is created [15]. Observe that because the voltage at the gate is attached to Resistive Network (RN) which acts as a ability divider.

$$V_{Th} = V_{Th0} + \gamma_B(\sqrt{|2\phi_F - V_{BS}|}) - (\sqrt{2\phi_F})$$

If voltage at the gate rises, the body voltage is ahead-biased with respect to the supply and VT drops. At 0 V gate enter, VT is the same as a ordinary, floating-frame transistor. DTMOS transistors have the blessings of low leakage contemporary, excessive modern-day force. Here simple differential pair is used as a switch. The unwanted capacitance such as parasitic capacitances are main components to degrade the dynamic behavior the so-called designed DAC and also interconnections plays a critical role. Due to this reason and to improve the dynamic behavior of the DAC we mainly focused on low wiring capacitance in the layout designs shown in figure 5.

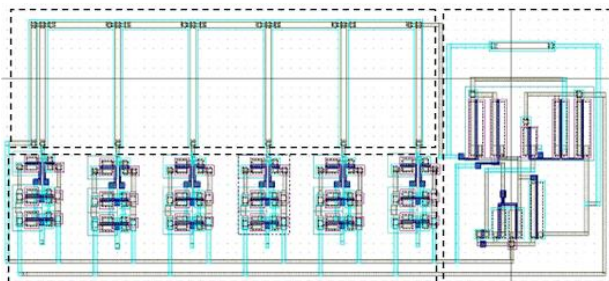


Fig. 5: Layout of 6-bit DAC

4. Results and Discussions

The Low power 10GS/s 6-bit DAC has been achieved desired specifications. This is designed using UMC 0.18µm CMOS technology. This complete Digital to analog converter can operating with 1V supply voltage. It consumes power of 1.5mW, with a counter for testing the DAC; this counter consumes almost 70% of the total power dissipation. The 6-bit DAC was tested by generating test patterns using 6-bit binary counter, the layout of counter is shown in figure 3. The primary purpose of this senior design is to test a functional 6-bit Digital to Analog Converter that can generate up to a frequency of 20GHz. The DAC consists of two general stages. The counter output is fed to the DAC and also the reference (input) signal given to that. The DAC output is in stair case analog signal. That is if the counter output increases sequentially then the DAC output step size is increased. The test setup is presented in Figure 6.

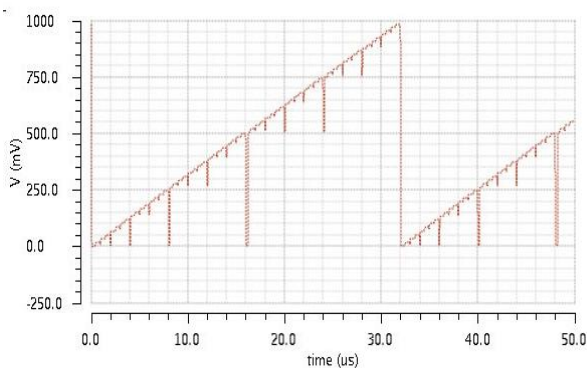


Fig. 7: Simulation results of 6-bit DAC

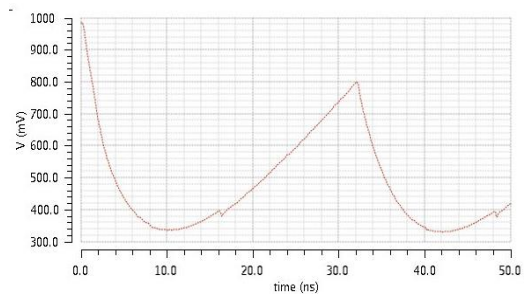


Fig. 8: Simulation Results of 6-bit DAC after filtering with 1GHz clock

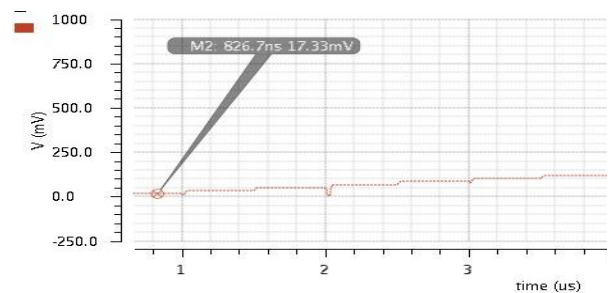


Fig. 9: Zoomed portion Simulation results of 6-bit DAC

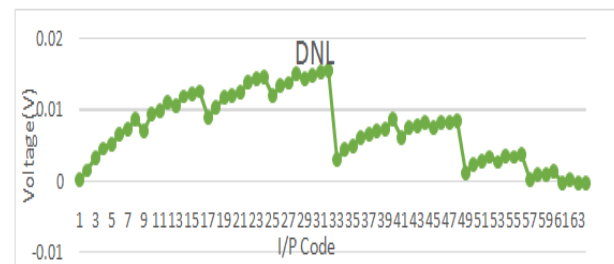


Fig. 10: Measured DNL plot

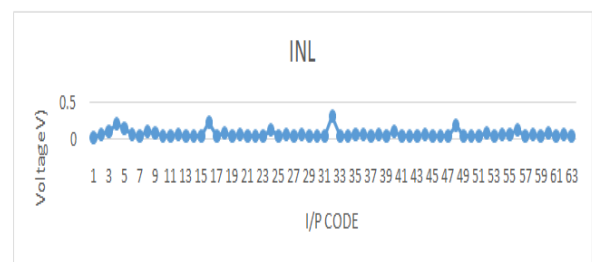


Fig. 11: Measured INL plot

Table 1: Summary of DAC Characteristics.

Process	0.18µm CMOS
Resolution	6 bit
Conversion rate	10 GHz
INL / DNL	0.3 / 0.016 LSB
Power supply	1 V
Power	20µW

Fig. 7shows reconstructed DAC output for input bit patterns. A 10 GHz clock is applied to the DAC. Here in this step response of the Digital to analog converter getting full-swing as shown in Fig. 8. The zoomed portion of the full-swing transition is shown in Fig. 9. The figures 10 and 11 shows the achieved DNL plot of 0.06LSB and INL plot of 0.3LSB.

5. Conclusion

Digital to Analog conversion is a process which is often required for application such as radar, satellite communication, wireless applications and many more. The main application of this Digital to Analog Converter is to generate a UWB Wave i.e. above 16GHz frequency for mobile communications. The design process of 6-bit 10G/s Binary weighted DAC included the realization of individual blocks such as Binary switch, R-2R ladder network, summing amplifier, Low Pass Filter and 6-bit Counter. The design based on conversion of CMOS schematics in to physical layout. All the cells are verified using a composite test bench. The 6-bit 10G/s Binary weighted DAC has been realized by cascading the individual blocks. All the layout cells are wired to form the final core of the low power 6-bit 10G/s DAC have been verified. The Digital to analog converter is achieved DNL of 0.06LSB and INL of 0.3LSB.

References

- [1] Van den Bosch, A. et al, A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter, IEEE Journal of Solid State Circuits, Vol. 36, pp. 315-324, 2001.
- [2] Yoan veyrac, Francois Revet, Yenn Deval "A 65-nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter", IEEE Transactions on Circuits and systems II, vol.3, 2016, pp.104-108.
- [3] J.P. UYEMURA, Fundamentals of MOS Digital Integrated Circuits, Addison- Wesley, 1988.
- [4] P.E. Allen and D.R Holberg, CMOS Analog Circuit Design, Second Edition, Oxford University Press, 2002.
- [5] R.T. Howe and C.G. Sodini Microelectronics: A Integrated Approach, Prentice Hall, NJ, 1997.
- [6] J.M. Soden, C.F. Hawkins, R.K. Gulati and W. Mao IDDQ testing: a review, Journal of Electronic Testing: Theory and Applications, vol.3, 1992, pp. 291- 303.
- [7] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995, ISBN 0-7803-1093-4.
- [8] D. Baranauskas, D. Zelenin, A 0.36W 6b upto 20GS/s DAC for UWB Wave Formation, Proc. ISSCC, pp. 580- 581, 675, 2006.
- [9] B. Schafferer, R. Adams, A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications Proc. ISSCC, pp.360-361, 532, 2004.
- [10] D. C. Larson, "High Speed Direct Digital Synthesis Techniques and Applications", Proc. GaAs IC Symposium, pp. 209-212, 1998.
- [11] P. Schvan, et al, "A 22 GS/s 6b DAC with Integrated Digital Ramp Generator", Proc. ISSCC, pp. 122-123, 588, 2005
- [12] M. Rodwell, "High Speed Integrated Circuit Technology, Towards 100GHz Logic", World Scientific, 2001, ISBN 981-02-4638-2
- [13] W. Cheng et al. "A 3b 40GS/s ADC-DAC in 0.12 μ m SiGe", Proc. ISSCC 2004, pp. 262-263, 2004.
- [14] Samiran Halder, Hans Gustat "A 30 GS/s 4-Bit Binary Weighted DAC in SiGe BiCMOS Technology" IEEE BCTM 4.1, 4244-1018, 2007.
- [15] Assaderaghi, F., "DTMOS: Its Derivatives and Variations, and their Potential Applications," Int. Conf. on Microelectronics, pp. 9-10, Nov. 2000.
- [16] Dr. Seetaiah Kilaru, Hari Kishore K, Sravani T, Anvesh Chowdary L, Balaji T "Review and Analysis of Promising Technologies with Respect to fifth Generation Networks", 2014 First International Conference on Networks & Soft Computing, ISSN:978-1-4799-3486-7/14, pp.270-273, August 2014.
- [17] Meka Bharadwaj, Hari Kishore "Enhanced Launch-Off-Capture Testing Using BIST Designs" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.12, Issue No.3, page: 636-643, April 2017.
- [18] N Bala Dastagiri, Kakarla Hari Kishore "Reduction of Kickback Noise in Latched Comparators for Cardiac IMDs" Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.43, Page: 1-6, November 2016.
- [19] A Murali, K Hari Kishore, D Venkat Reddy "Integrating FPGAs with Trigger Circuitry Core System Insertions for Observability in Debugging Process" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.11, Issue No.12, page: 2643-2650, December 2016.
- [20] Mahesh Mudavath, K Hari Kishore "Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications Integrating FPGAs" Asian Journal of Information Technology, ISSN No: 1682-3915, Vol No.15, Issue No.20, page: 4040-4047, December 2016.
- [21] P Bala Gopal, K Hari Kishore, B.Praveen Kittu "An FPGA Implementation of On Chip UART Testing with BIST Techniques", International Journal of Applied Engineering Research, ISSN 0973-4562, Volume 10, Number 14, pp. 34047-34051, August 2015.
- [22] S Nazeer Hussain, K Hari Kishore "Computational Optimization of Placement and Routing using Genetic Algorithm" Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.47, page: 1-4, December 2016.
- [23] N Bala Gopal, K Hari Kishore "Analysis of Low Power Low Kickback Noise in Dynamic Comparators in Pacemakers" Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.44, page: 1-4, November 2016.
- [24] T. Padmapriya and V. Saminadan, "Inter-cell Load Balancing technique for multi-class traffic in MIMO-LTE-A Networks", International Journal of Electrical, Electronics and Data Communication (IJEEEDC), ISSN: 2320- 2084, vol.3, no.8, pp. 22-26, Aug 2015.
- [25] S.V.Manikanthan and D.Sugandhi "Interference Alignment Techniques For Mimo Multicell Based On Relay Interference Broadcast Channel" International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE) ISSN: 0976-1353 Volume- 7, Issue 1 –MARCH 2014.
- [26] Rajesh, M., and J. M. Gnanasekar. "GCCover Heterogeneous Wireless Ad hoc Networks." Journal of Chemical and Pharmaceutical Sciences (2015): 195-200.
- [27] S.V.Manikanthan and T.Padmapriya "Recent Trends In M2m Communications In 4g Networks And Evolution Towards 5g", International Journal of Pure and Applied Mathematics, ISSN NO:1314-3395, Vol-115, Issue -8, Sep 2017.