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Research paper

A modified PV fed 9 level inverter for standalone applications with reduced number of switches

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Abstract

The power crisis in India is increasing at an alarming rate. Solar power is a domestic source of energy and its availability throughout the year makes it a primary target to solve this crisis. It will never produce any hazardous waste and it won't pollute the air. But various issues like Power quality problems and Harmonic distortion seep in due to the intermittent nature of PV system. Multi-Level Inverter (MLI) gives solution for PQ issues and helps in high power handling capabilities. In this work a new multilevel inverter topology is proposed. The controlled pulses are generated through sinusoidal PWM techniques. The proposed topology is implemented and the controlled circuit is simulated in MATLAB/SIMULINK. The same is realized in the hardware circuit having a cost effective dsPIC30F2010 digital controller. The proposed topology consists of only seven power electronic switches and that is the main advantage of this topology. The Simulation results and the Hardware results reveal that the suggested technique is highly advantageous.

Keywords: *Photovoltaic; Power Quality; Alternating Current; Multilevel Inverter; Digital Signal Processor.*

1. Introduction

The exhaustion of fossil fuels and the environmental hindrance caused by the conventional sources is a huge concern in the modern world and it has gradually resulted in global warming. India is a significant consumer of energy sources. India consumes its maximum energy in residential, commercial and agricultural purpose. According to the International Energy Agency (IEA) coal accounts for 40% India's total energy consumption followed by 27% percent of the combustible renewable and other sources like nuclear, oil, hydro, solar, wind etc contribute another 33% over all. Therefore a huge emphasize on power generation through renewable sources is the need of the hour. Being a tropical country, India receives abundant solar energy. So Photo Voltaic power generation can be one of the key things to resolve the rising energy demand. Power generation through PV system has its own advantages as it is pollution free & cheap. Another advantage of using solar energy is its portability. In order to tackle the present energy crisis one has to develop an efficient method so that maximum power can be extracted from the incoming solar radiation [1]. The power conversion mechanisms become more compact in the past few years. The development in power electronics has helped engineers to come up with very small but powerful systems to withstand the high power demand. But the disadvantage of these systems is the increased power density [2].

There are certain demerits for inverters which usually convert DC power to AC power such as low efficiency, high switching losses and they are expensive too. Another topology which have an advantage over the other topologies are microinverter type topology. It increases the system reliability by 15 to 20 percent but with an extra burden of high cost [3]. These demerits can be rectified to a certain extend using multilevel inverters. In recent years multilevel inverters are used for high power and high voltage applications [3]. Its output voltage produces a staircase like waveform which is similar to a sinusoidal waveform and also its output has the advantage of fewer harmonics when compared to the conventional bipolar inverter. If the level of multilevel inverter increases to N level, the harmonics of the output voltage will be reduced to zero [4].

The main classifications of Multilevel Inverter are Diode clamped multilevel inverter, Flying capacitor inverter and cascaded multilevel inverter.

The cascaded multilevel inverter has an advantage over the other two topologies as it requires less number of components. As the components become lesser, the price and weight of the inverter will also reduce. The control methods used in cascaded is very easy when compared to the other topologies [5].

However, the main disadvantage of the multilevel converter is that the more number of voltage level lead to increase in number of main switches and with it complexity of control technique and DC link capacitor voltage imbalance also increases [6][7]. But there are several advantages compared with traditional or conventional power conversion methods. In multilevel converter the isolated DC sources or bank of series capacitors are used [8]. Isolated DC sources are available from the Photovoltaic cell or rectified output from the three phase main supply [9].

These advantages when compared to other multilevel inverter topologies make this topology very attractive to the industrial applications and researchers all over the world contributing to improve the performance of multilevel converter [10]. And along with these different control strategies such as fuzzy logic controller can increase the efficiency of the system [11].

2. Existing topology

The existing seven level inverter topology can be used in solar systems and other industrial applications. It uses six power electronic switches for its operation. The seven level inverter used in

photovoltaic system requires a power converter, transformer and capacitors. Boost or flyback converter is commonly used as power converter which boosts the voltage from solar array to a required level. An inverter which generates 11 level is also generated by increasing the number of semiconductor switches [12]. The power converters can be connected in different configuration depending on its applications.

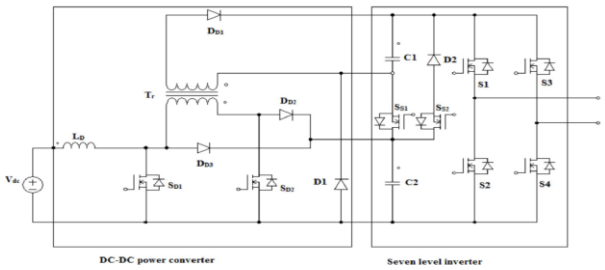


Fig. 1: Seven Level Inverter Circuit Diagram.

But the main disadvantage related to these topologies is that when the voltage level increases, the number of semiconductor switches and the source required also increases. In order to overcome this, a new topology is introduced.

3. Proposed topology

This paper proposes a new topology for generating nine output voltage levels using multicarrier modulation technique. This cascaded H-bridge multilevel inverter will have an added advantage as it is almost similar to a seven level inverter with one added bidirectional switch. The proposed nine level inverter circuit diagram is shown in Fig. 2. The proposed nine level inverter generates nine output voltage levels ie Vdc, 3Vdc/4, Vdc/2, Vdc/4, 0, -Vdc/4, -Vdc/2, -3Vdc/4, -Vdc.

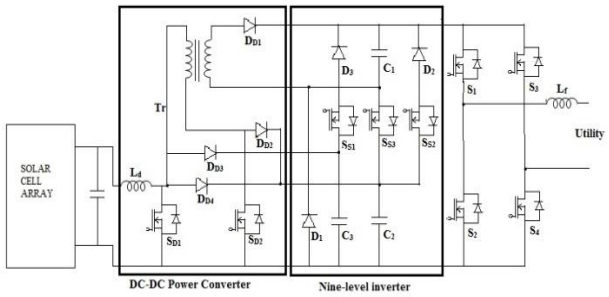


Fig. 2: Nine Level Inverter Circuit Diagram.

The fig.3 represents the different modes of operation of the proposed nine level inverter. In positive half cycle S1 and S4 will be forward biased and S2 and S3 will be reverse biased. Fig. 3(a) shows mode 1 operation of the proposed inverter. In this mode switches S1 and S4 will be conducting and the switches SS1, SS2 and SS3 will be in off state. Diode D1 will provide a passage for the capacitor C1 to discharge and the output voltage of the inverter in this mode will be Vdc/4. Fig. 3(b) shows mode 2 operation. Switches S1, S4 and SS2 will be conducting in this mode and switches SS1 and SS3 will be in off state. The capacitor C2 acts as the discharging capacitor and it discharges through diode D2. The output voltage generated in this mode will be Vdc/4. Mode 3 is shown in fig. 3(c). In this mode switches SS1, SS2, S1 and S4 will be conducting and the switch SS3 will be off. Two capacitors C2 and C3 discharges through diodes D2 and D3 and as a result of that the output of the inverter will be 3 Vdc/4. Fig. 3(d) represents Mode 4. All switches SS1, SS2, SS3, S1 and S4 will be conducting at the same time in this mode and also all the capacitors will be discharging through diodes D3 and D2. As a result of this full voltage Vdc appears across the output. In mode 5 which is shown in fig. 3(e), all switches will be turned off except S4. So the output voltage will be zero.

In negative half cycle S2 and S3 will be forward biased and S1 and S4 gets reverse biased. Mode 6 is shown in fig. 3(f). Switches S2 and S3 will be conducting in this mode and the switches SS1, SS2 and SS3 are turned off. The capacitor C1 discharges through diode D1 and –Vdc/4 appears across the output. Switches SS2, S2 and S3 will be conducting in mode 7 which is shown in fig. 3(g) and the switches SS1 and SS3 are turned off. The capacitor C2 discharges through the diode D2. An output voltage of –Vdc/2 will be produced in this mode. In mode 8, switches S2, S3 and SS1 will be conducting and switch SS3 will be turned off. Mode 8 operation is given in fig. 3(h). Here capacitors C2 and C3 will be discharging through diodes D2 and D3. The output voltage in this will be -3Vdc/4. In mode 9 all the switches will be conducting and the capacitors C1, C2 and C3 discharges through the diode D3 and D2. The output voltage will be –Vdc. This mode is shown in fig. 3 (i).

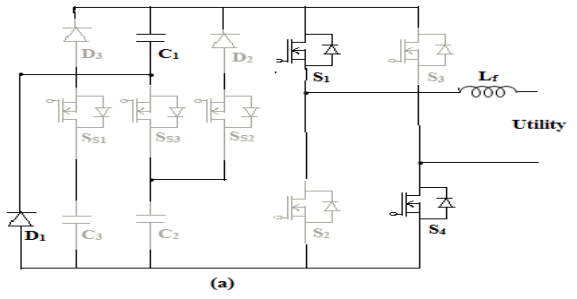
Table 1: Switching Table Nine Level (A) Positive Cycle (B) Negative Cycle

(A)

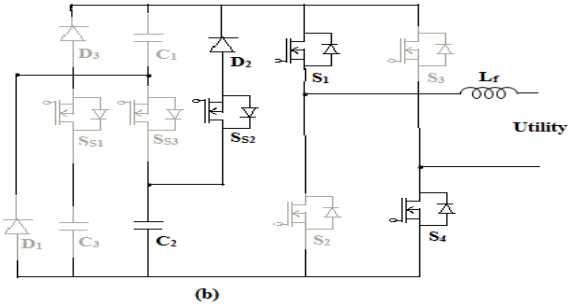
	Ss1	Ss2	Ss3	S1	S2	S3	S4
0 - 0.25 Vdc	0	0	0	1	0	0	1
0.25 Vdc – 0.5 Vdc	0	PWM	0	1	0	0	1
0.5 Vdc – 0.75 Vdc	PWM	1	0	1	0	0	1
0.75 Vdc - Vdc	1	1	PWM	1	0	0	1

(B)

	Ss1	Ss2	Ss3	S1	S2	S3	S4
0 - 0.25 Vdc	0	0	0	0	1	1	0
0.25 Vdc – 0.5 Vdc	0	PWM	0	0	1	1	0
0.5 Vdc – 0.75 Vdc	PWM	1	0	0	1	1	0
0.75 Vdc - Vdc	1	1	PWM	0	1	1	0



(a)



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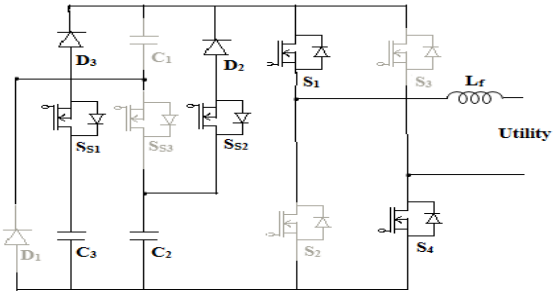
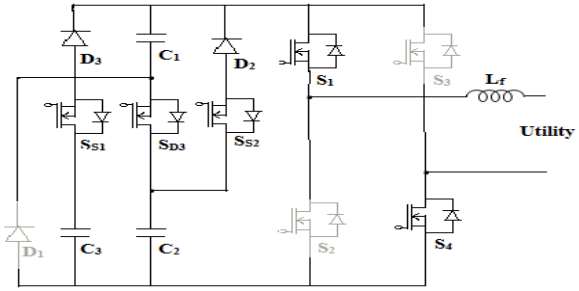
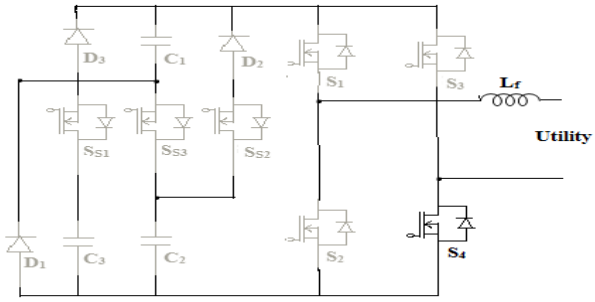


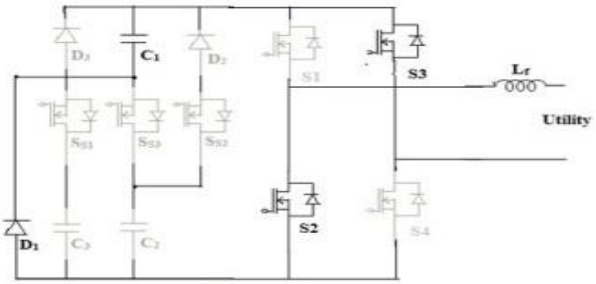
(c)



(d)



(e)



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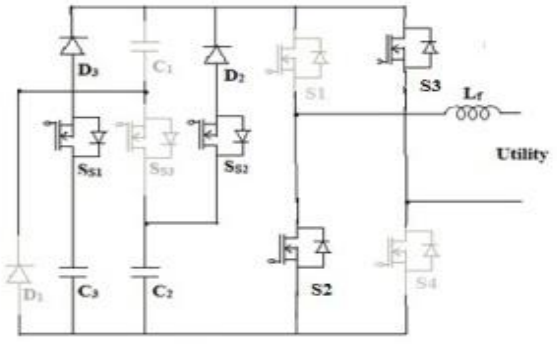
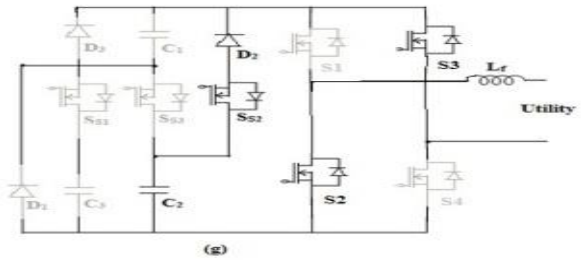
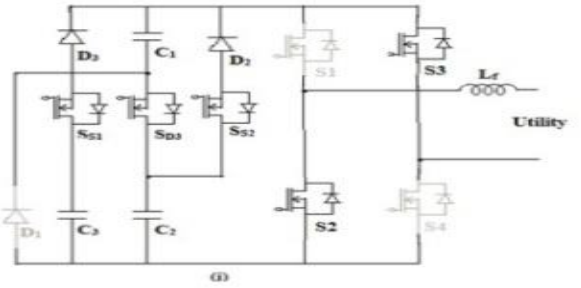


(h)



(g)



(i)

Fig. 3: Different Modes of Operation (A) Mode 1 (B) Mode 2 (C) Mode 3 (D) Mode 4 (E) Mode 5 (F) Mode 6 (G) Mode 7 (H) Mode 8 (I) Mode 9.

4. Simulation analysis and hardware results

The generation of the pulses for the nine level MLI is shown in Figure 4. The Output of the nine level MLI is shown in Figure 5.

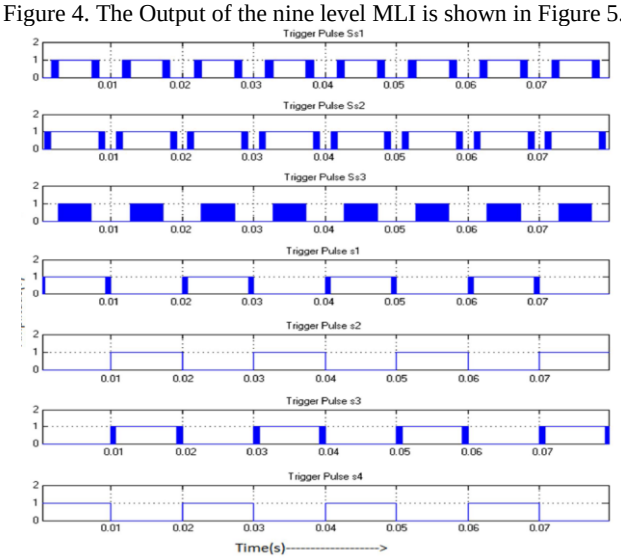


Fig. 4: Inverter PWM Pulses.

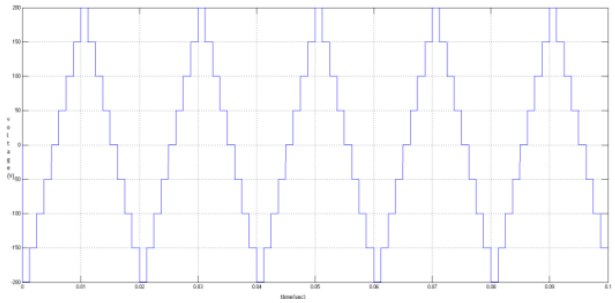


Fig. 5: Inverter Output Voltage.

The hardware implementation of proposed method is shown in the fig.6. The hardware consists of solar PV array, a boost converter circuit, multilevel inverter circuit and a microcontroller. The controller used in the hardware is DSPIC30F2010.

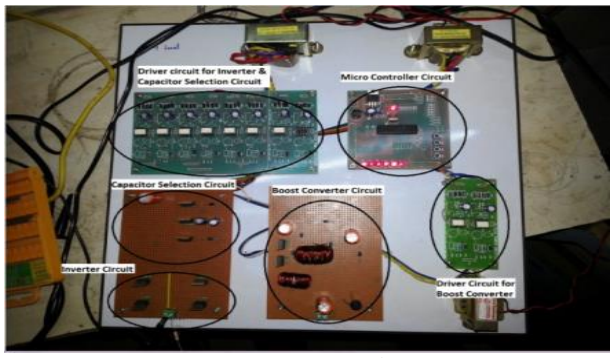


Fig. 6: Hardware Prototype of the System.

The Output obtained from a DSO is shown in figure 7.

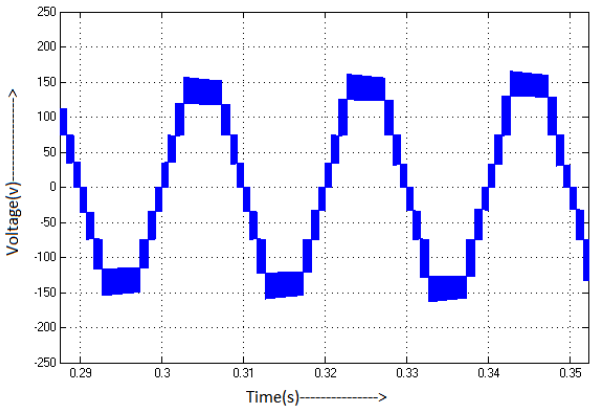


Fig. 7: Obtained Result.

5. Conclusions

A nine level hybrid H-bridge inverter is proposed and the same has been simulated using MATLAB/Simulink. The hardware implementation has also been done. This proposed solar power generation system consists of a dc-dc power converter and a nine-level inverter. This nine-level inverter gives the most simplified circuit configuration with only seven power electronic switches and to generate this nine-level output voltage only one power electronic switch is switched at high frequency at a time. This reduces the switching power loss and improves the power efficiency. The result of Simulation and Hardware validates the choice of topology, components and MPPT controller employed to the system. This work can be further extended by introducing a new topology of converter, novel DC-AC converter, advanced controller schemes like FPGA or advanced PWM techniques like SVPWM to improve performance and integration of the PV system to micro grids.

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