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Research paper

Low-power, low-latency transceiver design using d-TGMS flip-flop for on-chip interconnects

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Abstract

The routers in Network on Chips (NoCs) are used to transmit the data among the Processing Elements (PEs) in the field, and it can be done through transmission links between the routers. Traditionally, the data transmission between the PEs of NoC is carried out by the parallel bus which consumes more power, leads to be complex routing strategies and occupies more area within the field. Instead of parallel bus, serializes and deserialisers are used for serial data transmission, which consumes very less power and area than traditional method. To implement serialiser-deserialiser at the transceiver in the router for on chip communication, a three-level encoding technique is implemented in this design, which eliminates power hungry blocks in earlier works, such as Phase Locked Loops, Feed Forward Equalizers, Decision Feedback Equalizers and the repeaters along the transmission line. In this paper, a low-power transceiver is proposed using modified C^2MOS flip flop and Dynamic TGMS flip flop circuits in order to minimize the delay. The power reduction of 35.683% and the delay reduction of 44.71% were achieved in the proposed transceiver than the NAND gate based D flip flop transceivers.

Keywords: *Network on Chip; Serialiser-Deserialiser; On-Chip Interconnects; D-TGMS; Low Power.*

1. Introduction

This Technology scaling has now reached to nanometer regime, and that gives an opportunity to integrate several numbers of cores on a single chip, called system on Chip (SoC). Most of the current SoCs use a traditional system bus to connect several functional units. Later, a new communication protocol has introduced, named as NoC and several research works are carried out by the designers. The communication process in NoC is done by passing data from one router to another router over the conventional parallel bus for a long distance on-chip. But this conventional bus has become no longer suitable for MPSoCs in terms of power, area and reliability. As said earlier, technology scale down has major impact on gate delay leads to better functional units but not on interconnects, which puts a lot of pressure on wiring complexity and area occupied. Timing errors due to jitter and skew on the parallel bus makes the receiver synchronization very hard, and limits the bandwidth. Also, other factors like cross talk, noise and coupling from adjacent lines limit the bandwidth [1], [2], [3].

One solution to solve the above disadvantages is, replacing the parallel on chip bus by serial transmission links between the PEs through routers. At low frequencies, transmission links between the routers behave like RC interconnect, and its performance has improved by introducing repeaters but leads to larger area and high power. To suppress the area and power, serialization techniques have introduced in NoCs with the Serializer-Deserializer (SerDes) transceiver. This serializing technique allows the data transmission among the PEs at high frequencies to benefit from the characteristics' issues of the transmission line [3] and [4]. Several coding techniques can be used for serial links between transceivers at PEs in NoC to improve the data rate, to eliminate the power-hungry blocks and area. In [17], Manchester coding along with the resistive termination scheme was implemented to reduce voltage swing in the transmission line and to improve the data rate. The PAM-4 and Non-Return to Zero (NRZ) coding schemes are implemented at transmitter and receiver sides of the transmission links for higher data rate. The PAM4 transmitter adopts feed-forward equalizer (FFE) with pre-distortion driver and PAM4 receiver employs linear and decision-feedback equalization together with purely linear CDR. The NRZ transmitter hires a phase aligner before the last multiplexing stage to dynamically line up the data and clock. At the transmitter side, NRZ uses unique method to extract clock signal and data [18]. In [19], 3-level coding technique has used for the same agenda, but the circuit consumed more power due to the current paths in the voltage divider segment.

In this paper, data and the clock signal are multiplexed using a three-level coding technique shown in Figure 1 [1] which helps to reduce the power and unnecessary routing resources in SerDes transmission links. The main advantage of this coding technique is, the clock signal will be extracted from the received data at the receiver side with simple circuitry. Additionally, this coding technique maintains the signal DC level at half of the power-supply independent of the data pattern.

And also this approach takes away the need for equalization circuits and eliminates the need of sending the clock signal using an extra wire or a Clock Data Recovery (CDR) circuit or a Phase Locked Loop (PLL) at the receiver side. As a result, this coding technique reduces area, power consumption and wire usage as compared to other conventional SerDes designs [5], [6], and [7]. This three-level encoding technique is unaffected by jitter effect gathered during signal transmission because the clock signal is extracted from the data. If any timing errors occurred in the re-

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ceived signal that will be reflected in the extracted clock signal, and the data will be sampled appropriately [8]. With these advantages, this paper shows the various implementations and analysis of transceivers for on-chip communications. Recently, the designers have shown their interest on optical interconnects instead of metal wires for on chip wired data transmission, and they are using it because of its efficacy but here we have considered only metal inter connectors [9], [10] and [11].

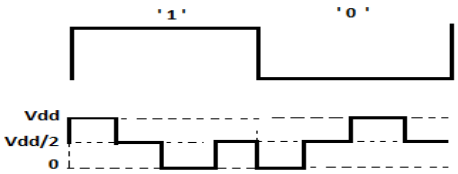


Fig. 1: Three-level coding Technique.

The organization of this paper is as follows: SerDes architecture including the transmitter and receiver is presented in section II. Transmission line and signaling technique is presented in section III .The simulation results is discussed in section IV and finally section V presents the conclusions.

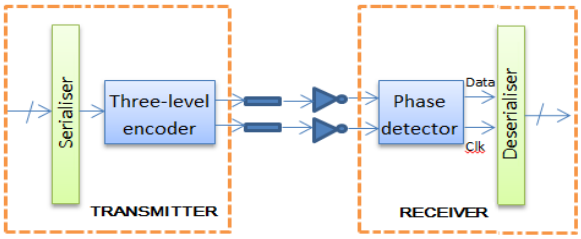


Fig. 2: Block diagram of SerDes Transceiver.

2. SER-DES transceiver

The block diagram of the SerDes Transceiver is shown in Figure 2.The transceiver for on chip communication consists of three modules such as transmitter, receiver and a metal wire between them which is used as a transmission medium that helps to exchange the information among the PEs in a chip. The transmitter part of the transceiver serializes 8-bit and 16-bit parallel input data and generates the corresponding differential three-level code to drive the transmission line between the PEs. In this work, the frequency of input signal to the transceiver is selected as 1.5GHz.

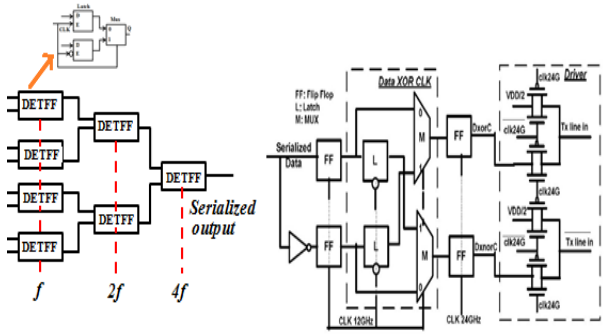


Fig. 3: A) Serialiser; B) Three-Level Encoder.

On the other side, receiver portion receives the transmitted coded-signal via on chip communication wires and the phase detector helps to extract the clock signal and serialized data. Then, clock and extracted data are fed into to the deserialiser which recovers the transmitted 8-bit and 16-bit parallel data.

a) Transmitter

The transmitter consists of a serialiser and a three level encoder with the clock frequency of 24GHz produced by ring oscillator. The serialiser can be implemented in anyway but in this work it is constructed by using Double Edge Triggered Flip-Flop (DETFF). The architecture of serialiser is shown in Figure 3 (a).The DETFF block is realized by the combination a flip-flop, latch and 2:1 mux. Each stage of the serialiser is supplied with three different clock frequencies i.e., 1.5 GHz, 3GHz and 6GHz. The serialised data is then given to the three - level encoder for encoding. The architecture of three-level encoder is shown in Figure 3 (b). The driver will produce the data EXOR clock and the signal will be given to the receiver. For the encoder a 12GHz clock and a 24GHz clock is needed. The D flip flop is designed using NAND gates or using C^{2}MOS [13]. To reduce the power consumption in the transceiver, modified C^{2}MOS (mC^{2}MOS) flip flop is used and to further reduce the power Dynamic TGMS (D-TGMS) flip flop is used.

b) Receiver

The receiver consists of skewed inverter, phase detector and a deserialiser. The phase detector is used to retrieve the data and the clock from the received signal. The phase detector used for the transceiver is as shown in Figure. 4 (a). This phase detector works as a three-state machine, starting with both QA and QB set to '1' representing the reset state. When a '0' pulse is received on A the phase detector will reset QA, and then wait for a pulse on B to set it back to '1'. The same will be done with QB, when the phase detector receives a pulse on B followed by a pulse on A. An SR latches is used to set the output using QA and reset it using QB. An OR gate is used to extract the 12 GHz output clock. The desternalize is simply a shift register used to convert the serial data stream, to 8-bit parallel data at a clock frequency of 1.5 GHz.

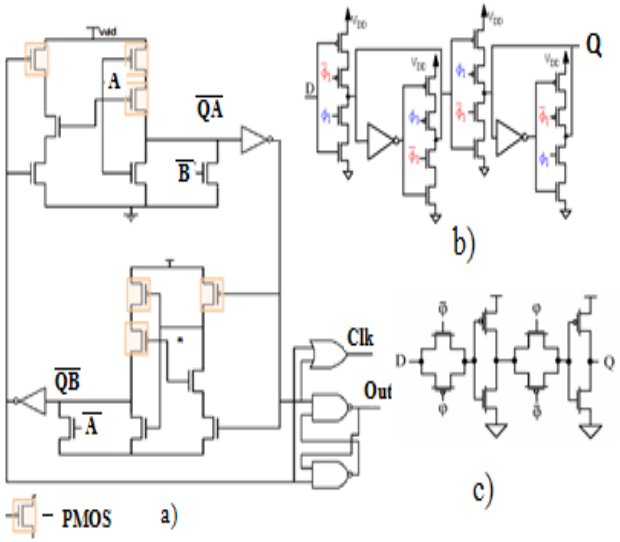


Fig. 4: A) Phase Detector B) Mc^{2}mos Flip Flop C) D-TGMS.

c) MC2MOS flip flop

In this paper, the mC^{2}MOS flip flop is used in serialiser, three-level encoder as well as the de-serialiser to achieve low power consumption. This mC^{2}MOS flipflop is implemented by cascading two complementary latches. This master-slave implementation results in robust flip-flop with a good hold time behavior. The mC^{2}MOS flip flop uses clocked inverters in the circuit for better performance. Also this flip flop has an advantage of insensitivity to overlap of clock signals which causes less power consumption. The mC^{2}MOS flip flop is shown in Figure 4 (b).

d) D-TGMS Flip flop

The D-TGMS flip-flop is considered in this work to achieve high speed and low power but it is sensitive to overlap of the clocks. The D-TGMS flip-flop is constructed with transmission gates and MOS transistors. The performance and comparative analysis is presented by Oskuii and Alvandpour in [14] and its delay is very less compare to other flip-flop topologies. Additionally, energy per transition and clock energy of D-TGMS are very less than NAND, mC^{2}MOS and C^{2}MOS. This flip-flop malfunctions if the clocks overlap for a length of time period. The detailed working function of D-TGMS is presented in [15], [16]. The D-TGMS structure is illustrated in Figure 4 (c).

3. Signaling

At low frequencies on-chip interconnects behave as RC interconnects that introduces a low pass effect to the signal. For higher frequencies, the inductance effect becomes significant that enabling the high frequency signals to travel with the speed of light. These high frequency signals still suffer from attenuation along the line due to the resistance of interconnect. However, this attenuation is constant across different frequency components, so the signal keeps its eye [5].

The random data streams cover the entire frequency spectrum, and low frequency components will introduce large distortion to the signal. To suppress this distortion effect, equalization is required using either a Feed-Forward Equalizer at the transmitter or using a Decision Feed-back Equalizer at the receiver [2], [12]. These equalizers are very complex in design and require more power. So, three-level coding technique is used in this work to avoid using these complex and high power equalizers. Another issue that should be considered especially with high frequency signals is signal reflections, which requires matching the transmission lines to avoid signal distortion. In this design source matching is used instead of matching at the receiver side to make use of the transmission gate resistance and benefit from the signal reflection at the receiver side to double the amplitude of the received signal.

4. Simulation results and discussion

The SerDes transceiver for on chip communication is designed, simulated and synthesized using Cadence virtuoso with 180nm technology. The transceiver is designed with flip flops using NAND gates, flip flops using C^{2}MOS and mC^{2}MOS flip flop and D-TGMS flip flop. The complete integrated block diagram of the transceiver using D-TGMS in Cadence Virtuoso is presented in Figure 5.

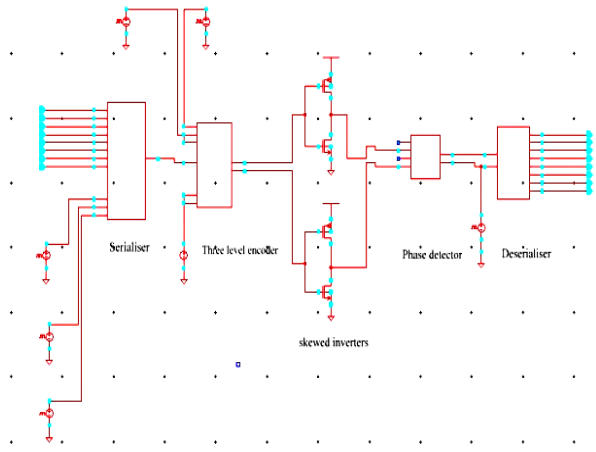


Fig. 5: Complete Transceiver Implementation on Cadence.

The output waveform of the proposed D-TGMS transceiver is shown in Figure 6. According to the results obtained from the experiments, the input data that is given to the transceiver of source PE is correctly transmitted and the same data is received and decoded by the transceiver of destination PE.

Table 1 shows the power consumed by transmitter and receiver modules in the transceiver designed using D-TGMS based flip flops. The summation of each module results in the total power consumed by the transceiver. The power consumption and the delay of transceiver using various flip flops are calculated and tabulated in Table 2. The comparison results show that, the transceiver with NAND based flip flops consumed more power and delay than all other transceivers. The existing transceiver that uses C^{2}MOS flip flop consumes more power than the proposed transceiver that uses mC^{2}MOS and D-TGMS.

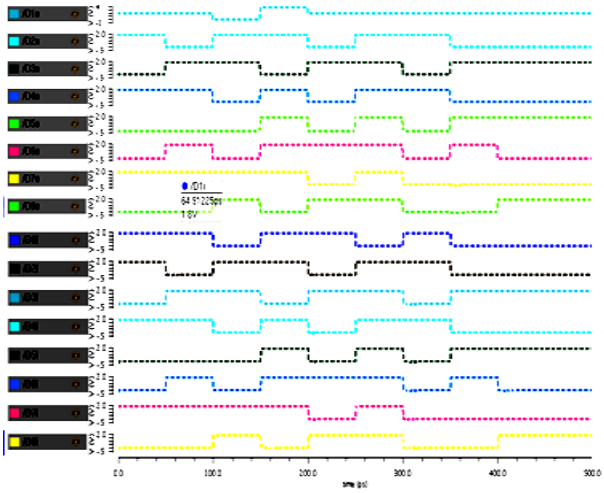


Fig. 6: Complete Output Waveform of the Transceiver.

Table 1: Power Consumption

Module	Component	Power
Tx	Serialiser	7.29mW
	Three level encoder	4.735mW
Rx	Phase Detector	0.59mW
	Deserialiser	0.54mW

Table 2: Design Comparisons

S. No	Transceivers (Flip Flop used)	Power (mW)	Delay (ps)
1.	NAND D	20.155	68.53
2.	C^{2}MOS	16.656	49.68
3.	mC^{2}MOS	14.474	47.76
4.	D-TGMS	12.963	37.89

5. Conclusion

A new signaling technique was used in this paper to design the transceiver that consumes very less power with minimum delay. The proposed transceiver uses mC^{2}MOS flip flop and D-TGMS flip flop in the serialiser, three level encoder and the Deserialiser circuits. The three levels encoding technique enables recovering the clock from the transmitted data at the destination side, which eliminates the need for sending the clock through an extra wire or using power hungry complex blocks, such as PLLs and CDRs. The complete transceiver is implemented using various flip flop topologies. The proposed transceiver circuits using D-TGMS flip flops consumes very less power with minimum delay than other circuit topologies.

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