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***Research paper***

# An efficient high speed, high frequency domino-logic based circuit

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**Abstract**

As the Very Large-Scale Integration (VLSI) techniques are mostly focused on high-speed and low power consumption circuits, various techniques and technologies were investigated to gain these two precious goals. Domino-logic is one of the circuits which is regarded to have high speed, high frequency and low power consumption. This work proposes a Domini logic circuit which has improved PDP compare to the previous one. The suggested circuit was simulated and the attained results show a considerable improvement in circuit's speed in respect with its ancestor. The PDP of the circuit in 90 nm, biased at 1V, has been calculated as 53% approximately improvement. This improvement for PDP in 65 nm, 45 nm and 32 nm are 48%, 47% and 51% respectively.

***Keywords***: *VLSI, Domino Logic, Power, Delay, PDP.*

## 1. Introduction

The CMOS transistors, were introduced in 1976 to reduce the power consumption of their ancestors, the NMOS transistors. This valuable feature has made it possible to integrate the large number of transistors in a single chip. But as the ability of operation at lower power consumption is an essential requirement, the final operational speed of produced chip is also an important factor. In the CMOS logic, each logical function is applied twice; once as pull down circuit and the other as pull up circuit which utilizing nMOS & pMOS transistors, respectively. This procedure will increase the area consumption; enhance the node-capacitance and finally lowering the overall operational speed.

Introduction of high performance dynamic circuits with higher operational speed and less deployed transistors, was a solution to these prescribed unwanted features. But these dynamic CMOS circuits, were also showing some undesirable features such as higher leakage current and less noise immunity which prevent wide utilizing of dynamic circuits. These two parameters are important in low-power and high-performance applications.

Most of suggested circuits have reduced the power consumption at the expense of losing the noise-margin [3, 6]. Domino-logic based circuits were also one of the dynamic designations which were suggested and investigated thoroughly [1, 4, 8]. The chain-like behavior of these logical gates is the main appellation of this family of circuits [12]. Herein a novel & efficient domino-based circuit with better performance, higher speed and lower consumed power will be introduced.

In the following of this paper, we will introduce precedent research in section2 and present the previous and proposed circuit in section3 and 4 respectively. Simulation results are given in section5 and finally section6 concludes the paper.

## 2. Precedent researches

The first decade of 21st century is a new age in which the Domino-Based circuits evolved essentially. Kursan et. al. introduced a novel low fluctuation, low power Domino-based technique which decreased the required power as low as 9.4% and enhanced the noise margin up to 2.6% [1]. Two years later, Ding described the vulnerability against the noise & for the first time classified various techniques to encounter these inherent and unwanted features in detail [2]. Another milestone created again by Kursan in 2006 and by Frustaci in 2007 to minimize the power consumption of 45nm Domino-based circuits [3] & to enhance the noise margin up to 116% with less delay, respectively[4]. A novel Keeper Circuit introduced by David which decreased the short-circuit power dissipation in Domino-based gated up to 70% [5]. In 2009 a novel high speed design introduced by Frustaci which consumes 25% to 30% less power [6]. Massiamo Alioto reviewed the prescribed researches thoroughly and found the dependency of delay variation to keeper transistor & output inverter. Using these facts, he introduced his high speed suggestion in 2012 which reduces the variation of delay for Domino-based logical gates [7].

In the following year, Preetisuda described the difficulties arises from load sharing & introduced his designation, using a CMOS invertor at the output of Domino gate. The suggested circuit shows higher immunity against noise and also lower power consumption in respect with its ancestors [8]. Another suggestion was made by Shiksha as for charge sharing. This suggestion has high speed with better performance using 90nm in OR gates biased at 1V [9]. Also details of Sang-Yun's low swing & low power circuit, which deployed using a pair of pMOS & nMOS transistor to lower the signal's amplitude, was published in 2014 [10]. In same year, Kashyap developed his low power and high speed 90nm Domino circuit based on current mirror which decreased the PDP and en-

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hanced its noise immunity & operational speed [11]. Finally, details of another low power and high speed Domino-based circuit were published by Prasath in 2016. This circuit utilizes an analog current mirror and is analysed in the worst case of leakage current. Due to the reduction of parasitic capacitance in its dynamic node, the circuit speed & performance has been improved [12].

## 3. High speed domino logic circuit

There are four usual distinct variant of Domino-based circuits which are 1- Basic Domino Logic, 2- Footless Domino Logic, 3- Footer Domino Logic and finally 4- High-Speed Domino Logic which will be focused here. Figure 1 illustrates a two-input High Speed Domino-based OR gate, or simply a HSD OR gate [9]. Besides having higher resistance against leakage currents in respect with Footer and Footless Domino circuits, the proposed circuit shows higher operational speed.

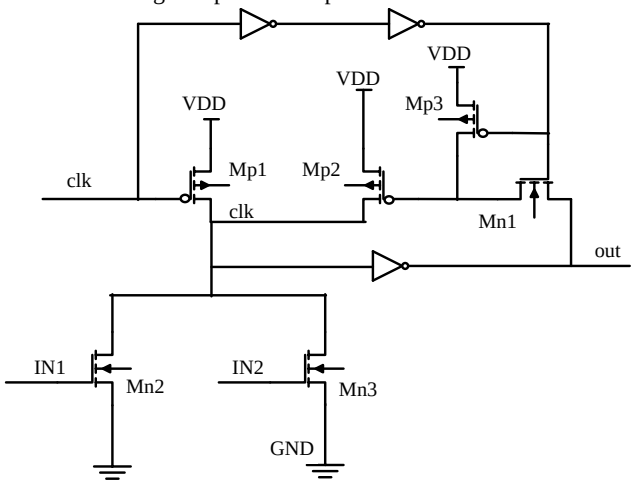



**Fig. 1:** The original high speed domino-logic based circuit

In the presented circuit, Mp2 acts as a keeper for the node named "mid". During its evaluation phase, when the clock changes to its High state, the Mn1 transistor will be delayed to be turned on as long as the inverter gates delay. The reason of this delay is to permit output signal to reach its final stabilized state. Then one of the following listed states will happen:

1- The HIGH state of output node will turn off the MP2 transistor. In this state the "mid" node is zero and would not require any keeper.

$$\text{mid} = 0 \rightarrow \text{out} = 1 \rightarrow \text{no keeper is required} \quad (1)$$

2- Contradictorily, the Mp2 transistor will be turned on and compensates the leakage currents by Mn2 & Mn3 transistors, as long as the output node is in its LOW state. Herein the Mp2 acts as a Keeper and prevents the "mid" node's voltage to drop while the IN1 & IN2 are in their LOW state.

$$\text{mid} = 1 \rightarrow \text{out} = 0 \rightarrow \text{keeper is required} \quad (2)$$

## 4. Proposed high speed domino logic circuit

Figure 2 Illustrates the suggested circuit which enhances the operational speed while lowers the overall power consumption. As it is shown, the MP3 transistor is omitted. This transistor with the Mp2 act as the output signal's keeper. During the evaluation phase, the Mn1 is ON and supplies the Mp2's input current. As the Mp2 acts as a Keeper, and omitting the Mp3 is possible and reduces the size of final circuit while reducing the consumed power.

Omitting the inverters is the other optimization in figure 2. As described, the essential requirement for delay in turning on the Mp2, origins from the states in which the Mp2 should be turned on after the "mid" node reached its stable HIGH state. During the time in which the clock is in its HIGH state, the Mn1 transistor turns on before the Mp2. Afterward, the Mn1's output signal will be delivered to the Mp2's input and turns it on. Thus, the Mp2 turning on is delayed inherently and there is no need for two inverter gates which are placed in series, as shown in Figure 1. Elimination of these two gates results in total size of circuit to be reduced while lowering the power consumption.

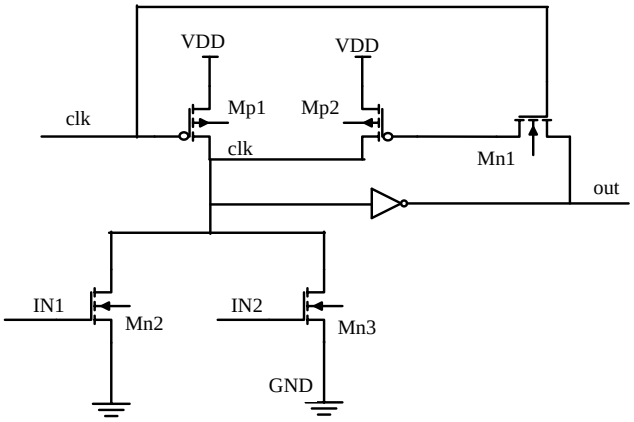



**Fig. 2:** The suggested domino-logic based circuit. The Mp3 transistor and two inverter gates were eliminated.

The suggested circuit of Figure 2, has reduced 5 transistors of the original circuit which results in smaller final size of circuit & lowering its power consumption.

## 5. Simulation results

The prescribed circuit has been simulated precisely, using HSPICE and the final results are shown in tabular format. Table 1 is representing the simulation results for delay, power consumption and PDP in different technologies, ranging from 90 to 32 nm, all at 1V.

The simulation for proposed circuit using 90 nm technology at 5GHz of clock rate showing the similar delay of the original circuit but the power consumption falls to its half and consequently, 51.57% improvement is resulted in PDP. As the clock rate increases to 6 GHz, the delay and the power consumption decreases

**Table 1:** the simulated PDP of various technologies at different frequencies

| TECHNOLOGY | | 90 nm | | | | | | 65 nm | | | | | | 45 nm | | | | | | 32 nm | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CIRCUIT TYPE | | HIGH SPEED DOMINO LOGIC | | | PROPOSED DOMINO LOGIC | | | HIGH SPEED DOMINO LOGIC | | | PROPOSED DOMINO LOGIC | | | HIGH SPEED DOMINO LOGIC | | | PROPOSED DOMINO LOGIC | | | HIGH SPEED DOMINO LOGIC | | | PROPOSED DOMINO LOGIC | | |
| TRANSISTOR (nm) | L | 0.1 | | | 0.1 | | | 0.07 | | | 0.07 | | | 0.05 | | | 0.05 | | | 0.04 | | | 0.04 | | |
| | W | 0.1 | | | 0.1 | | | 0.07 | | | 0.07 | | | 0.05 | | | 0.05 | | | 0.04 | | | 0.04 | | |
| KEEPER (nm) | L | 0.1 | | | 0.1 | | | 0.07 | | | 0.07 | | | 0.05 | | | 0.05 | | | 0.04 | | | 0.04 | | |
| | W | 0.1 | | | 0.1 | | | 0.07 | | | 0.07 | | | 0.05 | | | 0.05 | | | 0.04 | | | 0.04 | | |
| FREQUENCY (GHZ) | CLK | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 | 5 | 6 | 7 |
| | IN1 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 | 0.5 | 0.6 | 0.7 |
| | IN2 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 |
| DELAY (PS) | | 76.81 | 71.83 | 66.21 | 75.95 | 71.22 | 65.47 | 69.50 | 64.91 | 59.29 | 68.52 | 64.06 | 58.55 | 67.09 | 62.68 | 57.14 | 66.47 | 62.16 | 56.56 | 69.97 | 65.55 | 59.86 | 69.61 | 65.10 | 59.64 |
| POWER (mW) | | 15.55 | 16.23 | 16.81 | 8.81 | 9.08 | 9.26 | 12.30 | 12.57 | 12.90 | 7.65 | 7.84 | 8.02 | 8.76 | 8.87 | 9.01 | 5.33 | 5.42 | 5.54 | 5.89 | 5.98 | 6.07 | 3.24 | 3.31 | 3.38 |
| PDP (fJ) | | 1.19 | 1.16 | 1.11 | 0.669 | 0.647 | 0.606 | 0.885 | 0.816 | 0.765 | 0.524 | 0.502 | 0.469 | 0.588 | 0.556 | 0.515 | 0.354 | 0.337 | 0.313 | 0.412 | 0.392 | 0.363 | 0.225 | 0.215 | 0.201 |
| KEEPER (nm) | L | 0.3 | | | 0.3 | | | 0.21 | | | 0.21 | | | 0.15 | | | 0.15 | | | 0.12 | | | 0.12 | | |
| | W | 0.1 | | | 0.1 | | | 0.07 | | | 0.07 | | | 0.05 | | | 0.05 | | | 0.04 | | | 0.04 | | |
| DELAY (PS) | | 81.19 | 76.26 | 70.59 | 80.23 | 75.14 | 69.36 | 72.08 | 67.57 | 61.90 | 71.22 | 66.44 | 61.08 | 68.80 | 64.37 | 58.82 | 68.18 | 63.83 | 58.07 | 71.71 | 67.19 | 61.64 | 71.03 | 66.66 | 61.12 |
| POWER (mW) | | 15.67 | 16.29 | 16.86 | 7.67 | 7.73 | 7.83 | 12.35 | 12.60 | 12.90 | 6.61 | 6.60 | 6.71 | 8.80 | 8.87 | 9.01 | 4.67 | 4.73 | 4.80 | 5.92 | 5.98 | 6.07 | 2.96 | 2.94 | 2.99 |
| PDP (fJ) | | 1.27 | 1.24 | 1.19 | 0.615 | 0.581 | 0.543 | 0.890 | 0.851 | 0.798 | 0.471 | 0.438 | 0.410 | 0.605 | 0.571 | 0.530 | 0.324 | 0.302 | 0.279 | 0.424 | 0.402 | 0.374 | 0.210 | 0.196 | 0.182 |
| IMPROVEMENT (%) | | -- | -- | -- | 51.57 | 53.14 | 54.36 | -- | -- | -- | 47.07 | 48.53 | 48.62 | -- | -- | -- | 46.44 | 47.11 | 47.35 | -- | -- | -- | 50.47 | 51.24 | 51.33 |
| AVERAGE(%) | | -- | -- | -- | 53.02 | | | -- | -- | -- | 48.07 | | | -- | -- | -- | 46.96 | | | -- | -- | -- | 51.01 | | |

a little and the final PDP improvement reaches to 53.14% approximately. Finally, at clock rate as high as 7 GHz, the final PDP decreases 54.36% compare to the original circuit.
While we migrated to 65nm devices, the PDP improvement of the suggested circuit varied to 47.07%, 48.53% and 48.62% while the clock rates are 5GHz, 6GHz and 7GHz, respectively.
The 45 and 32nm technologies, show verifier results in previous technologies, especially at higher frequencies. The best resulted PDP for suggested circuit are 47.35% and 51.33% at 7GHz for these two technologies, respectively. Figure 3 represent the PDP improvement in various frequencies when the keeper transistor channel length is minimum feature size. As seen, 90nm shows better improvement compare to other technologies. However, the value of PDP in 32mn is minimum. As it is 0.182fJ in 32nm which is approximately half of PDP value in 45nm. As illustrated, The PDP value decreases as the technology is scaled down.

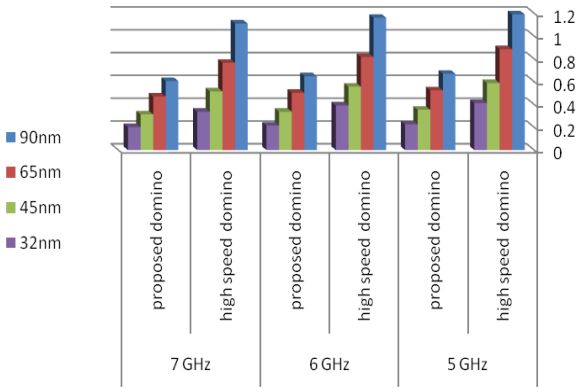



**Fig. 3:** PDP comparison between high speed domino logic and proposed domino logic in different technologies when the keeper transistor channel length is minimum size.

For more detailed and better insight into the problem, the simulation have been done twice; once while the length of keeper transistor adjusted to its practically minimum size and Once it tripled to limit the injected current of keeper transistor into the "mid" node. As depicted in Figure 4, the calculated PDP is increased in the original circuit as the keeper transistor length is increased. However, in the proposed circuit, the value of PDP is improved by tripling the length of keeper transistor. Thus, this is the other advantage of our proposed circuit.

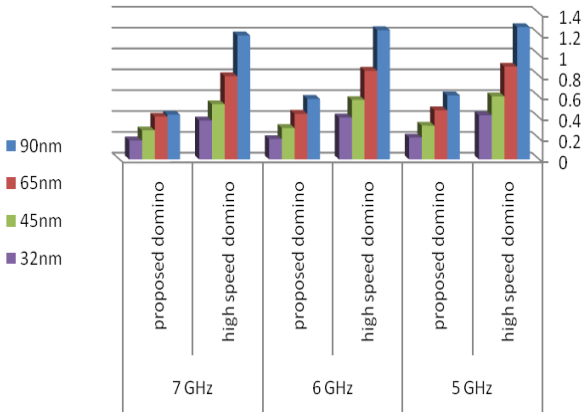



**Fig. 4:** PDP comparison between high speed domino logic and proposed domino logic in different technologies when the keeper transistor channel length is triple the minimum size.

To check the operational status of suggested circuit at higher frequencies, the simulation at these frequencies have been done in stepwise manner while the quality of circuit's output considered continually. Figure 5 illustrates the frequency response of high speed domino versus suggested circuit. As seen, the output voltage has not been dropped till 10GHz. Also, the bandwidth of the proposed circuit is 13GHz which is more than the bandwidth of high speed domino logic (12GHz).

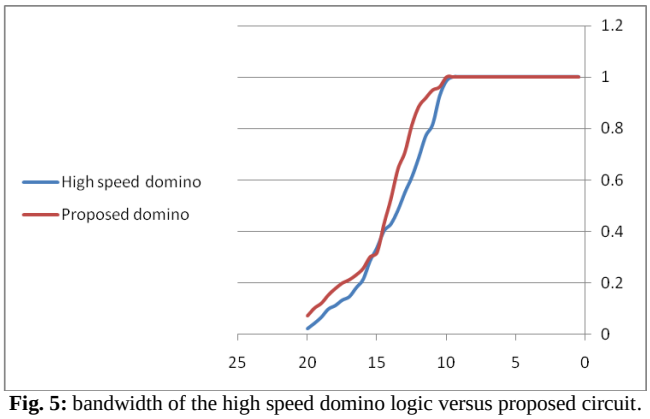



**Fig. 5:** bandwidth of the high speed domino logic versus proposed circuit.

We also calculate the average improvement of PDP in the mentioned technologies. As seen in table 1, the average PDP improvement in 90nm is about 53.02% and for 65nm, 45nm & 32nm is 48.07, 46.96% & 51.01% respectively. As seen in Table 1 & as described above, the resulted PDPs of 32nm in various frequencies are the lowest, as it is nearly 50% & 33% of the PDP in 65nm and 90nm technologies, respectively. Also in 90nm, the suggested circuits shows faster fall in PDP, among all other ones.

## 6. Conclusions

This paper introduced a variant of high speed Domino-Logic based circuits to improve its PDP. The suggested and original circuits were deployed and simulated, using HSPICE. An average improvement of 53.02% in PDP for 90nm and also 48.07%, 46.96% & 51.01% of improvement in PDP for 65nm, 45nm & 32nm variants were found, respectively. In the original circuit, increment in the length of keeper transistor will worsen the PDP. In contrast, the PDP of tripled length keeper transistor of suggested circuit is improved, which is a remarkable feature of it.
Finally the maximum stable operational frequency of suggested circuit is 10 GHz with fractional bandwidth of 13 GHz. This feature beside its low power consumption, categorized the suggested circuit as high frequency one.

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