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Research paper

Gate work function variability-dependent short channel effects in nanoscale double gate finFETs: an in-depth comparative analysis

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Abstract

We explored the impact of gate work-function variations on Short Channel Effects (SCEs) in nanoscale Double Gate FinFETs utilizing GaAs, GaSb, GaN, and Si as semiconductor channel materials. The analysis is carried out using PADRE Simulator. Critical performance parameters examined are Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage Roll-off, On-Current and Transconductance. The results show that GaAs-FinFET excels in terms of DIBL and threshold voltage and on-current. GaN-FinFET shows higher superiority in terms of SS. While GaAs and GaN outperform the other two in terms of transconductance. These findings underscore the significance of work-function variability in enhancing nanoscale electronic device performance and developing semiconductor technology.

Keywords: *Gate Work-Function; PADRE Simulator; Semiconductor Technology; Threshold Voltage; Transconductance*

1. Introduction

A number of challenges such as short channel effects (SCEs) to device performance and difficulties with manufacturing are caused by the drastic reduction in transistor size, that is, in traditional Metal Oxide Semiconductors (MOSFETs) [1-3]. To overcome these challenges due to continuous scaling, the double gate FinFET has emerged as a potential approach [4-5]. This FinFET was made possible by the unrelenting pursuit of higher levels of integration with lower power requirements, enabling "to manufacture faster, simpler and smaller ones" as a successor to conventional planar transistors [5]. These devices have performed admirably in significantly scaled device configurations. FinFET technology has attracted many device designers and researchers who are seeking for effective structural and process variables in these devices, resulting in a plethora of research on such new device architectures. [6]. The search for more effective and potent electrical devices never stops in the ever-evolving field of semiconductor technology. Think about a scenario in which our smartphones operate faster, use less energy, and pack even more capability into smaller places. Understanding short channel effects and the significance of work function variability at a fundamental level is essential for realizing this aim.

The usage of metal gates to modify threshold voltage in nanoscale FinFETs was investigated in [6]. The study found that altering the metal gate work-function effectively regulates the threshold voltage, eliminating short channel effects and improving device performance. However, raising the gate work-function increases several characteristics such as DIBL, SS, off-current, and on/off current ratio while decreasing device on-current. In [7], impact of work function variation and line-edge roughness on TFET and FinFET Devices was studied. The authors investigated 32-bit carry-lookahead adder (CLA) circuits in the near-threshold region, III-V homo-junction tunnel FET (TFET) and FinFET devices, and these components together. Through simulations, they examined intrinsic device changes such as work function variation (WFV) and fin line-edge roughness (fin LER). Due to enhanced on-current and gate capacitance uniformity, the results revealed that TFETs performed better than FinFETs in low-voltage delay and power-delay products.

Another research by Rathore & Rana [8] explored the effects of work function variation (WFV) in 14 nm metal-gate FinFET architectures by employing 3-dimensional device and circuit simulations. The stability of a 6-T SRAM cell was examined, as well as the influence of WFV on FinFET properties. The results showed that WFV can significantly reduce performance at CMOS technology nodes with a sub-20 nm process, creating difficulties for device scaling. Ko et al. in [9] utilized TCAD simulations to look into work function variation (WFV) in 3-dimensional stacked nanowire FET (NWFET) and FinFET devices for 6-T SRAM cells in 5 nm gate-all-around (GAA) . The results demonstrated that, compared to FinFETs, NWFETs offered better gate control but are more vulnerable to WFV because of their smaller gate area. Researchers in [10] investigated how the orientation of the metal-gate granularity affects analog performance in high-k/metal-gate junction-less (JL) FinFETs and gate-all-around (GAA) nanowire MOSFETs.

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The figures-of-merit (FOM) of computer-aided design simulations were compared in linear and saturated areas, demonstrating large FOM fluctuations due to work-function variation (WFV). JL FinFETs suffered more than GAA NWFETs. Authors in [11] examined the effects of total ionizing exposure on SOI and bulk linear gate work-function modulated P-FinFET devices. The research shows that in radiation-prone conditions, both devices exhibit improved I_{OFF} and decreased subthreshold swing, indicating improved electrostatic integrity. In comparison to a bulk device, the suggested SOI device showed superior radiation resilience. To the best of our knowledge, no comparative study of the influence of work-function variations on short channel effects in nanoscale double gate FinFETs using compound semiconductors as channel materials has been carried out yet. Short channel effects offer a major challenge in the shrinking of electronic devices, thus resolving this issue is critical to technological growth.

This work is aimed at carrying out a comprehensive analysis of the impact of gate work-function variation on short channel effects in nanoscale double gate FinFETs utilizing channel materials like GaAs, GaSb, GaN, and Si. The study focuses on crucial short channel restrictions, which have a significant influence on the operation of nanoscale electronic devices. These restrictions include threshold voltage roll-off, DIBL, and SS. Investigations will also be conducted on the on-current and transconductance properties. The study will be carried out using PADRE Simulator, a well-known tool for semiconductor device modeling and simulation.

1.1. Device structure

Figure 1 depicts a two-dimensional representation of the FinFET device structure utilized in the current simulation study, as well as the different device parameters that were used in the simulation.

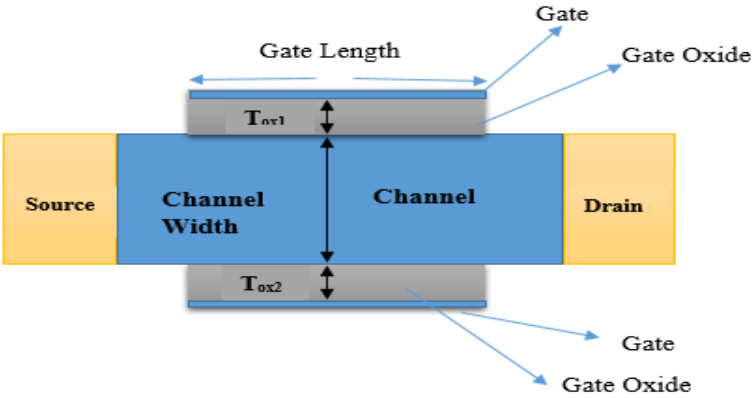


Fig. 1: Two-Dimensional Double Gate Finfet [12] [13]

The device structure of an n-channel double gate FinFET is shown in Fig. 1. The structure has important parts such the source, drain, gate length (also referred to as channel length), and channel width (also referred to as fin width or fin thickness). Before making the gate contact, the oxide is placed on the top surface of the fin, both on the side walls, and both sides of the side walls. Tox1 and Tox2 stand for the thickness of the side wall oxide [12],[14].

2. Method

The PADRE Simulator has the ability to create usable FET curves, which are very valuable for engineers when describing the basic physics of FETs. Additionally, it can offer self-consistent answers to the equations of poison and drift-diffusion [15],[16]. The device was simulated using four distinct channel materials: GaAs, GaSb, GaN, and Si. The work-function of the gate has been altered from 4.4Ev to 5Ev. During the simulation, an oxide thickness of 2 nm, a gate length of 45 nm, and a channel width of 10 nm were selected. During the simulation, the channel doping concentration was held constant at 1×10^{16} cm^{-3}, and the drain/source was fixed at 1×10^{19} cm^{-3}. The drain bias was set between 0.05 V and 1 V, whereas the gate bias was set between 0 V and 1 V. Table 1 contains these parameters.

Table 1: Parameter Specifications

Parameter	Value
Work-function	(4.4, 4.5, 4.6, 4.7, 4.8. 4.9, 5) eV
Oxide Thickness	2 nm
Gate Length	45 nm
Channel Width	10 nm
Channel Doping Concentration	1×10^{16} cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 1.0 V
Gate Bias	0 V to 1 V

3. Results and discussion

The results of the influence of the gate work-function variability on the short channel effects in nanoscale double gate FinFETs for various semiconductor channel materials are presented here.

3.1. Work-function variation vs DIBL

The difference in threshold voltage occurs when the drain voltage is raised from 0.01 V to 0.05 V. This is known as Drain Induced Barrier Lowering (DIBL) [13]. The DIBL value can be determined using the equation [6] [17]:

$$\text{DIBL}\left(\frac{\text{mV}}{\text{V}}\right) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (1)$$

Where V_{TH} is denotes threshold voltage and V_{DS} denotes drain-source voltage.
The influence of work-function variation on the DIBL of four FinFETs, GaAs, GaSb, GaN, and Si, is shown in Fig. 2. The figure shows that the DIBL in each FinFET is constant for a range of work-function values used. This demonstrates unequivocally that gate work-function has no discernible impact on the DIBL. It is clear from the context of the investigated FinFETs that the performance of the GaAs-FinFET is superior to that of the other three FinFETs. This is especially noteworthy when considering Drain-Induced Barrier Lowering (DIBL), where the GaAs-FinFET continuously maintains the lowest DIBL value of 4.38 mV/V across the range of the work-function as observed in Fig. 2. This result highlights how superior the GaAs-FinFET is in efficiency and effectiveness when compared to the other three FinFETs. Reduced DIBL can limit the short channel effects (SCEs), maintain correct device operating frequency, and enhance threshold voltage roll-off characteristics [12].

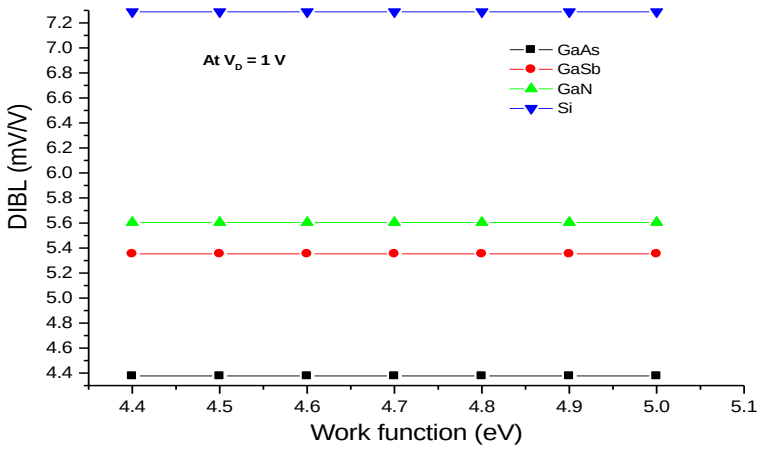


Fig. 2: DIBL vs Work-Function.

3.2. Work-function variation vs SS

The primary factor in determining the leakage current, holding time in dynamic circuits. For a Multigate Field Effect Transistor, the SS parameter typically has a value of 60 mV/dec. The SS can be represented by the formula [16]:

$$\text{SS (mV/ dec)} = \frac{\text{d } V_{GS}}{\text{d } (\log_{10} I_{DS}} \quad (2)$$

where V_{Gs} denotes gate-source voltage and I_{DS} denotes drain-source current.
Fig. 3 shows how the subthreshold properties of GaAs, GaSb, GaN, and Si FinFETs are affected by work function variation. The figure shows that over the range of the work-function taken into consideration, all the FinFETs maintain almost similar SS properties. GaN-FinFET, in contrast to the other three FinFETs, excels at the work-function of 4.4 eV as it exhibits SS value of 0 mV/dec. Zero threshold swing (ZTS) is an ideal scenario in which the threshold swing approaches zero. In other words, it suggests that the transistor can switch between the off and on states with little energy consumption and voltage change at the gate. Achieving ZTS in FinFETs is an essential goal as it allows for more efficient operation and helps minimize power consumption in electronic devices.

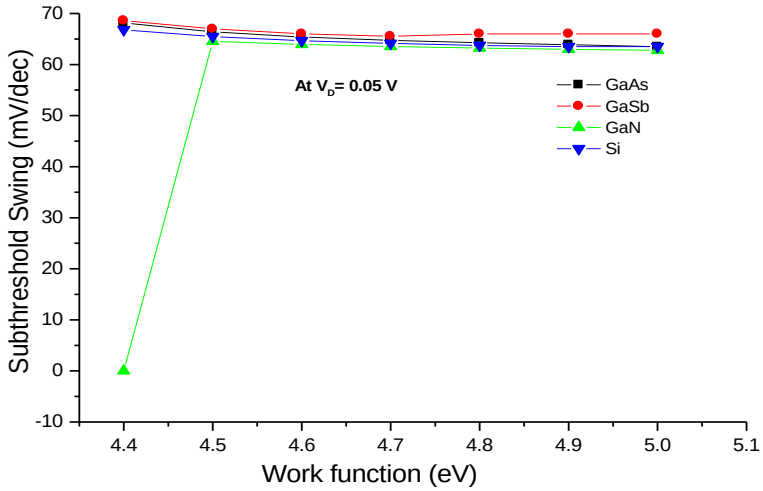


Fig. 3: Subthreshold Swing vs Work-Function.

3.3. Work-function variation vs threshold voltage

Evaluating a device's threshold voltage is an important step in establishing its potential as a viable channel material for switching applications. The threshold voltage is the least gate voltage needed to provide a conduction route between the source and the drain [18]. The threshold voltage of a fin field-effect transistor (FinFET) device can be determined using [6]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3)$$

Where Q_{SS} denotes charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential.

Fig. 4 depicts the influence of work-function variation on the threshold voltage properties of GaAs, GaSb, GaN, and Si FinFETs. It is evident from the figure that the threshold voltage increases steadily as the work-function increases. The figure also demonstrates that GaAs-FinFET excels in terms of the threshold voltage characteristics as it shows lowest threshold voltage of 0.27 V. This behavior projects it to be useful in applications where faster switching effect is required.

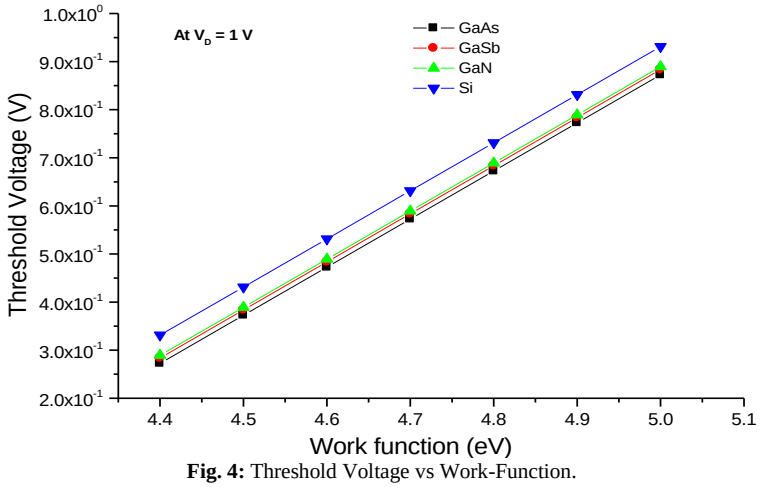


Fig. 4: Threshold Voltage vs Work-Function.

3.4. Work-function variation vs on-current

Fig. 5 shows the influence of work-function variation on the drive current of FinFETs for different semiconductor channel materials; GaAs, GaSb, GaN and Si. The graph clearly shows that each FinFET's on-current remains constant between 4.4 eV and 4.8 eV work-function values. Notably, the GaAs-FinFET displays the highest value of 2.35×10^{-4} A/μm within this range. This indicates that GaAs-FinFET is better than the other three FinFETs in terms of on-current. The figure also shows that for all four FinFETs, on-current decreases when the work-function increases beyond 4.8 eV. In FinFET devices, a higher on-current can result in superior performance, faster switching times, faster circuit speeds, less propagation delay, better power efficiency, lower noise margins, and more flexibility in design.

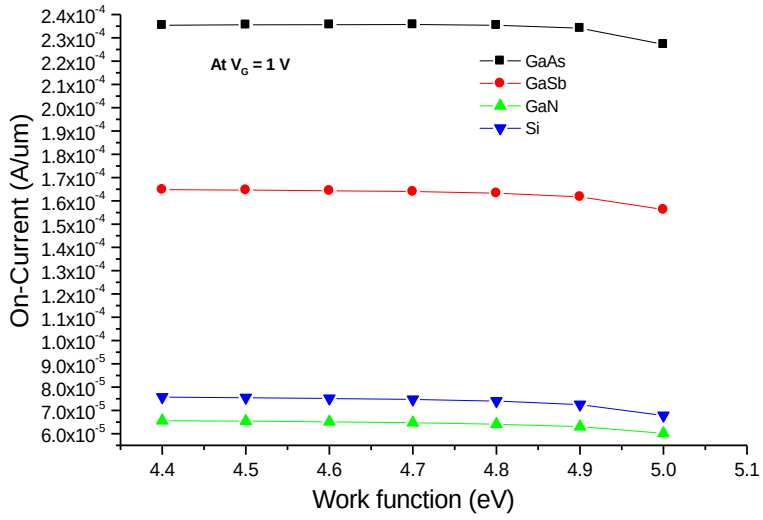


Fig. 5: On-Current vs Work-Function.

3.5. Work-function variation vs transconductance

The transconductance measures how the drain current varies in response to changes in the gate-source voltage while keeping the drain-source voltage unchanged. This parameter can be calculated using equation [15]:

$$g_m = \frac{dI_D}{dV_{GS}} \quad (4)$$

where I_D denotes the drain current and V_{GS} denotes the gate-source voltage

Fig. 6 shows the effect of work-function variation on the transconductance of FinFET using GaAs, GaSb, GaN, and Si as channel materials. The figure illustrates that transconductance is constant for all four FinFETs in the 4.5 to 4.6 eV work-function range. This trend continues up to 5 eV for Si-FinFET. It can be observed from the figure that GaAs and GaN FinFETs show higher transconductance of 1.53×10^{-5} S/μm than the other two FinFETs at the work-function of 4.4 eV. GaAs and GaN FinFETs are thus superior compared to the other two

FinFETs in terms of transconductance. Higher drive currents, reduced power consumption, increased noise immunity, and compact design are only a few benefits of higher transconductance in FinFET devices. These advantages help semiconductor technology continue to improve, making finFET devices more efficient.

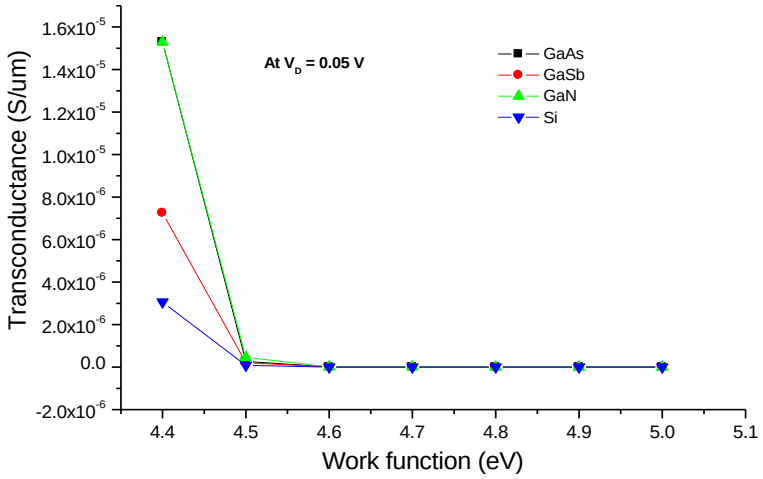


Fig. 6: Transconductance vs Gate Work Function.

4. Conclusion

We investigated the effect of work function variations on the performance of nanoscale Double Gate FinFETs in terms of short channel effects, using various semiconductor channel materials such as GaAs, GaSb, GaN, and Si. DIBL, SS, Threshold Voltage Roll-off, On-Current, and Transconductance are the key performance metrics investigated. The results showed various benefits and capabilities associated with certain semiconductor materials. GaAs-FinFET was found to have exhibited excellent properties in terms of DIBL, threshold voltage and on-current, demonstrating their potential applicability for high-performance electronic devices. On the other hand, GaN-FinFET outperformed other FinFETs in terms of SS, suggesting that they are useful in applications requiring low-power operation and efficient switching. Furthermore, in terms of transconductance, GaAs and GaN FinFETs surpassed the other FinFETs, underscoring their importance in the development of advanced semiconductor technologies that demand high-speed and high-gain amplification. These discoveries are crucial as they increase our understanding of how gate work function variations impact nanoscale Double Gate FinFET performance, assist in material selection, and offer strategies to improve the performance of advanced semiconductor devices. They address critical difficulties in semiconductor technology and give significant insights for future developments. Further research can be carried out by investigating the power efficiency of Double Gate FinFETs under various work-function variations.

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