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Research paper

Design of Low-Power 2.5 GHz Integer-N Frequency Synthesizer

M. A. Raheem[1]*, Subhanvali Shaik 2, Abdul Majid 3, Suhaib ur Rehman 4, Syed Arif [5]

[1,2]*Assistant Professor, MuffakhamJah College of Engg. and Tech. , Banjara Hills, Hyd, TS.*
[3,4,5]*Students, MuffakhamJah College of Engg. and Tech. , Banjara Hills, Hyd, TS.*
**Corresponding author E-mail:abdulraheem@ieee.org*

Abstract

In this context a low powered, N-Integral frequency synthesizer of 2.5GHz for RF applications is proposed. Corroboration of concept is established by implementing the design of frequency synthesizer circuit in 180nm CMOS technology. The frequency generated by the synthesizer ranges from 2.4GHz to 2.5GHz and power consumption is 5.54mW from a 1.8V power supply. This synthesizer is found to have a phase noise of -95.15dBc/Hz at an offset of 1MHz from the carrier.

Keywords*: Frequency synthesizer; LC oscillator; phase locked loop.*

1. Introduction

The growth in wireless communication is unprecedented due to new applications which demand small-size, low-cost and long-battery-life. Inorder to provide smaller-sized and lower-cost solution, many efforts are being made to integrate whole of the system in a low-cost technology. The improvement of technology and design is driving the cost down. The application area of wireless communication includes WLAN, GPS, cordless phones, smart phones, remote control appliances etc.

VLSI designers always endeavor to provide less area, reduced cost and highest performance. Power consideration was of secondary concern. In contrast, power is of primary concern these days due to remarkable growth and success in personal computing devices and wireless communication system which demand agile computations and tortuous functionality with power consumption to be low.

Phase locked loop (PLL) is the decisive building block of all electronic systems for clock generation and atuning, signal recovery from noisy channel, frequency synthesizer, communication systems and FPGA's. Hence, designing the components of PLL with optimized power consumption is imperative.

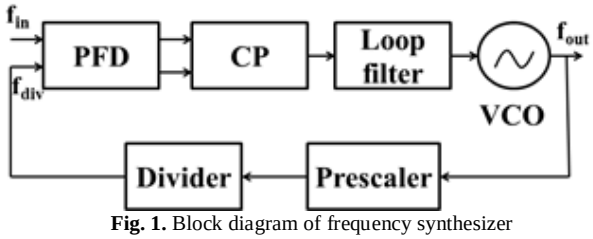


Fig. 1. Block diagram of frequency synthesizer

2. Proposed Frequency Synthesizer Architecture

Fig. 1 depicts the architecture of our frequency synthesizer along with prescaler and divider. It is a negative feedback system. The PFD, CP, VCO and loop filter are in the feed forward path. The prescaler and the frequency divider form the feedback path.

The PFD takes two inputs signals and reckons the difference in their phase. The PFD output is given to the charge pump and loop filter which varies the control voltage of the VCO, thereby varying the frequency of the synthesizer. The VCO frequency keeps varying till it is in phase with the input signal and that condition is known as the phase-lock condition. The output signal from VCO is given as feedback to PFD via divider. This divider divides the VCO frequency by a certain amount such that its output will be of the same frequency as the input signal. Under the phase-lock condition, the VCO output will be N-multiples of the input frequency, where N is the division ratio of the divider. Therefore, by varying the value of N, we can achieve different frequencies from a single input Signal.

3. Circuit Design

3.1. Voltage Controlled Oscillator

One of the most critical building blocks in the PLLor frequency synthesizer is the VCO. Generally, the oscillator operates at the highest frequency with a dominant phase noise at frequency offsets way above the synthesizer's loop bandwidth. In sharp contrast to the ring oscillator, an LC tuned VCO [1] is used to achieve oscillation at high frequency with low phase noise [2]. On the other hand, on-chip inductors are plagued with low Q factor, narrow frequency tuning range, increased silicon and high power consumption

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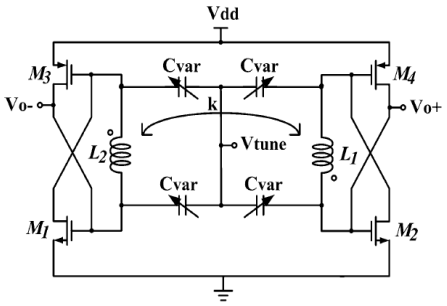


Fig. 2. Voltage Controlled Oscillator (VCO)

Fig. 2 shows the LC VCO that has been implemented. In the proposed VCO, the Varactors are composed in balanced topology and the inductors are configured in a transformer structure in order to increase the Q-factor and to force the differential outputs.

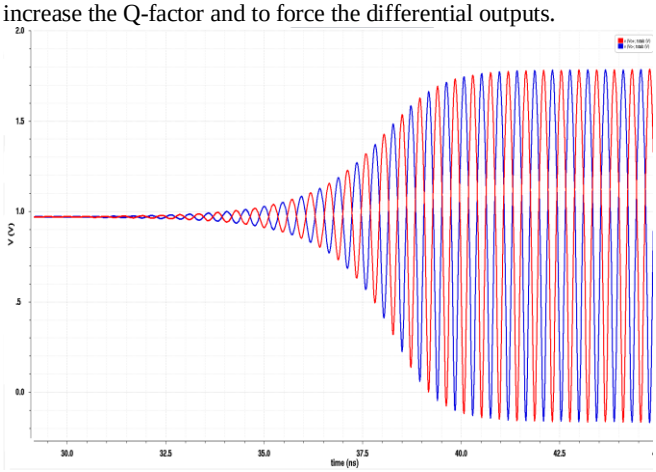


Fig. 3. Differential outputs of the LC VCO

Fig. 3 shows the simulated output transients of the proposed VCO with the transformer coupling; the VCO generates two differential outputs. The phase noise can be improved by using a transformer based LC tank VCO which has a high Q. Frequency tuning can be done by using Accumulation-mode MOS varactors. The proposed VCO is shown in Figure 4 as implemented in the frequency synthesizer. The oscillation frequency of the VCO is equal to

$$f_0 = \frac{1}{2\pi\sqrt{L_2(1+p)C_{vnet}}} \quad (1)$$

Where C_{vnet} is the net capacitance; it is a function of tuning voltage Vtune. p is the transformer coupling coefficient.

The LC VCO used in this design gives a fairly linear variation between the VCO control voltage and the output frequency. The control voltage vs. output frequency characteristics of the VCO can be seen in figure 5.

3.2. Pre - Scaler and programmable divider

It is very important to include the divider capable of operating at high frequency signal of the VCO, in the feedback to track the VCO signal and to lock the frequency synthesizer. The high frequency divider consumes maximum power.

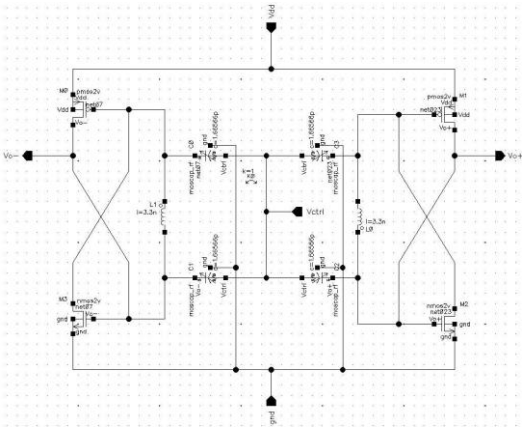


Fig. 4. Schematic of Voltage Controlled Oscillator

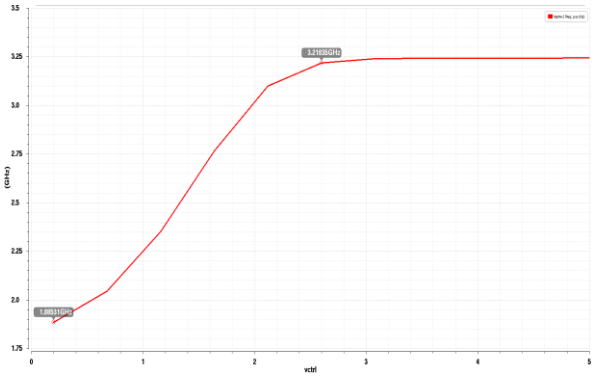


Fig. 5. VCO output frequency vs. control voltage

In order to keep the power consumption lower, design of the divider is very crucial. After few initial dividers, signal frequency goes low and automatically reduces the power consumption at these stages. Hence, this paper implements a split topology for the high frequency and low frequency dividers. A prescaler is used after the VCO in the feedback path for dividing the high frequency output of the VCO. The prescaler is designed using different logic blocks which can operate at high frequencies. This prescaler divides the VCO frequency to a lower value which can be given as an input to the programmable divider which is designed using conventional digital logic blocks which do not operate properly at high frequencies. The output of this divider is then given as feedback to the PFD which compares it with the input signal and generates the corresponding signal depending on whether the signals are in-phase or out of phase.

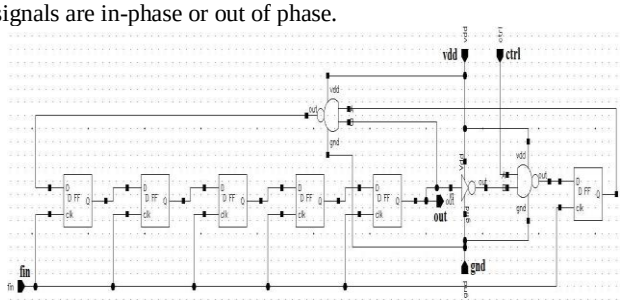


Fig. 6. Schematic of 10/11 prescaler

Fig. 6 shows the prescaler that has been implemented in the frequency synthesizer. A divide by 10/11 prescaler has been used. A high value prescaler has been used because it reduces the VCO frequency to a lower value, which decreases the requirement for the complexity of the programmable divider.

The prescaler is followed by the programmable divider which is depicted in fig. 7, consisting two blocks: a duty cycle improved circuit (DCIC)and aprogrammable counter (PC). This programmable divider generates a divided output signal which has 50% duty cycle.

The signal F_{in} is the input signal and the signal IN [1:N] is the binary input divisor which is used to vary the division ratio of the divider. Q[1:N-1] is the internal signal which is the binary counting output of the PC.

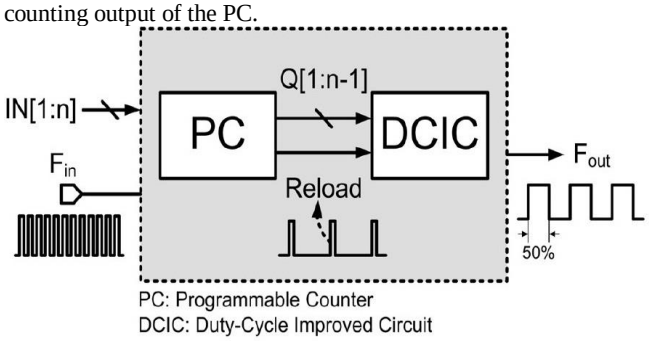


Fig. 7. Programmable divider

Reload is the output signal of PC which is also used to reload the complete divider. F_{out} is the divided output signal of the programmable divider. To explain the operating principle of the divider, a timing diagram is shown in fig. 8 for the condition when the input divisor is 6.

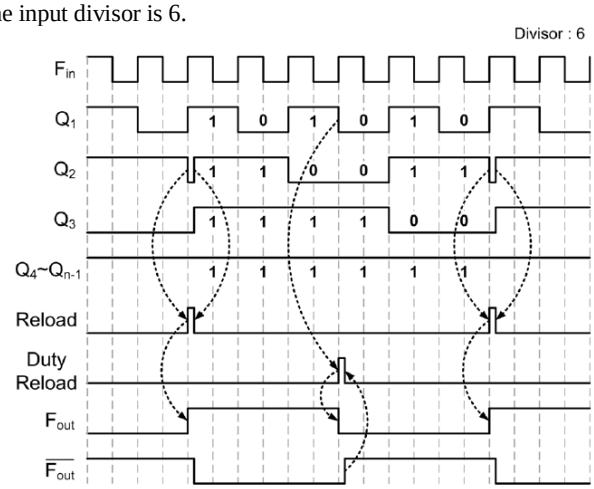


Fig. 8. Timing diagram of the programmable divider

3.3. Phase Frequency Detector (PFD)

Basically, the PFD is also a sequential phase detector, with an extra feature that it has a memory function.It can not only work as a phase detector but also afrequency detector. A typical circuit implementation of a PFD is shown in fig. 9.

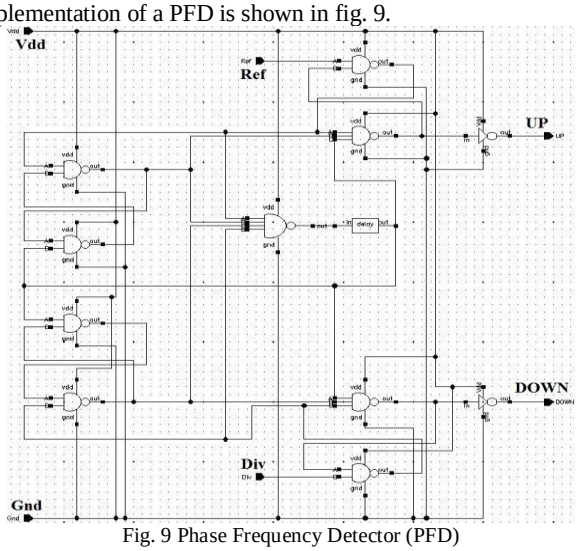
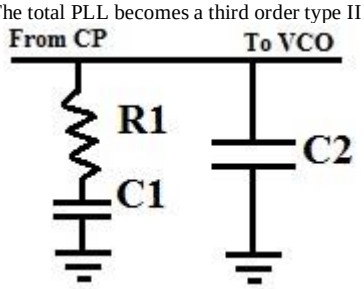


Fig. 9 Phase Frequency Detector (PFD)

3.4 Loop Filter (LF)

Second order passive loop filter, as shown in Fig. 10, has been implemented. The total PLL becomes a third order type II system.



Second order loop filter

Transfer function of second order loop filter is

$$Z(s) = \frac{1}{C_1+C_2}.\frac{(1+sR_1C_1)}{s\left(1+s\frac{R_2C_1C_2}{C_1+C_2}\right)} \quad (2)$$

Time constants for zero and pole are

$T_z = R_1.C_1$and $T_p = \frac{R_1C_1C_2}{C_1+C_2}$, respectively.

The complete open loop transfer function is

$$G(s)|_{s=j\omega} = \frac{I_{CP}}{2\pi}.\frac{K_{VCO}}{j\omega}.\left\{\frac{1}{C_1+C_2}.\frac{(1+j\omega T_z}{j\omega(1+j\omega T_p)}\right\}.\frac{1}{N} \quad (3)$$

Where I_{CP} is the charge pump current, K_{VCO} is the VCO gain, N is division ratio. Expression for phase of G(jω) is

$$\phi(\omega) = \tan^{-1}(\omega T_z) - \tan^{-1}(\omega T_p) - 180^o \quad (4)$$

$\frac{d\phi}{d\omega} = \frac{T_z}{1+(\omega T_z)^2} - \frac{T_p}{1+(\omega T_p)^2} = 0$gives a maxima in phase margin at $\omega_m = \frac{1}{\sqrt{T_zT_p}}$. The phase margin maxima should occur at unity –gain crossover frequency (ωc) i.e. at ωc=ωm and transfer function gives

$$C_1 + C_2 = \frac{I_{CP}\,K_{VCO}}{2\pi N\,\omega_c^2}.\sqrt{\frac{1+(\omega_cT_z)^2}{1+(\omega_cT_p)^2}} \quad (5)$$

The time constants can be written as

$$T_p = \frac{\sec\phi_o - \tan\phi_o}{\omega_c}\text{and}T_z = \frac{1}{\omega_c{}^2T_p} \quad (6)$$

From the above equations, for a target bandwidth (ωc) and phase margin (ϕ0), R1, C1 and C2 are obtained as

$$C_1 = \left(\frac{T_z}{T_p} - 1\right)C_2\,;\, C_2 = \frac{T_p}{T_z}(C_1 + C_2)\text{and}R_1 = \frac{T_z}{C_1}$$

All the individual blocks have been designed and simulated and have been cascaded to form the frequency synthesizer using cadence virtuoso software. The final schematic of the frequency synthesizer is as depicted in fig. 11.

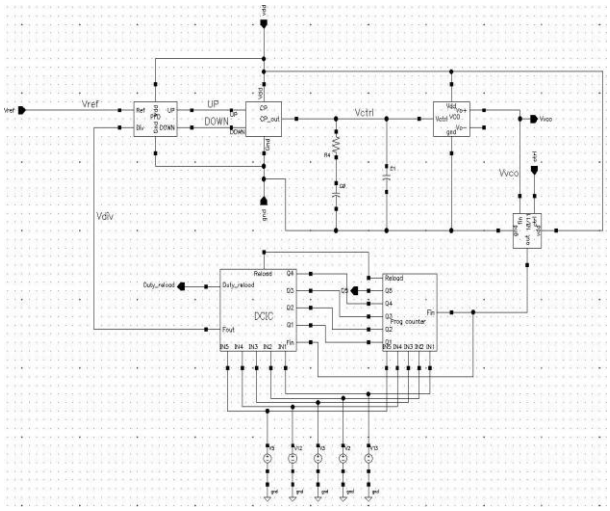


Fig. 11. Schematic of Integer-N Frequency Synthesizer

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4. Simulation Results

The frequency synthesizer was designed in 0.18µm CMOS process and was simulated using Cadence virtuoso software. The simulation results are as follows.

The transient output of the synthesizer is shown in fig.12. The frequency synthesizer is given an input frequency of 5MHz with amplitude 1.8V. The synthesizer takes less than 20µs to obtain the lock condition. The detailed view of the lock condition can be seen in fig. 13.

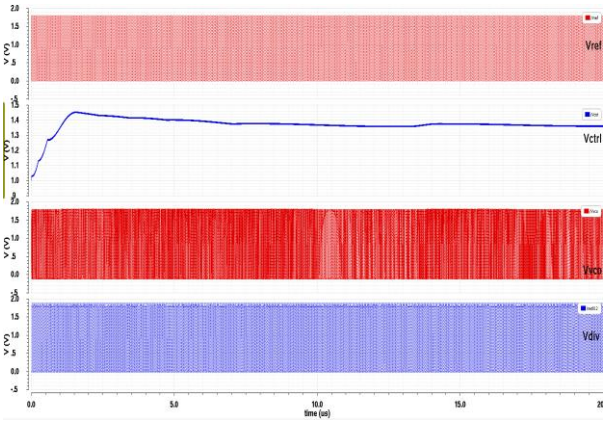


Fig. 12. Frequency synthesizer output

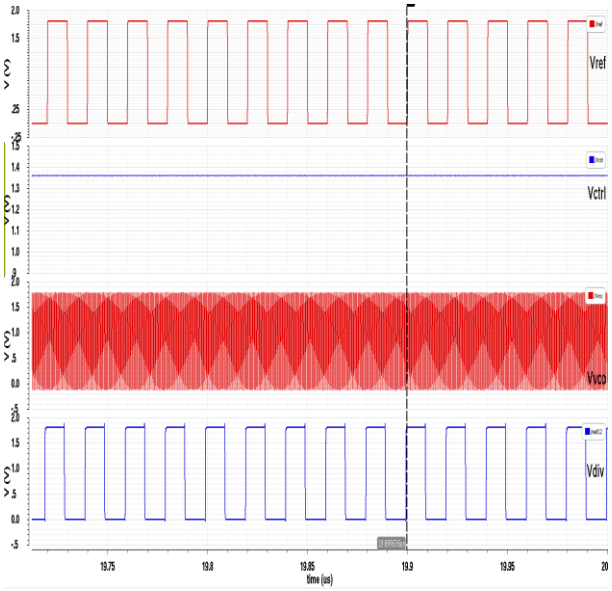


Fig. 13. Detailed view of the lock condition

Table-1 Performance summary of proposed work

Power consumption	5.54mW
Frequency range	2.4-2.5GHz
Channel spacing	5MHz
Reference frequency	5MHz
Phase noise	-95.15dBc/Hz @ 1MHz
Settling time	20µs
Division ratio	480 to 500

Table-2 Comparison of various frequency synthesizers

Parameter	[7]	[8]	[9]	This work
Process	180nm	180nm	180nm	180nm
Supply voltage	1.8V	1.8V	1.2V	1.8V
Reference frequency	5MHz	290MHz	2.5MHz	5MHz
Output frequency	2.4-2.48GHz	2.4-2.48GHz	2.4-2.475GHz	2.4-2.5 GHz
Phase noise (dBc/Hz)	-108.55 @ 1MHz offset	-121 @ 3MHz offset	-116.5 @ 1MHz offset	-95.15 @ 1MHz offset
Power	7.95mW	14.1mW	4.2mW	5.54mW

5. Conclusions

The frequency synthesizer is designed and simulated using 180nm technology in Cadence environment. The output frequency of the synthesizer ranges from 2.4GHz to 2.5GHz and power consumption is 5.54mWfrom a 1.8V power supply. The phase noise at 1MHz offset is -95.15dBc/Hz. The VCO with fairly linear VCO output frequency vs. tuning voltage has been implemented which reduces the K_{VCO} variation which reduces the noises from PFD, charge pump, loop filter and input reference frequency source at synthesizer output.

6. Acknowledgement

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