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Research paper

A design of sequential reversible circuits by reversible gates

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Abstract

Reversible logic has become increasingly important in the design of low power CMOS circuits, quantum computing and nanotechnology. In this article we work on recent sequential circuits namely RS Flip Flop JK Flop Flip Flop Flop Flip Flop Master Slave Flip Flop using some reversible gates FG (Feyman Gate), FRG (Fredkin Gate), NG (New Gate) , PG (Peres Gate), BJN (New BJN Gate), while modifying them to obtain new circuits keeping their same functionality and increasing their performances.

Keywords: *RS Flip Flop; D FLIP FLOP; JK FLIP FLOP; T FLIP FLOP; Master Slave FLIP FLOP; Quantum Cost; Hardware Complexity.*

1. Introduction

In the irreversible circuit each lost bit generates a loss of heat described by KTln2 joules of or K: Constant of BOLTZMAN T: Absolute temperature related to the computation, Formula established by Landauer [1] .In the reversible case Bennett showed that this said quantity heat would not occur [2], the proof is that this amount of heat is related to the number of bits lost in an irreversible circuit. These circuits have a bijection between its inputs and outputs, hence a reversible gate NXN can be represented by $Iv = (I1, I2, I3, I4, \ldots IN)$ $Ov = (O1, O2, O3, \ldots ON)$. Where Iv and Ov unveil the input and output vectors respectively. In the irreversible gates one can not deduce the input vector in a unique way from the output one. There are certain reversible gates Feyman Gate (FG), Fredkin Gate (FRG) New Gate (NG) Peres Gate (PG) [3], New BJN (BJN) [4].The irreversible logic strongly dissipates the energy in the form of heat by minimizing the life of the circuits against the reversible reversible logic, which can be exploited speed in circuits sensitive to power at high speed, so in the CMOS design, optical computing and quantum making the most important application, which gives rise to what is called a quantum computer that is a set of quantum networks each of which is composed of quantum logic gates performing an elementary operation on one or two or more quantum systems with two states named qu-bits, which represent an elementary unit, of information corresponding to the conventional values of bits 0 and 1 [5]. The reversible logic differs from the irreversible one in that the first does not allow any derivation, in other words, the exit of a gate is represented as an entry into the next gate, which indeed reflects an inter-gate dependence, In addition, reversible logical synthesis sequential differs from the combinatorial one in that in the first the output of the logic circuit depends on the inputs present and thus past inputs ie the current internal state.
To design a complex system one will need circuits based on electronic flip-flops. In this paper we exploit a recent study to design reversible sequential circuits that can perform more delicate operations using quantum computers using certain reversible gates namely Feyman Gate (FG), Fredkin Gate (FRG) , New Gate (NG), Peres Gate (PG) and New BJN Gate (BJN) [3,4].Also we designed sequential circuits synthesized by the reversible logic namely RS, JK, D, T and Master Slave Flip Flop while improving performance and obtaining better results.

2. Reversible equivalent gates used for designing sequential circuit

In our work, we have convert conventional logic sequential circuits into reversible mode using some of the same type of gate to improve the performance [5]. The Figure 1 (fig1) shows the design of the AND using the Fredkin Gate, then designed NAND, NOR using the Peres Gate and New BJN Gate in the Figures 2 and 3 respectively (fig2, fig3). Also, we can use Feyman Gate (FG) to copy the output (fig4) or to reverse the output (fig5).

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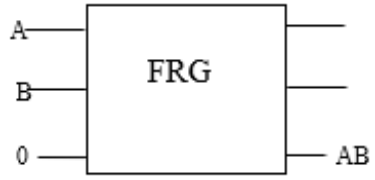


Fig. 1: Fredkin Gate as AND Gate.

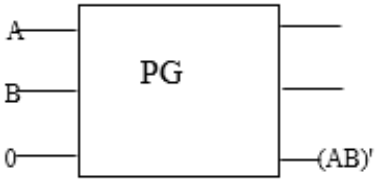


Fig. 2: Peres Gate as NAND Gate.

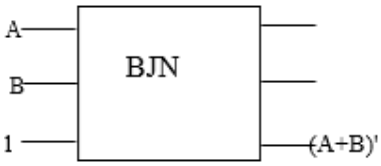


Fig. 3: BJN Gate as NOR Gate.

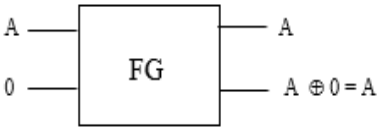


Fig. 4: Feyman Gate as Copying Output.

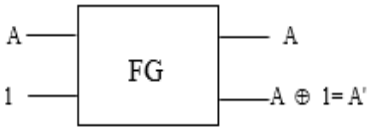


Fig. 5: Feyman Gate as Not Gate.

3. Exploited work

In this section, we are going to exploit recent sequential circuits [6] to modify them while improving their performances, starting with:

3.1. RS flip flop

The Figure 6 [6] shows an RS flip-flop designed with irreversible gates, containing 2 AND gates and 2 NOR gates, in the figure 7 (fig. 7) [6] shows its equivalent using reversible gates.

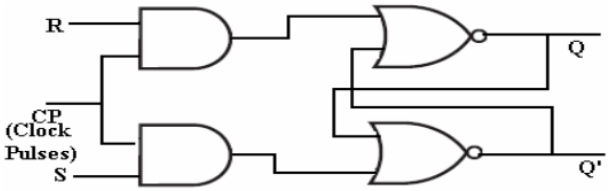


Fig. 6: Conventional RS Flip Flop.

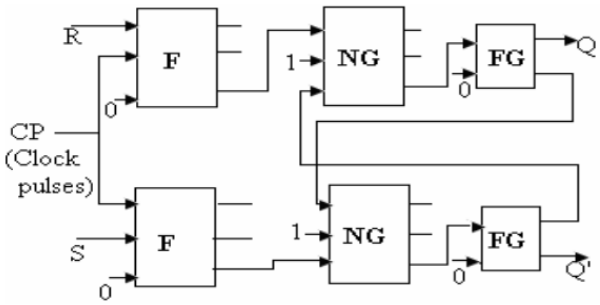


Fig. 7: RS Flip Flop with Reversible Gates.

After moderating the exploited circuit, replacing FRG by PG and NG by BJN while maintaining the third entry at 1 and keeping the same functionality, we obtained our proposed design of the circuit (Fig 8). The Table 1 shows the evaluation of the design and the improved results obtained from this moderation.

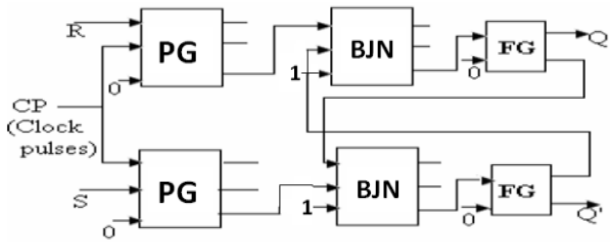


Fig. 8: Our Design RS Flip Flop with Reversible Gates.

Table 1: Evaluation of the Proposed of RS Flip Flop

Design of RS Flip Flop	Quantum Cost	Hardware complexity
Our Design	20	$8\alpha + 2\beta$
Exploited Design [6]	34	$10\alpha + 12\beta + 8\delta$

α: number of CNOT gates, β: number of AND δ: number of NOT.

From these results we deduce that we have minimized compared to the model exploited:

- The quantum cost of 41,17%
- The Hardware complexity at 20% for CNOT gates and 83,33% for AND gates and eliminating all NOT gates.

3.2. D Flip flop

In the figure bellow (fig. 9) [6], FLIP-FLOP D is designed with five conventional irreversible NAND gates. the Figure (fig10) [6] shows its reversible equivalent.

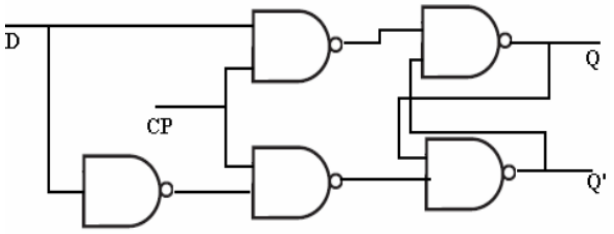


Fig. 9: Conventional D Flip Flop.

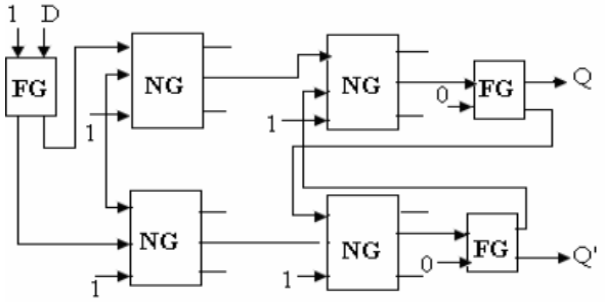


Fig. 10: D Flip Flop with Reversible Gates.

After moderating the exploited circuit, replacing NG by PG and keeping the same functionality, we got our proposed design (Fig 11).the Table 2 shows an evaluation of the proposed D Flip Flop design and the improved results obtained with this moderation.

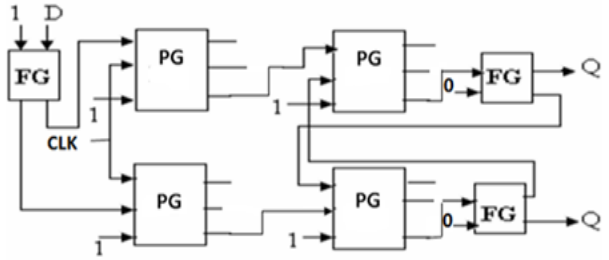


Fig. 11: Our Design D Flip Flop with Reversible Gates.

Table 2: Evaluation of the Proposed of D Flip Flop

Design of D Flip Flop	Quantum Cost	Hardware complexity
Our Design	19	$11\alpha + 4\beta$
Exploited Design [6]	47	$11\alpha + 8\beta + 12\delta$

α: number of CNOT gates, β: number of AND δ: number of NOT.

From these results we deduce that we have minimized compared to the model exploited:

- The quantum cost of 59.57%.
- The Hardware complexity at 50% for AND gates and eliminating all NOT gates.

3.3. JK flip flop

The JK flip-flop is the moderation of that of the RS since its indeterminate state is defined (JK flip-flop). when the inputs J and K are applied at the same time, the JK flip-flop returns to its complement state. The irreversible design of the JK flip-flop is illustrated in (fig. 12) [6] and the reversible moderation in (fig. 13)[6] .

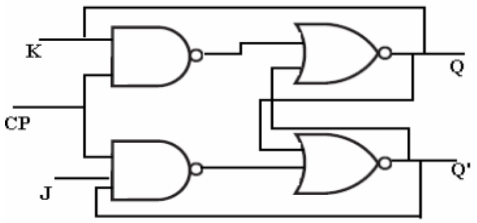


Fig. 12: Conventional JK Flip Flop.

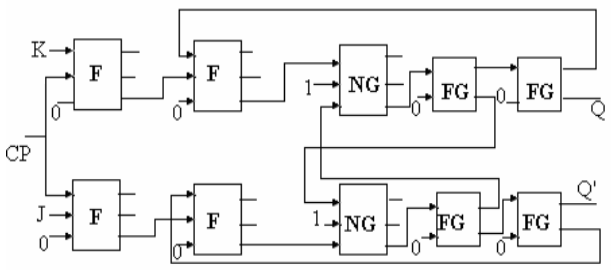


Fig. 13: JK Flip Flop with Reversible Gates.

By moderating the exploited circuit, replacing FRG by PG and NG by BJN while maintaining the third entry at 1 and keeping the same functionality, we get our proposed design (Fig 14) .the Table 3 shows an evaluation of the proposed of JK Flip Flop and the improved results obtained with this moderation.

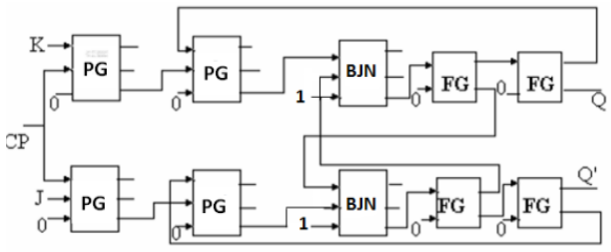


Fig. 14: Our Design JK Flip Flop with Reversible Gates.

Table 3: Evaluation of the Proposed of JK Flip Flop

Design of JK Flip Flop	Quantum Cost	Hardware complexity
Our Design	30	$14\alpha + 4\beta$
Exploited Design [6]	46	$16\alpha + 20\beta + 10\delta$

α: number of CNOT gates, β: number of AND δ: number of NOT.

From these results, we deduce that we have minimized compared to the model exploited:

- The quantum cost of 34.78%.
- The Hardware complexity at 12,5 % for CNOT gates and 80% for AND gates and eliminating all NOT gates.

3.4. T flip flop

In the JK flip-flop if the two inputs are linked and having the same input signal, it constitutes the flip-flop T shown in fig 15 [6] , designed from conventional irreversible gates. The Figure (fig 13) [6] shows the Flip Flop T designed from the reversible equivalent gates.

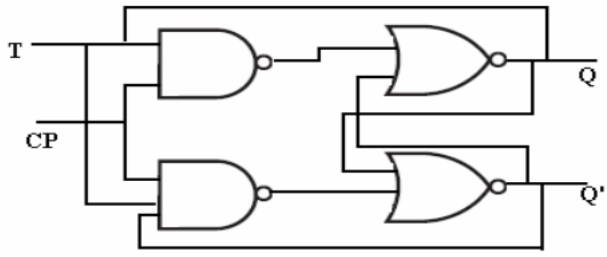


Fig. 15: Conventional T Flip Flop.

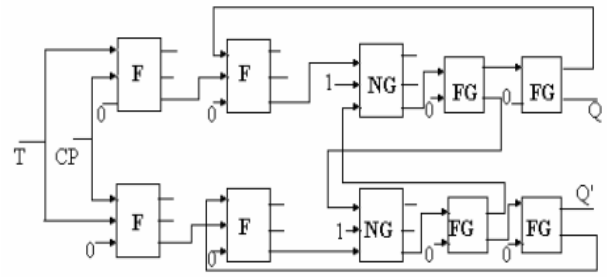


Fig. 16: T Flip Flop with Reversible Gates.

By moderating the exploited circuit, replacing FRG by PG and NG by BJN while maintaining the third entry at 1 and keeping the same functionality we get our proposed design (Fig 17). The Table 3 shows the improved results obtained with this moderation.

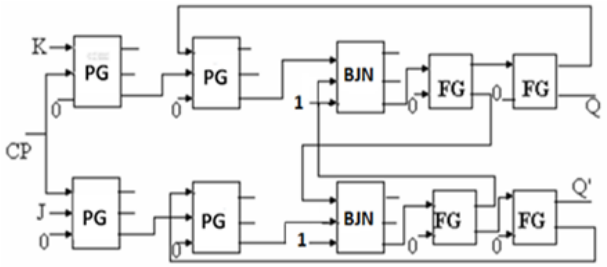


Fig. 17: Our Design T Flip Flop with Reversible Gates.

Table 3: Evaluation of the Proposed of T Flip Flop

Design of JK Flip Flop	Quantum Cost	Hardware complexity
Our Design	30	$14\alpha + 4\beta$
Exploited Design [6]	46	$16\alpha + 20\beta + 10\delta$

α: number of CNOT gates, β: number of AND δ: number of NOT.

The results obtained are similar to those of the design of the last JK flip-flop.

3.5. Master slave flip flop

The master-slave rocker as indicated by its name consists of two flip-flops; one for master and the other for slave represented in (fig. 18) [6]. In irreversible mode consisting of NAND gates in reversible mode (fig. 19) [6].

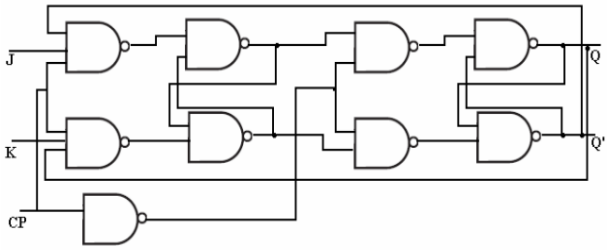


Fig. 18: Conventional Master Slave Flip Flop.

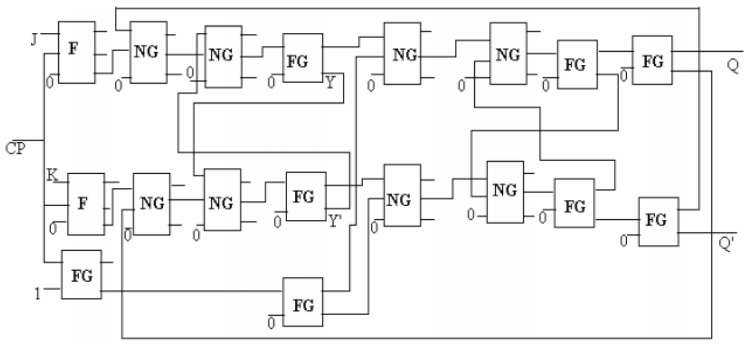


Fig. 19: Conventional Master Slave Flip Flop.

By moderating the exploited circuit, replacing FRG and NG by PG 1 and keeping the same functionality we get our proposed deign (Fig 20). The Table 4 shows an evaluation of the proposed of Master Slave Flip Flop and the improved results obtained with this moderation.

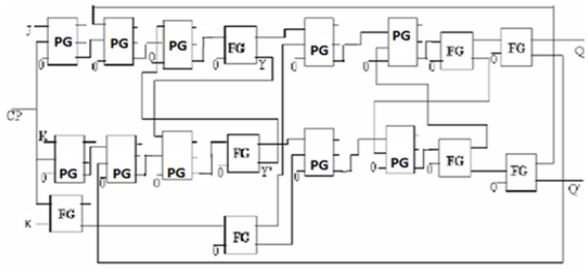


Fig. 20: Our Design Master Slave Flip Flop with Reversible Gates.

Table 4: Evaluation of the Proposed of Master Slave Flip Flop

Design of JK Flip Flop	Quantum Cost	Hardware complexity
Our Design	48	$28\alpha + 10\beta$
Exploited Design [6]	106	$28\alpha + 24\beta + 26\delta$

α: number of CNOT gates, β: number of AND δ: number of NOT.

From these results, we deduce that we have minimized compared to exploited model:

- The quantum cost of 54.71%.
- The Hardware complexity at 58.33% for AND gates and eliminating all NOT gates.

4. Conclusion

Some gates are important for circuit design, including reversible sequential circuits. In this article, we used older systems to design sequential circuits using logical inversion gates while trying to improve performance by minimizing the quantum cost and the Hardware complexity we achieved better, and more outstanding results compared to our basic items. While waiting for new reversible gates that can produce better results in the future.

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