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Research paper

Design and implementation of smart traffic light controller using VHDL language

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Abstract

The purpose of this paper is to design and implementation of smart traffic light controller system using VHDL language and FPGA. A structure of four road intersection has been selected. The intersection to be controlled is between a busy (main street), and somewhat less busy (side street), with sensor for the side street and walk request button. Also, the system contains switches to control the traffic light manually. The intersection uses four timing parameters with ability to change these parameters manually. The system has been successfully tested with VHDL using Xilinx ISE 14.7i software environment and Chip-Scope, while, it is implemented in hardware using Xilinx Spartan 3E FPGA. It is easy to use and the cost for the same is also less as compared to the others. The designed traffic light control system is presented to work correctly as predictable.

Keywords: *Traffic Light Controller (TLC); FSM; VHDL; Spartan 3E; FPGA; Xc3s500fg320-4.*

1. Introduction

Traffic jamming is a critical predicament in many of the cities and towns all over the world. Traffic congestion has been causing many setbacks and challenges in the major and most occupied cities all over the globe. This traffic jam directly impacts the productivity of the workers, traders, suppliers and in all affecting the market and raising the prices of the commodities in a way light [1], [2], [3]. The problem of heavy jam is happened because of never configure the level of jam in each way and set the delay time. Another problem represents when there is no jam, but the waiting still continues. The solution for these problems is to determine the level of jam and set the delay time. This problem need of evaluation of the traffic policeman, and then there is need for manual control of the traffic [4], [5], [6]. The target of this paper is to propose system provide solution for all above problems with least possible cost.

Traffic light controller (TLC) can be implemented using microcontroller, FPGA, and ASIC design. FPGA has many advantages over microcontroller, some of these advantages are; the speed, number of input/output ports and performance which are all very important in TLC design, at the same time ASIC design is more expensive than FPGA [7],[8]. Nowadays, FPGA becomes one of the most successful of today's technologies for developing the systems which require a real time operation. FPGA is a reconfigurable integrated circuit that consists of two dimensional arrays of logic blocks and flip-flops with an electrically programmable interconnection between logic blocks. The reconfiguration property enables fast prototyping and updates for hardware devices even after market launch [9], [10]. Most of the TLCs implemented on FPGA are simple ones that have been implemented as examples of Finite State Machine (FSM). [7]

The VHDL language has been selected for programming the FPGA to fill two important needs in the design process. Firstly, it gives full description of the structure of a design that is how it is decomposed into sub-designs, and how those sub-designs are interconnected. Secondly, it allows simulating the design before starting the manufacturing. Accordingly, the designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping [11].

In this paper, a traffic light system is designed using VHDL and implemented by a single FPGA chip. The outline of the paper is structured as follows: Section 2 covers the related works of traffic light system which are deliberated via VHDL and realized through FPGA. Also, traffic light controller system design is the subject of section 3. Furthermore, a simulation of the proposed traffic light system and the simulation results with a discussion are demonstrated in section 4. As well, section 5 includes the hardware implementation of traffic light system on Xilinx Spartan 3E FPGA and displays the testing and operation of it. Finally, the conclusions of this paper are provided in section 6.

2. Related works

Many researches about traffic light system have been done in order to overcome some complicated traffic phenomenon but most of them sometimes fail to deal efficiently with the complex, time-varying traffic conditions and controller can't satisfy real-time character for traffic signal [2] [12]. The following literature survey elucidates some of researches in the recent few years.

In 2012, B. Dilip et al. [13] presented the FPGA implemented low cost advanced TLC system using Chip-Scope Pro and Virtual Input Output. The TLC implemented was one of the real and complex signaling lights in Kingdom of Bahrain, for pedestrian way included four roads and sensors and camera assisted motorway. The system had been implemented in hardware using Spartan-3E FPGA.
In same year, A. Mandloi et al. [14] had used Mealy based Finite state machine to design an efficient and intelligent traffic light controller. Mealy machines were used to implement the system because outputs signal were controlled by the inputs signals. The language used for the implementation was VHDL with mixed modeling style. The design was tested on Spartan-3 xc3s200 FPGA development kit. Total memory usage was 105456 kilobytes.
In 2014, Surabhi S. et al. [15] presented an adaptive traffic light controller (TLC) customized to have user defined number of intersection lanes and counts of signals for various intersections. The proposed system prototype was implemented on FPGA and typical TLCs were modeled using the finite state paradigm and rely heavily on software design flow. The hardware design had been deployed using the structural style of VHDL programming and thus offers more robustness.
In 2015, V. V. Dabahde el at. [16] proposed the Intelligent Traffic Light Control system to reduce waiting times of the vehicles at traffic signals. The proposed system made use of FPGA technology along with traffic sensors to control traffic according to the traffic requirement and thus reduced the waiting time, at an intersection of two roads. The system had been successfully tested and implemented in hardware using ALTERA Cyclone II- FPGA. The system had many advantages over the exciting TLC.
In 2016, Ali K. A. [11] designed an intelligent traffic light control system using FPGA and VHDL. Moreover, multiple level of functionality such as adding a standby control signal, the motion sensor handling part, special request implementation, and loaded traffic design had been taken into consideration. Its function was verified and simulated using ModelSim.
In 2017, P.Giri Prasad el at. [17] designed an intelligent transportation of system (ITS) using VHDL and implemented on FPGA. Also, it was determined the traffic in each road by using sensors. Using the traffic status, the signal time can be managed and in this way, the traffic on road can be handled. On each particular way junction, the IR sensors can be placed to detect the traffic density and give the current traffic status particular way in the junction. Its function was verified and simulated by using ModelSim.

3. Traffic light controller system design

Figure 1 illustrates the structure of the selected traffic light model for four road intersections (one Main Street and three side streets). In general, Traffic Light Controller System consists of three lights (red, green and yellow) in each direction .The red light indicates to Stop, green light indicates to allow the traffic and yellow light indicates the caution that the traffic is going to be stopped in few seconds. While, turning in yellow and red lights at the same time indicates the caution that the traffic is going to be moving in few seconds. The intersection is fitted with a sensor for side street traffic and with walk request button.
This traffic light controller also has provision for walk light (which consists of two lights red and green, where, green light allows the walkers to pass the street while red light avoids the walkers from passing the street) and for the traffic sensors in each one of the side streets. A simple block diagram of the traffic light controller system is exposed in Figure 2. The design is composed of finite state machine (FSM), data storage (D_RAM), timer, divider, and various synchronizers (latch, and synchronizer).

3.1. Finite state machines (FSM)

Finite State Machines (FSM) is the heart of the traffic light controller system. This FSM controls the loading of static data storage locations with timing parameters, displaying these parameters by reading RAM locations, and the control of the actual traffic lights. There are four timing parameters in this system as displayed in Table 1. They are the base interval (TBASE) for side green, an extended interval for main green and walk green light (TEXT), the time for yellow light (TYEL), and a blink interval (TBLINK). The user can specify the four timing parameters using two switches (L0, L1) manually. The FSM can execute four functions specified by two functions switches (F0, F1). These functions are listed in Table 2, where, the user can execute one of four possible functions: writing new timing parameters, reading old timing parameters, running traffic light in normal mode, and running the traffic light in blinking mode as obtained in Figure 3a. Besides, the idle state of the FSM is called the reset state, in this state, the lights are turned off and the system does not do anything. The system will stay in the reset state until the GO button is pressed.

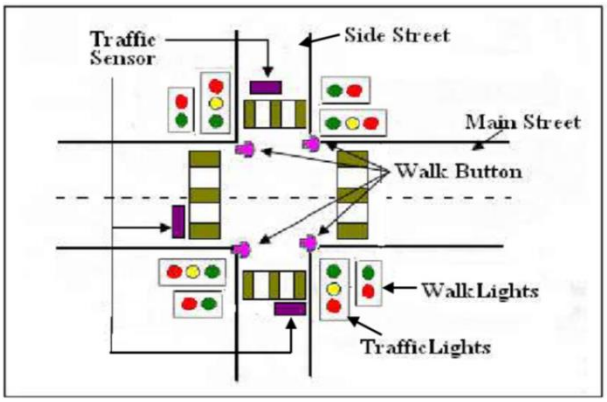


Fig. 1: Example for the Traffic Light System.

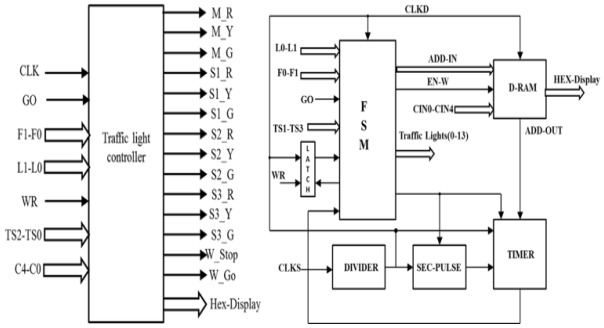


Fig. 2: The Structure Model of the Traffic Light Controller System.

Using the writing function, the user can specify the any one of the four timing parameters as shown in Table 1 using (L1, L0) switches, the value of the parameter is set using the (C4_C0) switches. For the reading operation, the user can use the same L1 and L0 switches to denote which of the four timing parameters to view on a set Hex-LEDs. In normal mode or blinking mode, the system just cycles through the various traffic light states. The regular controller has been designed with nine states as presented in Table 3 without taking the traffic sensors and walk request in the point view.

In the normal mode that is displayed in Figure 3b, the side street has a shorter green interval than the main street, but if there is traffic on the side street when the controller is about to cycle to turn that green light off, it will extend the green light by the shorter (side street) green interval. Thus the green light on the side street will stay on until traffic on the side street clears. Traffic sensor switch is used to simulate the effect waiting traffic on the side street, the system complies by keeping side street green until the traffic sensor is switch off. The walk light comes on after the main street yellow interval, and then only if the walk request button has been pushed. Late at night or when something in the system is not working, the light goes into the blinking mode this involves the lights blinking on and off, alternating between main yellow side red, and main red side yellow as shown in Figure 3a.

Table 1: Time Operations for the Traffic Light Controller System

F1	F0	Mode Type
0	0	Read Mode
0	1	Write Mode
1	0	Normal Mode
1	1	Blinking Mode

Table 2: Modes Operations for the Traffic Light Controller System

L1	L0	Time Type
0	0	TBASE
0	1	TEXT
1	0	TYEL
1	1	TBLINK

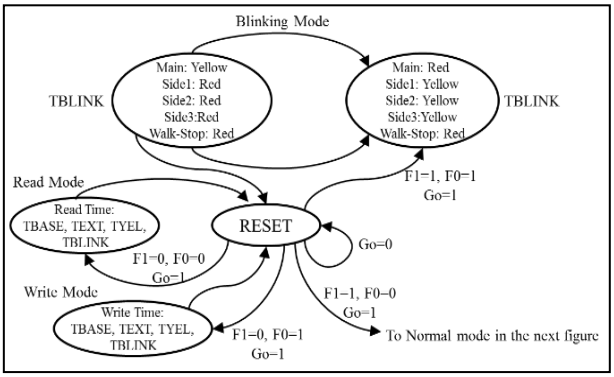


Fig. 3: A) FSM State Transition Diagram.

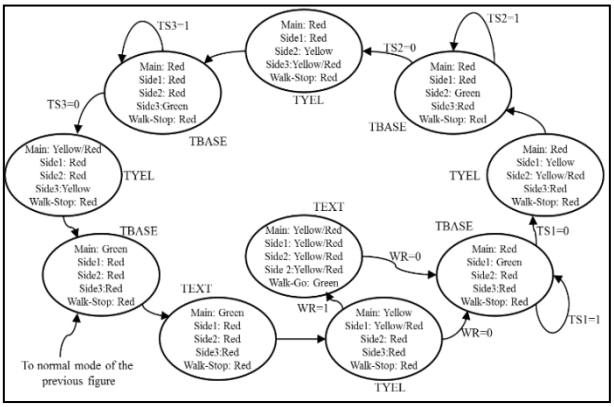


Fig. 3: B) FSM State Transition Diagram.

Table 3: Operations of Traffic Light Controller System in Normal Mode without Using the Traffic Sensors and Walk Request

Time Type	Main Street	Side 1 Street	Side 2 Street	Side 3 Street
TBASE	Green	Red	Red	Red
TEXT	Green	Red	Red	Red
TYEL	Yellow	Yellow/Red	Red	Red
TBASE	Red	Green	Red	Red
TYEL	Red	Yellow	Yellow/Red	Red
TBASE	Red	Red	Green	Red
TYEL	Red	Red	Yellow	Yellow/Red
TBASE	Red	Red	Red	Green
TYEL	Yellow/Red	Red	Red	Yellow

3.2. D_RAM

This component is used to store the four timing parameters which are declared in Table 1. Depending on the signal en_w, which select to read the contents by L0-L1 switches, or write new timing parameters by C0-C4 switches and display the contents on the HEX_LEDs

3.3. Divider, sec_pulse, and timer

The divider component is used to generate the clock (1 MHz) for overall system from 50 MHz of the chip FPGA Spartan 3E. While, the Secpulse component is used to generate one second clock, which is used in the timing of the traffic light. The timer is implemented as counter.

3.4. Latch and sensors

Walk signal is latched so that when the user pushes the walk button once the signal is queued until the FSM need it. Figure 4 expresses schematic circuit of walk latch. Furthermore, there are three traffic sensors which are synchronized by simply passing it through a flip flop.

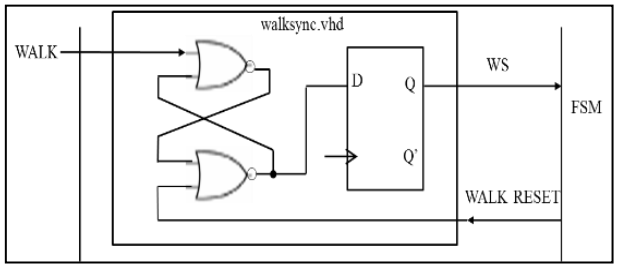
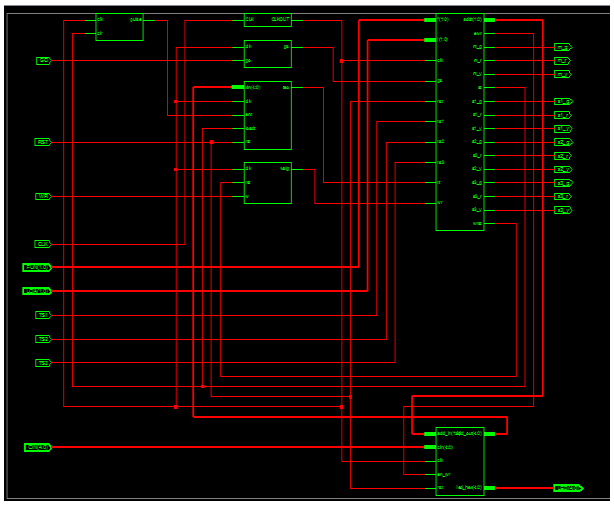


Fig. 4: Walk Latch Schematic Circuit.

4. Simulation results

The key advantage in using the VHDL in systems design is allowing the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires)[11]. Figure 5 indicates the RTL and technology schematic diagram of the traffic light controller system. All component of the system are simulated using Xilinx ISE 14.7i. Viewing a schematic allows to see a technology level representation of HDL optimized for specific device architecture, that it may be assisted to discover the scheme issues early in design process. The simulation result of the traffic light controller system in reading and writing modes are exhibited in Figure 6a. In this case, all traffic light outputs are off and HEX_LEDs display the output of memory location which represents the selected time mode. Furthermore, the normal mode is displayed in Figure 6b, which denotes the operation of TLC system as appeared in Figure 3b. The synthesis process generates net list for each design element. Synthesis process checks code syntax and analyzes the hierarchy of the design to ensure that the design is optimized for the system.



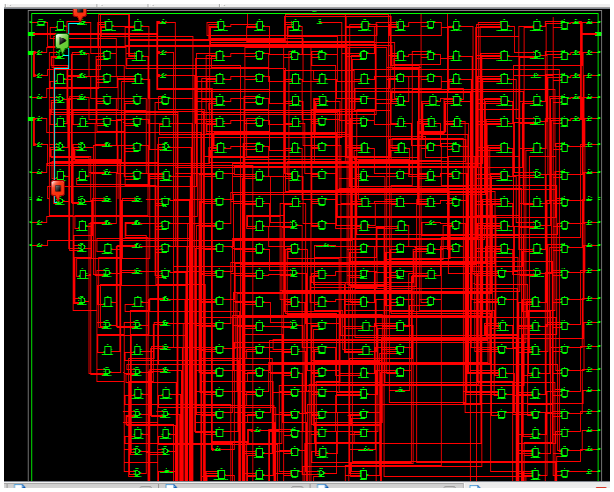


Fig. 5: RTL &Technology Schematic of the Traffic Light Controller System.

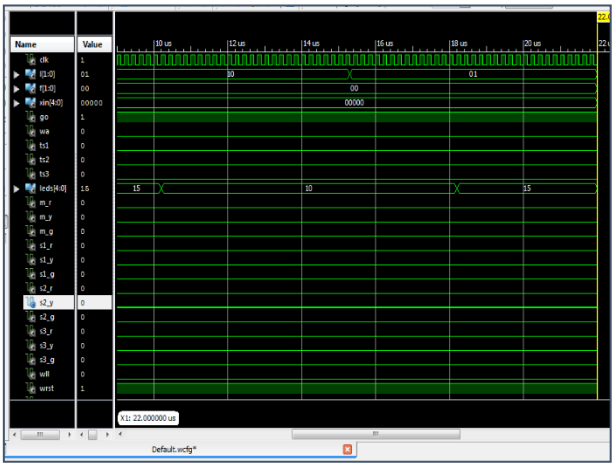


Fig. 6: A) Simulation Result of the T.L.C System in Reading and Writing.

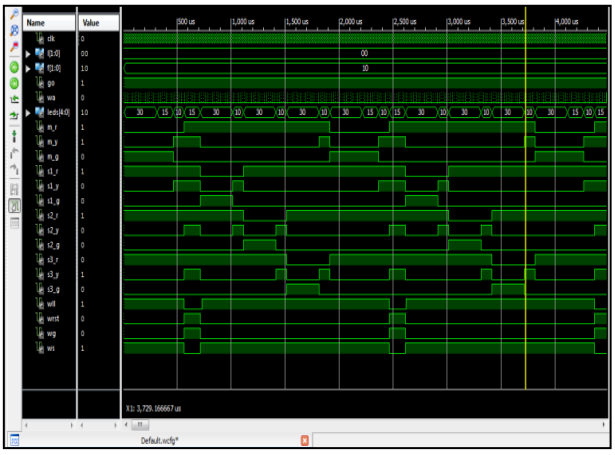


Fig. 6: B) Simulation Result of the T.L.C System in Normal Mode.

5. Hardware implementation

The traffic light controller system design is implemented by synthesizing the VHDL structural code design, then generating bit file using Xilinx ISE 14.7 tools. This bit file is downloaded to the FPGA Spartan 3E development kit xc3s500efg320. The system's outputs are more than the LED on FPGA, then, it is used the LEDs to display one state or use the supporting chip (expansion) external pin digilent (FX2 MIB) as confirmed in Figure 7. Figures 8 and 9 demonstrate the real time implementation of TLC and Chip-Scope implementation respectively. The system design gives the realization of the hardware system as well as the software. The hardware consumptions are listed in Table 4.

Fig. 7: Supporting Chip (FX2 MIB).

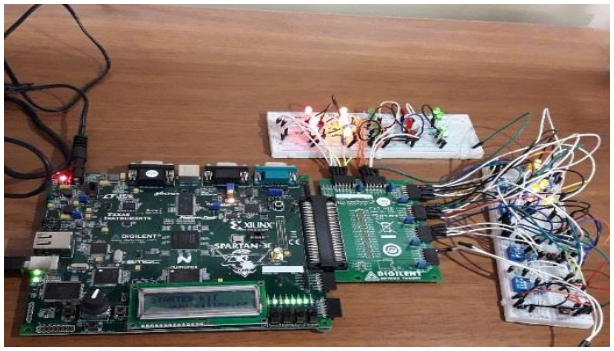


Fig. 8: FPGA Implementation of TLC System.

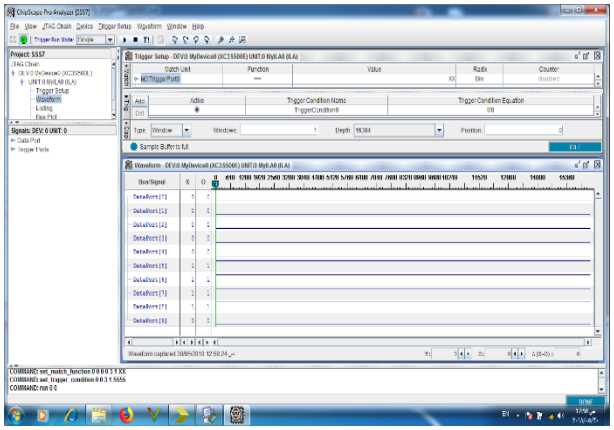


Fig. 9: TLC System Output Using Chip-Scope.

6. Conclusion

A smart Traffic Light Controller system is designed using FPGA for four roads intersection with traffic sensors and walk request signals. The system has been simulated using VHDL to realize alternating traffic light and FSM for efficient T.L.C. with ability to change its timing parameters manually. Each subcomponent is constructed and tested thoroughly before moving onto the next one. The design is robust; all the design decisions were inspected comprehensively before employment. Synchronization component are very important in the system design where they are implemented without any hazards in the system. Overall the design and implementation of the traffic light controller is respectable to design more complex system. The system is verified on FPGA Spartan 3E xc3s500efg320-4.

Table 4: Device Utilization Summary

Selected Device : 3s500efg320-4	
Number of Slices:	83 out of 4656 1%
Number of Slice Flip Flops	115 out of 9312 1%
Number of 4 input LUTs:	141 out of 9312 1%
Number of bonded IOBs	40 out of 232 17%
Number of GCLKs	2 out of 24 8%
Timing Summary:	
Minimum period:	6.132ns
Minimum input arrival time before clock	5.355ns
Maximum output required time after clock:	4.532ns

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