International Journal of Engineering & Technology, 7 (4.22) (2018) 192-196

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Enhanced Carrier Level Shifted PWM Technique for Capacitor Voltage Balance in Five-Level DCMLI

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Abstract

An Inherent problem with the Diode Clamped Multi Level Inverter is the unbalance in capacitor voltages. This unbalance may lead the inverter to have uneven levels of output voltage and more THD as compared to the expected. Therefore, the stabilization of neutral point voltage is the major task to get expected voltage and the desired levels. There are techniques, which are reliable for the neutral point stabilization of three-level diode clamped multilevel inverters, but there is no specific reliable technique, which would provide inherent stabilization of capacitor junction voltages in the five-level diode clamped multilevel inverters. Existing techniques use either back to back connection of five-level inverter-rectifier or use separate DC sources (SDCS). These methods use extra components and are complex to implement. To overcome this problem a new inherent control technique entitled as 'Enhanced Carrier Level Shifted PWM Technique' is recommended in this paper to stabilize the capacitor junctions in five-level diode clamped multilevel inverter (DCMLI).

Keywords: *Five-Level DCMLI; Neutral Point; Capacitor Voltage Balance; Medium High Power Drives; STATCOM; FACTS; HVDC; Renewable Energy Conversion.*

1. Introduction

Conventional inverters, well known as two level inverters were popularly used for DC to AC conversion. The output of the conventional two level inverters is a square wave, which is different from the sinusoidal wave. Moreover, the square wave consists of harmonics (including lower order and higher order) which leads to the more THD in the output wavefrom of the inverter. To reduce THD, Pulse Width Modulation (PWM) techniques were proposed. With these techniques, the lower order harmonics were shifted to high order and were easily filtered out or eliminated. However, the major disadvantage with this PWM technique is that the switching frequency must be high. If the switching frequency is increased then the dv/dt stress on the switches is increased which leads to the decrease in the lifetime and the reliability of the switches. Hence, inverter should be designed to have low THD and reduced dv/dt stress on the switches. From this performance perspective, Multilevel Inverters impressed with low THD, reduced dv/dt stress and less EMI and used for high power applications.

In the present scenario, Multilevel Inverters have drawn remarkable importance in the power transmission, power industries and medium voltage high power drives [1]. Multilevel Inverters deliver a new set of features that are well suited for the medium voltage high power applications which embraces traction drive system, reactive power (VAR) compensation, enrichment of active filtering, high voltage electric drives, HVDC, FACTS[5]. The sophisticated research on the development of switches like IGBT's(Insulated Gate Bipolar Transistor), IGCT's(Integrated Gate Commutated Thyristor) and the usage of these switches in voltage source multilevel inverters have directed to the extreme increase of the voltage and power ratings of the converters and to use these in the medium and high voltage electric drives[8]. These enhance the dynamic performance of the multilevel inverters.

1.1. Five Level Diode Clamped Multilevel Inverter

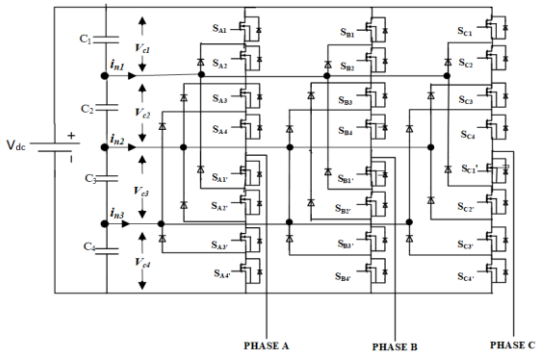

Fig. 1: Five-level DCMLI Topology

The widespread topologies of the multilevel inverters are classified into three categories [3] namely:

1. Flying Capacitor MLI,
2. Cascaded H-Bridge MLI and
3. Diode Clamped MLI

Considering each topology, the productivity of the Flying Capacitor Multilevel Inverter is somewhat poor because of more number of components and capacitors, which leads to the circuit to complex structure. As far as Cascaded H-Bridge Multilevel Inverter topology is considered, the usage of separate DC sources (SDCS) is needed to produce desired output and uses more number of components that leads the circuit to be inefficient, complex and uneconomical. While coming to the Diode Clamped Multilevel Inverter topology, which has been in use since 25 years in the

industries, uses less number of capacitors and switching devices that leads the circuit to be more efficient. Hence, the DCMLI topology is most preferred topology for the inverter design. The fig.1 demonstrates the topology of the DCMLI.

Table 1: Switching Table for Five-Level DCMLI

S.No.	S_{A1}	S_{A2}	S_{A3}	S_{A4}	Output Pole Voltage
1.	1	1	1	1	Vdc/2
2.	0	1	1	1	Vdc/4
3.	0	0	1	1	0
4.	0	0	0	1	-Vdc/4
5.	0	0	0	0	-Vdc/2

Diode Clamped Multilevel Inverter belongs to the family of Neutral Point Clamped (NPC) Multilevel Inverters. This topology uses (m-1) capacitors, (m-1)*(m-2) diodes and 2*(m-1) switching devices to produce m-level output. The switching logic for 5-level DCMLI uses 4 carrier signals compared with 1 reference signal in Phase Disposition manner of carriers as shown in the fig.2 and the switching table to produce 5-level output is mentioned in the TABLE:1. As this topology uses less number of switching devices and components, the efficiency and the reliability is more. The topology of the Diode Clamped Multilevel Inverter is shown in the fig.1.

Advantages of Diode Clamped Multilevel Inverter:

1. Less number of components.
2. More efficiency when compared to other topologies.
3. Single DC bus is enough to produce multilevel AC output.

Drawbacks of Diode Clamped Multilevel Inverter:

1. Loss distribution among switches.
2. Unbalance in the voltage sharing among the DC capacitors.

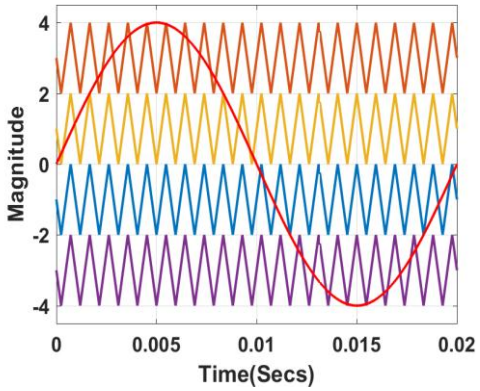

Fig. 2: Reference and Carrier Signals for Conventional CBPWM

1.2. Problem Description in Diode Clamped Multilevel Inverters

In Diode Clamped Multilevel Inverter, the input DC voltage is shared equally by the capacitors. The output levels of the multilevel inverter depends on the switching sequence logic and discharging of capacitors. From the output voltage wave form, it can be concluded that the duration of peak voltage level is less than duration of the medium voltage levels. So, middle capacitors discharges more time when compared to the extreme capacitors [2]. From the fig.3 and fig.4, when we consider pole voltage, we can conclude that the inner capacitors discharge time to the output more than that of the outer capacitors. Therefore there will be differences in the charging time and discharging time among the extreme capacitors and middle capacitors. The outer capacitors shares the whole supply voltage which leads to double the stress across the switches and the inner capacitors discharge more and contribute to the output voltage. Therefore the difference in the voltage sharing occurs among the capacitors. As there is voltage difference among the capacitors, instabilization at the capacitor junctions arises. This instabilization also results in rise of current from capacitor junctions (called as Neutral Point Current). This contributes to the decrease in the output voltage levels. This imbalance differs with constraints like load, power factor of the load and modulation index [6] [7]. The higher the power factor the higher is the imbalance. This imbalance increases as the power factor reaches to unity because at unity power factor (UPF) the voltage and current are in phase. Similarly imbalance is very minimum at the zero power factor (ZPF). Some existing techniques which are adopted for neutral point voltage stabilization in Five-Level DCMLI namely: using Separate DC Sources (SDCS's); using Back to Back Rectifier-Inverter Connection [11]; Hybrid PWM Technique. Although every technique stabilizes the neutral point of (capacitor junction), each technique has its own major shortcoming [9]. So, this paper deals with the neutral point voltage stabilization or equalization of voltage among the capacitors in the Five-Level DCMLI with an 'Enhanced Carrier Level Shifted PWM Technique'.

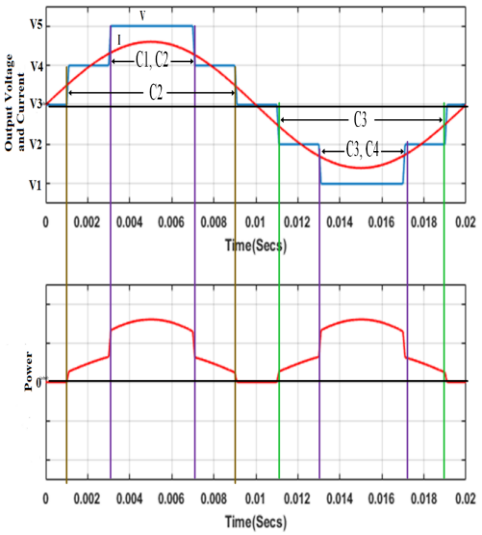

Fig. 3: Effect of switching on Capacitor Voltage imbalance for UPF Load

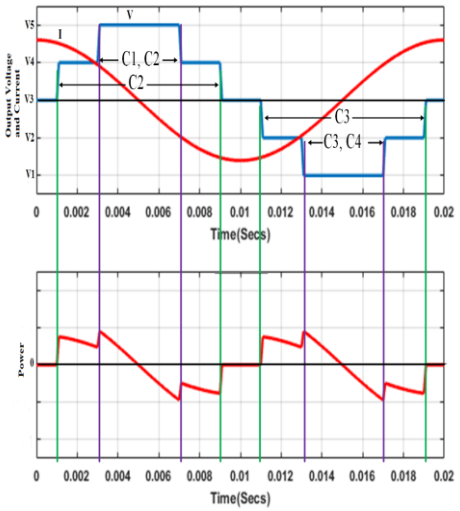

Fig. 4: Effect of switching on Capacitor Voltage imbalance for ZPF Load

2. Existing Techniques

There are techniques which are reliable for neutral point voltage balancing in three-level diode clamped multilevel inverters irrespective magnitude of load and power factor of the load. These

techniques could not solve the neutral point instabilization problem in five-level DCMLI. But there are techniques that could solve the problem in five-level DCMLI which include using Separate DC Sources (SDCS's). In this method separate DC sources, separate four transformers and four diode rectifiers are required which induce harmonics in to the supply and circuit becomes complex and costly. The other widely used technique is using back to back connection of five-level inverter and rectifier. Inspite of more redundant states offered by this configuration this uses more switches and complex control logic. After analyzing these techniques, it can be concluded that the above two techniques does not provide inherent stabilization of capacitor voltages in the five-level DCMLI. Currently there are many applications of these inverters in medium-high power drives, power quality management and renewable energy applications. Therefore, this paper proposes an "Enhanced Carrier Level Shifted PWM Technique" which provides inherent stabilization of neutral point voltage in five-level DCMLI.

3. Proposed Technique

For the stabilization of capacitor voltages in the five-level diode clamped multilevel inverter this paper proposes a novel inherent balancing technique called "Enhanced Carrier Level Shifted PWM Technique". As shown in the schematic diagram of five-level DCMLI, it has 3 junctions and 4 capacitors which makes the control complex if level shifting of reference is opted, which offers only single degree of freedom. Instead that, level shifting of carriers provide more degrees of freedom as the number of carriers proportionately increase with the level of the inverter which makes the control simple. According to this technique, shifting of carriers is done based on capacitors junction error voltage and junction current.

In this technique, the error between capacitor voltages connecting a particular junction and its corresponding current are taken as reference in determining the DC Off-set to be added. Considering junction-1, the corresponding capacitor voltages and junction currents are Vc1,Vc2,In1. Similarly for junctions 2 and 3 are Vc2,Vc3,In2 and Vc3,Vc4,In3 respectively. The DC Off-set E to be added is determined by the table:2.

Table 2: DC Off-Set Generation Table

S.No.	Sign of ($V_{Cn} - V_{Cn+1}$)	Sign of In	DC Off-set to be Added (E_n)
1.	+1 (+ve)	+1 (+ve)	-1
2.	+1 (+ve)	-1 (-ve)	+1
3.	-1 (-ve)	+1 (+ve)	-1
4.	-1 (-ve)	-1 (-ve)	+1

where n=1,2,3

3.1 Control Logic

Table 3: Switches and Carrier Signals responsible for Capacitor Voltages

S.No.	Carrier Signal	Capacitor Voltage to Balance	Switches Responsible for Capacitor Voltage		
			Phase – A	*Phase - B*	*Phase - C*
1.	Carrier -1	V_{c1}	S_{A1}, $S_{A1'}$	S_{B1}, $S_{B1'}$	S_{C1}, $S_{C1'}$
2.	Carrier – 2	V_{c2}	S_{A2}, $S_{A2'}$	S_{B2}, $S_{B2'}$	S_{C2}, $S_{C2'}$
3.	Carrier – 3	V_{c3}	S_{A3}, $S_{A3'}$	S_{B3}, $S_{B3'}$	S_{C3}, $S_{C3'}$
4.	Carrier – 4	V_{c4}	S_{A4}, $S_{A4'}$	S_{B4}, $S_{B4'}$	S_{C4}, $S_{C4'}$

The fig.5 shows the control logic to balance the capacitor voltages in the five-level diode clamped multilevel inverter. As per the control logic, the TABLE:3 illustrates the switches and carrier signals responsible for balancing the corresponding capacitor voltages.

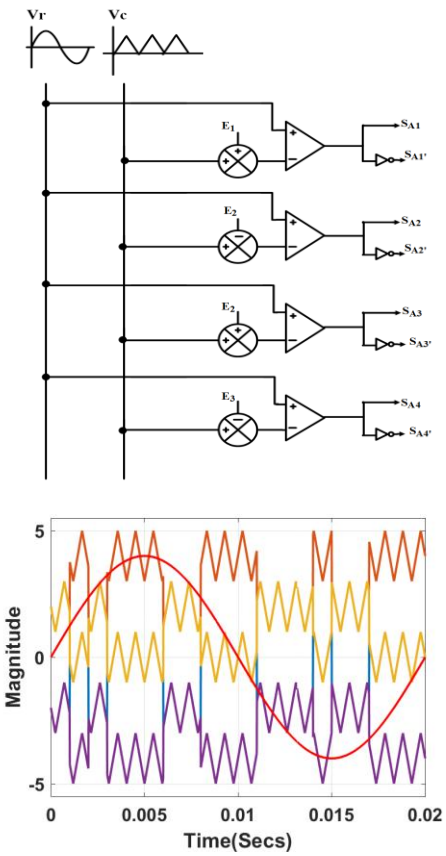

Fig.. 6: Reference and Carrier Signals for Proposed PWM Technique.

According to the control logic, the DC Off-sets (E_n) generated as per the TABLE:2 are added to the carrier signals which corresponds to the respective switches i.e., Carrier-X is responsible for pulses of switches SAX,SBX,SCX and their complementary switches(where X=1,2,3,4). These carrier signals are shifted above or below according to the given DC Off-set as shown in the fig.6. These shifted carrier signals are compared with the reference signal to generate the switching pulses for all switches in three phases.

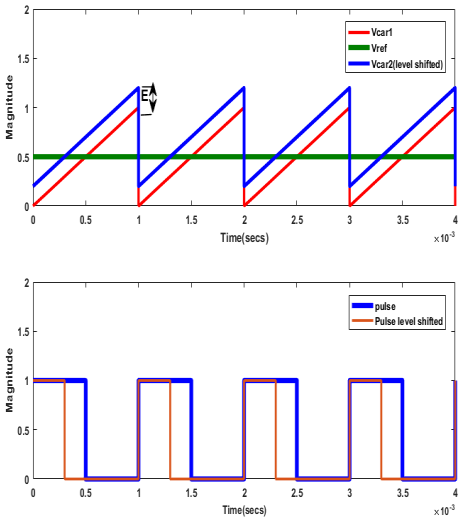

Fig. 7: Variation in pulse width due to added DC Off- set

Due to the level shifting of the carriers, the width of the pulses vary as shown in the fig.7. As the width of the pulses vary, the ON duration and the OFF duration of the switches vary. This alters the charging time and discharging time of the capacitors. The control logic is selected such that the pulse width of the switch which

controls the over charged capacitor is of long duration and that of the under charged capacitor is of short duration. Thereby the over charged capacitor discharges and the under charged capacitor charges until they share the DC bus voltage equally. So that the desired output levels are maintained.

4. Results and Discussions

The performance of the conventional CBPWM technique and the proposed 'Enhanced Carrier Level Shifted PWM technique' are compared in terms of capacitor voltage balance and output voltage for a 5-level DCMLI which is operated with Vs=1000V,a load of 0.8 pf and UPF at m_a=1.

4.1 Conventional CBPWM Technique

When five-level DCMLI is subjected to conventional CBPWM technique, the whole DC bus voltage is shared by the two extreme capacitors equally and the inner capacitors discharges completely, as shown in the fig.8 and fig.10, within a certain duration of time depending on the load pf. Because of this phenomenon, the level of the inverter decreases from 5 to 3 which can be observed from the load line voltage waveforms shown in the fig.9 and fig.11.

4.1.1 Conventional CBPWM Technique with pf = 1.0

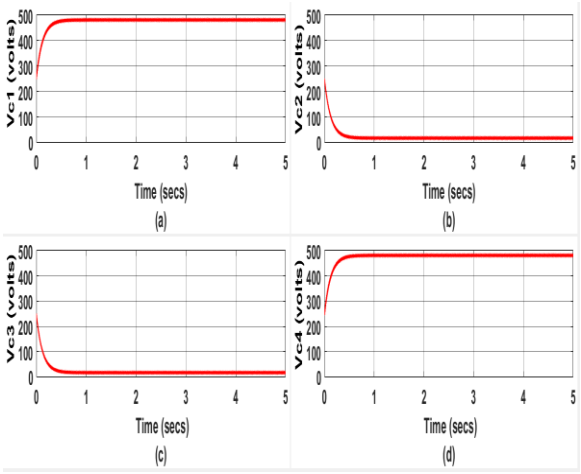

Fig. 8: Capacitor Voltages with Conventional CBPWM Tech. with UPF Load

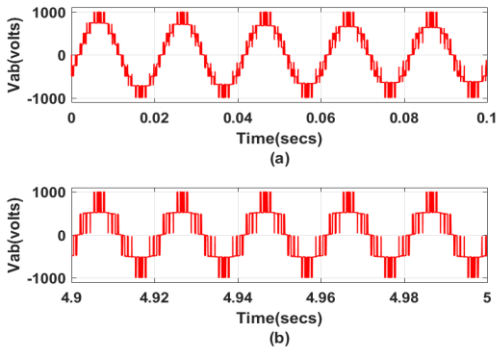

Fig. 9: Line Voltage with Conventional CBPWM Tech. with UPF Load

4.1.2 Conventional CBPWM Technique with pf = 0.2 lag

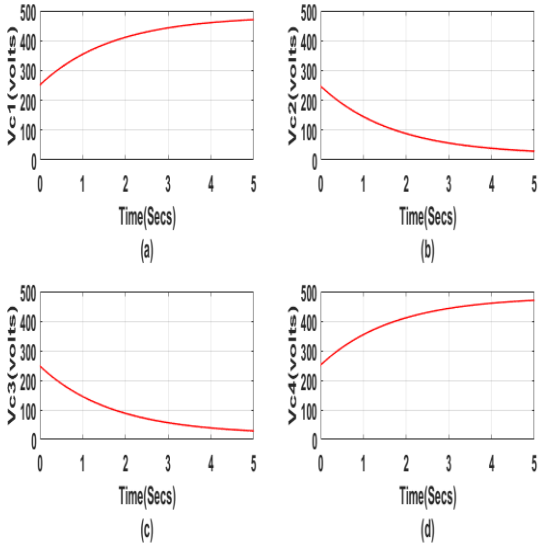

Fig. 10: Capacitor Voltages with Conventional CBPWM Tech. with 0.2 Lag Load

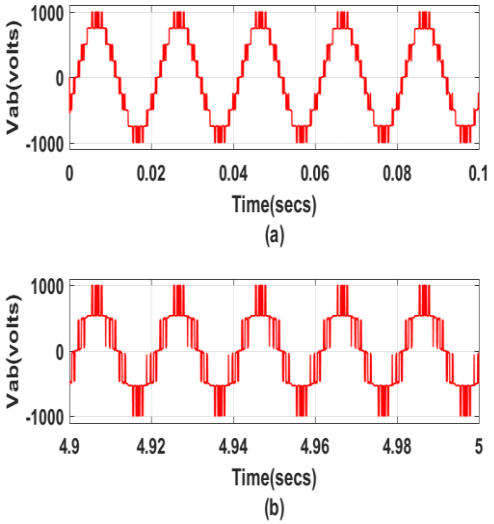

Fig. 11: Line Voltage with Conventional CBPWM Tech. with 0.2 Lag Load

4.2 Proposed Technique

When five-level DCMLI is subjected to proposed Enhanced Carrier Level Shifting technique, it can be witnessed from the fig.12 and fig.14 that the capacitor voltages are balanced which results to sustain the level of the inverter as 5-level as shown in the fig.15. When the load voltage waveform of Conventional CBPWM technique which is shown in the fig.9 and fig.11 is compared with the load voltage waveform of proposed Enhanced Carrier Level Shifting technique which is shown in the fig.13and fig.15, we can notice that the five levels of the inverter are regained which is a sign that the capacitor voltages are balanced with the proposed technique.

4.2.1 Proposed Enhanced Carrier Level Shifting technique with pf = 1.0

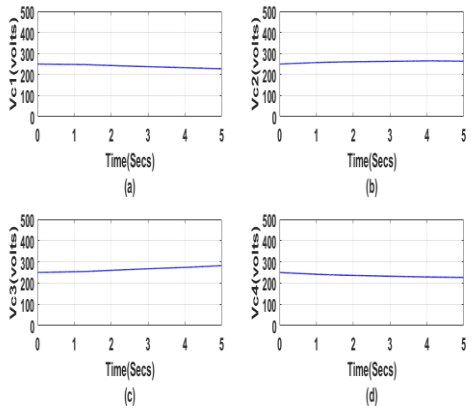

Fig. 12: Capacitor Voltages with Proposed PWM Technique with UPF

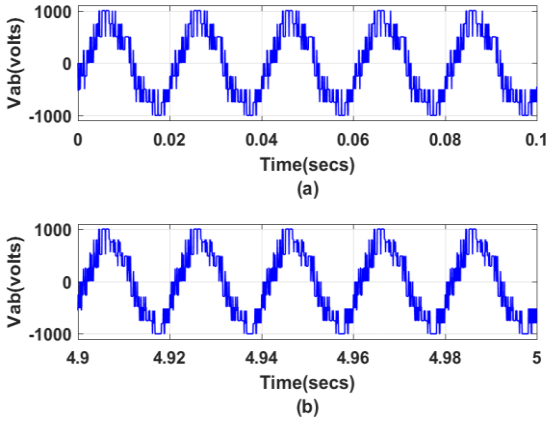

Fig. 13: Line Voltage with Proposed PWM Technique with UPF Load

4.2.2. Proposed Enhanced Carrier Level Shifting technique with pf = 0.2 lag

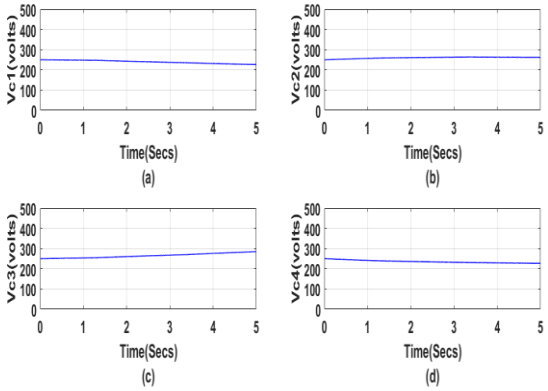

Fig. 14: Capacitor Voltages with Proposed PWM Tech. with 0.2 Lag Load

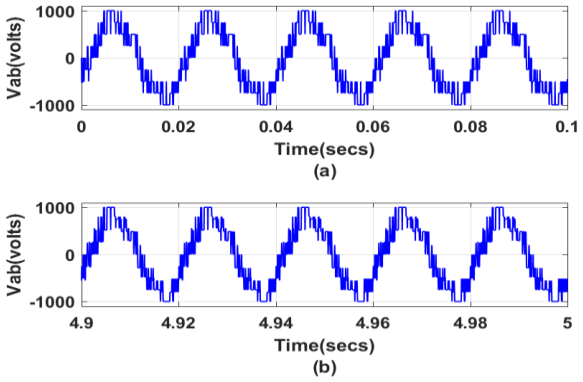

Fig. 15: Line Voltage with Proposed PWM Technique with 0.2 Lag Load

From the above waveforms, we can observe that capacitor voltages are balanced thereby the five levels in the inverter output are achieved and sustained.

5. Conclusion

In the present scenario of emerging technologies, energy conservation has high significance. Diode Clamped Multilevel inverters can contribute a great share in saving the power in medium and high power applications. These inverters save more energy in renewable energy conversions, medium and high power drives and enhancement of power quality when compared to the conventional inverters. These inverters are prominent practically only upto 3-level. The major problem, which is being suffered by these inverters, is the imbalances in the capacitor voltages as the level of the inverter increases. If this problem is rectified, then multilevel inverters could find many major applications. So, the proposed Inherent Enhanced Carrier Level Shifting technique in this paper for 5-level DCMLI is relatively simple in employment which stabilized the capacitor voltages to the major extent. There by sustaining 5-levels in the output voltage of the inverter with an improved THD performance for all modulation indexes.

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