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Research paper

Implementation of Phase Locked Loop for FM Demodulator Circuit

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Abstract

This paper aims to implement the phase locked loop for the FM demodulator circuit in Intermediate frequency band. Implementation of the proposed design is done using Simulink; further simulation is presented using Matlab as well as a comparative analysis of VCO parameters using charge pump, linearized and baseband are discussed. Charge pump based PLL design achieved phase noise of -120 dBc/Hz at 10 MHz offset frequency. Paper also presented FM demodulated output for 5000 kHz sampling frequency and 2000 KHz carrier frequency at 50 Hz deviation frequency. Simulation results are reported in tabular and graphical form.

Keywords: *Phase Locked Loop; Fast Fourier Transform; Voltage Controlled Oscillator; Frequency Modulation; Intermediate Frequency*

1. Introduction

The Phase-locked loop (PLL) is broadly used in recent communication-based applications. The telecommunication industry has greatly increased the request for low-cost devices at various ranges of frequencies to obtain the demanding applications. As a result, the performance of high speed, low voltage, and power consumption becomes a great challenge to PLL designs. The paper focuses on FM demodulator circuit using a phase locked loop which can be used to achieve high performance in the latest applications. High frequencies are not normally needed for most of the PLL based FM demodulator devices. That's why this paper focuses on applications on the intermediate frequency of the system. In a given system, PLL is used to show the two signals phase difference, and the capability to detect it. The loop frequency can be control by phase error and its differences. The output can be taken as control voltage or filtered output of VCO. Its output is applicable for the clock generation purpose and frequency demodulation purpose [1]. PLL design model using charge pump, linearized and baseband based methods are focused in this paper with comparative analysis [2]. In the PLL circuit, phase comparator compares the phase of two input signals and generates a voltage accordingly. Input and output variables use phase and frequency of the signal as shown below.

$$\varphi_{out}(t) = \phi_{in}(t) + cons. \quad (1)$$

$$\omega_{out}(t) = \omega_i(t) \quad (2)$$

Where

$\varphi_{out}(t)$ = Output Phase = $\phi_{in}(t)$ ‹Input Phase ‹

$\omega_{out}(t)$ =Output frequency and

$\omega_i(t)$ =Input Frequency‹

ω_0 = Output Frequency

Error signal $V_e(t)$, proportional to the two inputs phase difference. Here G_D represents phase detector gain (V/red) [3] as given in Eq. (3). Two inputs product shows the response of the mixer circuit given in Eq. (4)

$$V_e(t) = G_D[\varphi_{out}(t) - \varphi_{in}(t)] \quad (3)$$

$$V_e(t) = A(t)B(t) \quad (4)$$

Where

$A(t) = A\cos(\omega_0 t + \varphi_A)$ =Input Signal

$B(t) = B\cos(\omega_0 t + \varphi_B)$ =Input Signal

In PLL circuits, low pass filter is used as a loop filter, which passes the only low-frequency output of phase detector & blocks high-frequency jitter. The transient response of the filter depends upon the pole-zero magnitude of the system. The value of pole-zero in this filter can verify the type of PLL system [4]. Whereas in PLL applications, the VCO is treated as a linear, time-invariant system. The excess phase of the VCO is the system output. $\omega_{out}(t)$ is the angular frequency of VCO.

Its frequency ω_0 is set to nominal when the control voltage is zero.

1.1. PLL FM Demodulator

PLL system can be used as an FM demodulator, AM demodulator, frequency synthesizer, clock recovery, and time distribution system. In proposed work, it is used as an FM demodulator. Its basic model is shown in Fig. 1.

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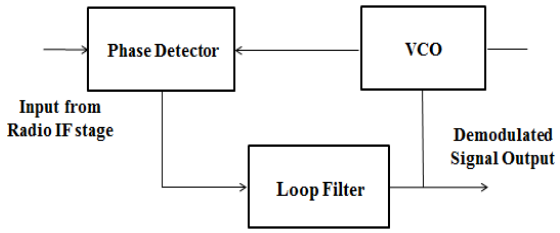


Fig. 1: PLL FM Demodulator.

1.2. Phase noise of Charge Pump PLL Design

The model represents the phase noise of PLL design, which is based on frequency, phase, and amplitude of the input and output signals. Detail analysis of this is shown in results. Noise analysis is given by

$$V_0(t) = [V_0 + A(t)]Cos[f_0 t + \varphi(t)] \quad (5)$$

Where

$V_0(t)$ = Desired peak amplitude,

$A(t)$ = Time-varying amplitude instabilities,

f_0 = frequency of the desired signal and

t = time in seconds.

Eq. (5) and (6) shows $\phi(t)$ signal, which is the source of the noise. For descriptive purposes, it is considered that the FM frequency would be higher carrier frequency [4] - [7]. Phase noise of this circuit is shown as

$$\varphi(t) = \frac{\Delta f}{f_m} \sin \omega_m t \, \varphi_m = \varphi_p \sin \omega_m t \quad (6)$$

Where, $f_m = \frac{\omega_m}{2\Pi}$ is the modulation frequency.

The peak phase deviation is $\phi_p = \frac{\Delta f}{f_m}$ also called the frequency modulation index.

2. PLL functional model

Fig. 2 shows the functional model of all kind of PLL circuits like charge pump, baseband, and linearized PLL .A PLL charge pump is merely a bipolar switched current source. The output of it could be positive and negative current pulses into the PLL loop filter. It cannot produce higher or lower voltages than its power and ground supply levels .The Baseband PLL section is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal .

Unlike the PLL block, this block uses a baseband method and does not depend on a carrier frequency .This model consists of an integrator used as a phase detector and filter circuit which specifies the filter's transfer function using the numerator and denominator parameters[8]-[12]. For VCO designing, researchers need to specify the sensitivity parameter of the VCO . This parameter ‹ measured in hertz per volts, which is a scale factor that determines how much the VCO shifts from its quiescent frequency. Below Fig. 2 shows a PLL functional model.

2.1. FM demodulator using PLL

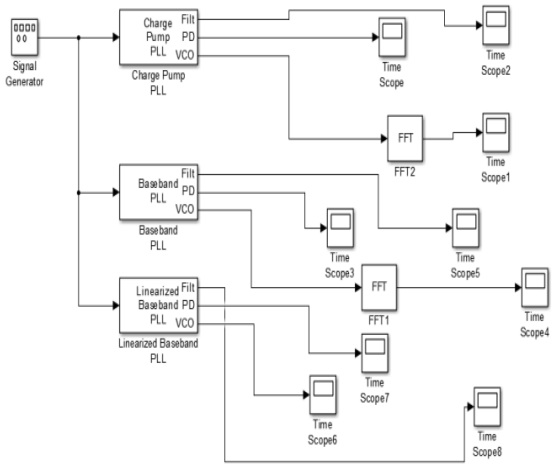


Fig. 2: PLL Functional Model.

FM demodulated output using a PLL circuit is proposed in this paper. Modulated output is coming from FM modulator to the mixer circuit which mixes the VCO output and modulated signals. The Continuous-Time VCO device generates a frequency shift signal from the quiescent frequency parameter ‹which is proportional to the applied input signal. If the input signal is $a(t)$ ‹then the output signal is given by

$$y(t) = A_c \cos(2\Pi f_c t + 2\Pi k_c \int_0^t a(t)dt + \phi) \quad (7)$$

Where,

A_c is the output amplitude,

f_c is the quiescent frequency and

k_c is input sensitivity.

Result of the mixer will be fed to the 2-D FIR filter, which filters the high-frequency signals and passes the low-frequency signal to the amplifier circuit. 2- Dimensional FIR filter design shows the input/output relationship in Eq. (8), (9) [13–[15]. T1 and T2 are the sampling time period, which is left out for the simpler design of the equation as given in Eq. (10). h (n1, n2) signifies the impulse response of the filter, and is defined over a window of size (2N1+1) (2N2+1) centered at the origin; x (n_1, n_2) is the 2-D input signal to the filter. If x (n_1, n_2) = 0 for (n_1 < 0) (n_2 < 0). Z-transform showed in Eq. (9).

$$Y(n_1, n_2) = \sum_{K_1=-N_1}^{N_1} \sum_{K_1=-N_2}^{N_2} h(k_1, k_2) x(n_1 - k_1)(n_2 - k_2) \quad (8)$$

$$Y(z_1, z_2) \sum_{K_1=-N_1}^{N_1} \sum_{K2=-N2}^{N_2} h(k_1, k_2) X(z_1, z_2) z_1^{-k_1} z_2^{-k2} \quad (9)$$

This filter response having the order ($2N_1$+ 1) * ($2N_2$+2). In most application, we set N_1=N_2=N. The frequency response of the 2-D filter can be calculated from Eq.10. After getting various responses of frequency, signals fed to the amplifier circuit.

$$H(\omega_1, \omega_2) = \sum_{K_1=-N_1}^{N_1} \sum_{K2=-N2}^{N_2} h(k_1, k_2) e^{-j(\omega_1 k_1 T_1 + \omega_2 k_2 T_2)} \quad (10)$$

This circuit amplifies week signals and passes demodulated output to the spectrum analyzer. At the end FM detector or demodulator, the response is fed to the receiver circuit [16] - [19].

3. Results and discussions

FM demodulated output using PLL is shown in Fig. 3. Sampling rate F_s for a given device is 5000 KHz with a difference of 500 samples as shown in graph and carrier frequency F_c is 2000KHz, respectively time period would be 0.5 microseconds deviation and frequency would be 50Hz. Due to a change in carrier and sampling frequency, the FM demodulator response may get change. For PLL based FM demodulator circuit, charge pump technique would be better than other techniques as analysis of all type of methods have been discussed in Table 1 and 3.

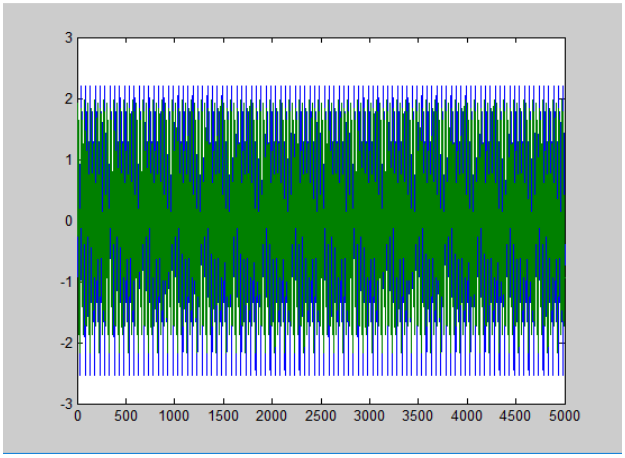


Fig. 3: FM Demodulated Output Using PLL.

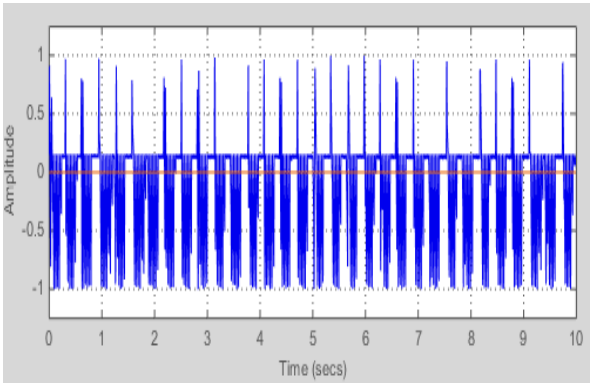


Fig. 4: FFT Response of VCO for Charge Pump PLL Design.

Fig. 4, 5 and 6 shows the FFT response of VCO circuit for all PLL designs (Charge pump, Linearized, and Baseband). Results have been represented using the FFT algorithm. This algorithm plays a vital role in signal processing based system. All the system based parameters computed accurately using this algorithm and shown in table 3 as well as analysis has been done in time to the frequency domain and vice versa.

Table 1 represents a comparative analysis of charge pump type PLL design with previously reported work. Phase noise parameter found

-120 dBc/Hz which is improved than earlier work. This work shows higher processing speed with lock-in time in the nanosecond range and higher lock-in frequency range. Whereas Table 2 shows detail analysis of VCO parameters for PLL based FM demodulator circuit which shows amplitude, initial phase, sensitivity and sampling time of the circuit. Apart from that detailed analysis of VCO is discussed in

Table 3 for all the types of PLL designs like charge pump, baseband and linearized.

Charge pump type design requires high voltage up to 147.477 mv, which is higher than baseband and lower than linearized method similarly its low voltage range, would be lower than other designs as well as input sensitivity is higher than others, quiescent frequency is only required by charge pump PLL, rest designs having not compulsion for this frequency range.

Table 1: Comparative Analysis of Charge Pump PLL

S. No.	Analysis parameters	This work	Previously reported work [8]
1	Phase Noise	-120dBc/Hz	-89 dBc/HZ
2	Offset Frequency	11MHz	8MHz
3	Initial Speed	1000	850
4	Lock Range	0.667GHz-2GHz	0.756GHz- 1.9GHz
5	Lock time	198ns	204ns

Table 2: VCO Parameters for PLL Based FM Demodulator

S. No.	Parameters	Values
1	Output Amplitude	1 Volt
2	Sensitivity	5 Hz/Volt
3	Initial Phase	20
4	Sample time	10

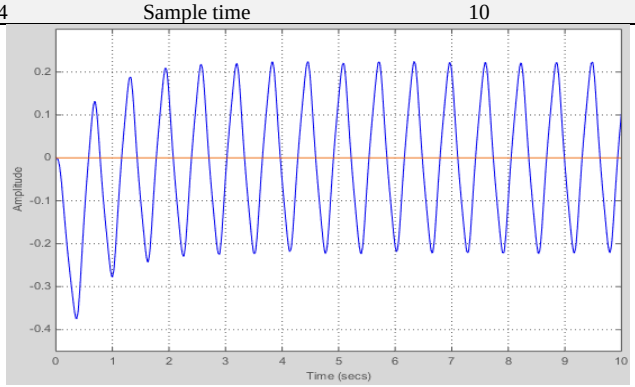


Fig. 5: FFT Response of VCO for Linearized PLL Design.

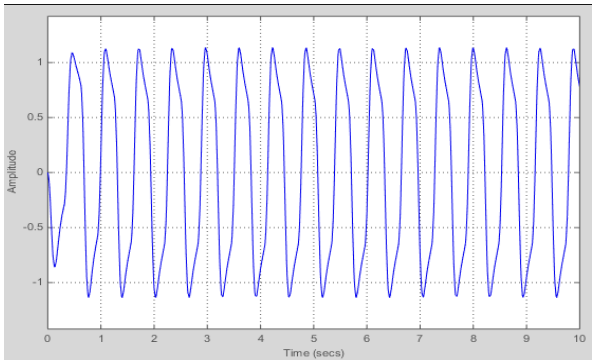


Fig. 6: FFT Response of VCO for Baseband PLL Design.

Table 3: Comparative Analysis of VCO for PLL Modeling

S. No.	Parameters	Charge Pump PLL	Baseband PLL	Linearized PLL
1	High voltage range of VCO	147.477mv	601.711mv	1.394v
2	Low voltage range of VCO	-990.001mv	-596.445mv	-1.356v
3	Amplitude of VCO signal	1.137v	1.198v	2.750v
4	Rise time of signal	7.873ms	206.236ms	65.647ms
5	Fall time of the signal	17.730ms	205.818ms	64.793ms
6	Quiescent Frequency of VCO	300Hz	-	-
7	Input Sensitivity	10	5	1

4. Conclusion

This paper presents a design of PLL in the communication-based system as a frequency demodulator circuit for IF frequency range, which is having sampling frequency @ 5000 KHz and carrier frequency @ 2000 KHz for 50 Hz deviation. Simulink analysis of all the basic types of PLL design like charge pump, baseband and

linearized PLL circuit shown here as well as a comparative analysis of charge pump method has been discussed in table 1.
Phase noise of this method is -120 dBc/Hz ، which is improved than previously reported work whereas VCO parameters have been also discussed in table 2 and 3 at 10 MHz. It is observed in this work, that charge pump based PLL design method is more useful than other methods in recent communication-based applications.

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