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Research paper

Synthesization of Low power Folded Tree Digital Signal Processor Architecture for WSN Applications

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Abstract

To monitor the execution of Wireless Sensor Network (WSN) applications effectively, different parameters like pressure, viscosity etc., to be measured accurately. A unique WSN environment is to be established through radio communication. The main requirement for this is high energy consumed wireless network sensor nodes. This paper presents unique design of low power folded tree architecture for wireless network sensor's data processing through parallel prefix operations and data localization equipment.

Keywords: *Wireless sensor network nodes, low power Folded-tree, Parallel prefix operations.*

1. Introduction

Wireless sensor network node comprises of several components like a radio transceiver encapsulated with integrated antenna. Sometimes they can be connected with an external antenna. A microcontroller, an integrated electronic interfacing circuit with the sensor embedded with the form of energy harvesting. A sensor node may be resized to the size of grain of dust which is almost similar to genuine microscopic dimensions and the sensor's cost which are variable depending on the complexity of individual sensor network nodes, communication protocol standard.

1.1 Motivation

To reduce power consumption and radiation effects in conventional Digital Signal Processor architecture and WSN. A low cost implementation of Digital Signal Processor for WSN to reduce the complexity of the network.

1.2 Existing System

Earlier existing system uses binary tree method. The bottleneck of this method is only one node act as root node at a time. The second drawback is the remaining nodes acts as leaves. Thus, only one data will be sent at a time. As a result power statistics and energy statistics and time requirements will be enormously enhanced along with interconnection complexity [1-4]. The proposed system consumes less power and energy even after enhancing of interconnection complexity. Due to all these reasons, we selected the folded tree mechanism to develop a novel approach to transmit the data using wireless means of communication techniques.

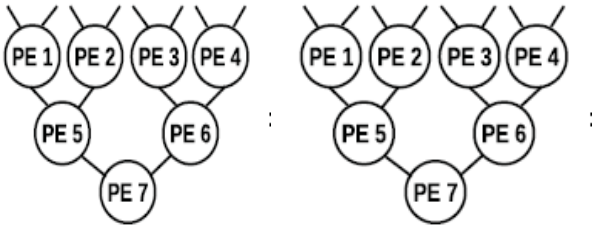


Fig.1: Binary tree

1.3 Proposed System

The proposed system processes the nodes and converts the readings in to a useful sample values. We applied the parallel prefix calculations by considering common denominator for various existing algorithms. The objective of this paper is to deduce a novel approach for a low energised wireless DSP processor used for data communication.

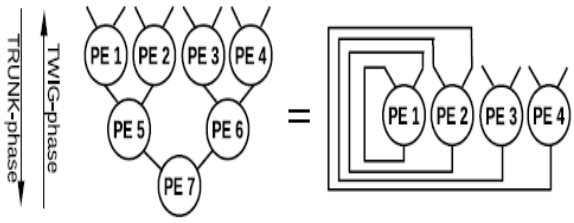


Fig.2: Binary tree reuse as Folded tree

In the proposed concept, we adopted the concept of "on the node operations performed on the collected samples from different sensor nodes directly. This procedure involves filtering , fitting, sorting and searching as usual. Previously proposed prefix algorithms evolved in terms of common denominator. But the tree folded

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flow algorithms will process on data path of programmable PEs and the same provides ease and compatibility along with prefix phenomenon.

1.3.1. Parallel prefix operations

In the operations of parallel prefix algorithm inputs A, B are added, which comprises of three stages

(i) PG logic stage bit wise,
(ii) Propagate Generate logic stage with group of bits ,
(iii) An addition stage.

The outputs of the PG stage bitwise are (Pi = Ai ⊕Bi and Gi = Ai ・Bi) are treated as (Pi , Gi)-couples to the group PG logic stage, which implements the following expression:

(Pi , Gi) ◦ (Pi+1, Gi+1) = (Pi ・Pi+1, Gi + Pi ・Gi+1) (1).

It can be shown this operator has an identify element I = (1, 0) and is associative.

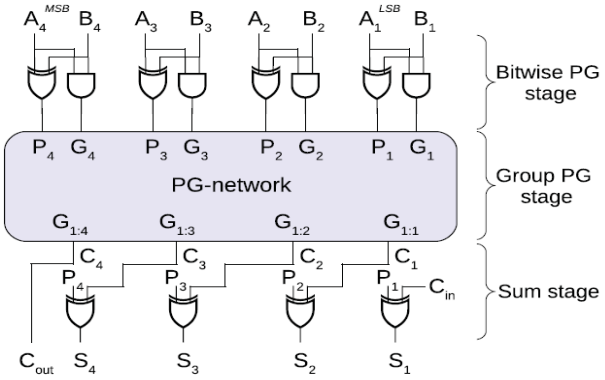


Fig.3: Addition with propagate-generate (PG) logic

The above figure explains the propagate generate logic where the addition of digital pair is done through the PG group network using prefix operations and the corresponding set of results are evaluated through blelloch's procedure to calculate prefix element and the same require two phases they are Trunk phase and Twig phase shown in below figure 4

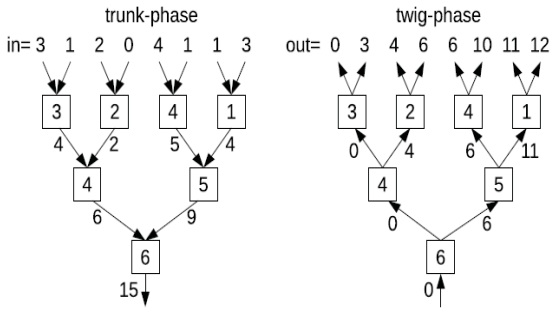


Fig.4: Trunk phase and Twig phase

In the trunk phase left value is added to the right value and the same is forwarded to the root and the same is continues till it founds the prefix element. In twig phase the data movement will be in opposite direction which is from root to leave level.

1.3.2. Programming using folded Tree

Generic patterns are having unique characteristics and had few rules used to model the folded tree data base depending on the activity, data type which are explicitly reasonably robust and are easy to understand. Generic pattern modelling makes data modelling flexible and prevents data errors with reference to change in the application environment.

2. Software Requirements

2.1. Xilinx

Integrated software development platform Xilinx opens, migrates projects and converts the same in to a navigation file after due simulation run. Project navigator will migrate the verilog instructions related to the folded tree instructions through following executive steps. They are

(a)Migrating a project

Advanced integrated software environments Xilinx suits are automatically converts our project instructions which is developed in ISE 5,ISE 6 environment in to an advanced ISE 12 project instructions and consumes very less number of simulation cycles.

(b) Creating a Project

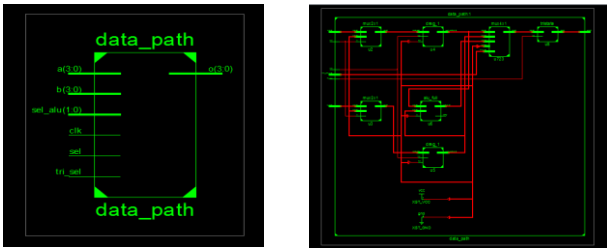
Venture Navigator permits us to do with FPGA and CPLD plans. This consists the entire source records and settings as per our requirement. We should make a task at the initial position. We should include source documents and set procedure properties. Then we should run procedures after undertaking to execute, compel, and break down your configuration. This project carried out on Verilog coding as it is an user friendly language.

3. Results and analysis

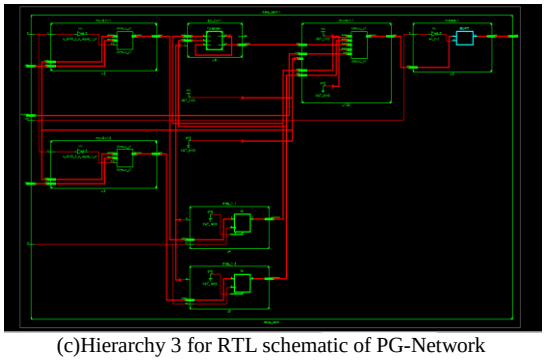
Results at various hierarchy and simulations are followed in this section.

3.1 Propagate Generate (PG) Network

RTL schematic of PG-Network



(a) Hierarchy 1 of PG- Network (b) Hierarchy 2 of PG-network



(c)Hierarchy 3 for RTL schematic of PG-Network

Fig.5: RTL Schematics different Hierarchies of Propagate Generate network

The above figures show the RTL schematics of PG network. The hierarchy 1 of PG-network consisting of two inputs (a & b) and one output (o) and also it having the clock & selection inputs. Here Tristate buffer logic was used in Group PG state. In this PG-network, we used multiplexer (2x1 & 4x1) operations & full adders. The clear connection of this PG-network is shown in above Hierarchy 2&3.

Technology schematic of PG-network

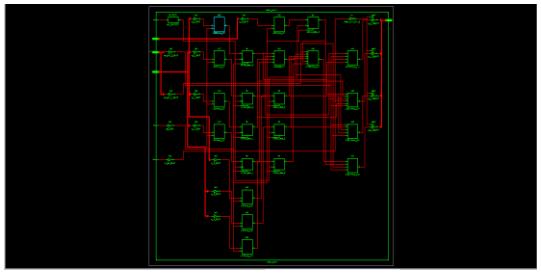


Fig.6: Technology schematic of PG-network

The technology schematic of PG-network having many look up tables (LUTs).These LUTs are used for performing the logic operations.

Simulation result of PG-network

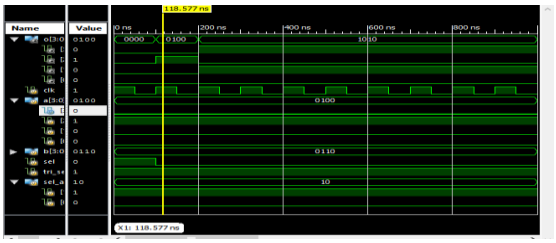
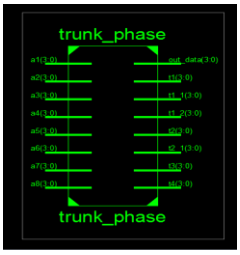


Fig.7: Simulation result of PG-network

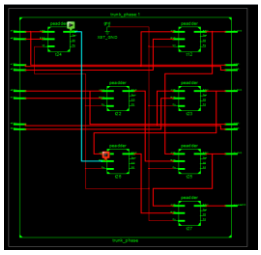
The simulation result shows inputs and outputs in the form of wave forms. For example "a & b" considered as 0100 & 0110 respectively, then the out will be 0100. It is shown in above figure.

3.2 Trunk Phase

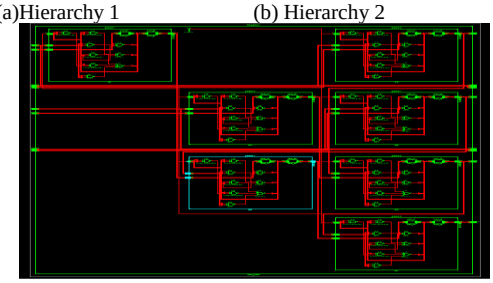
RTL Schematic of Trunk phase



(a)Hierarchy 1



(b) Hierarchy 2



(c) Hierarchy 3 for RTL schematic of Trunk phase

Fig.8: RTL Schematic of Trunk phase

The above figure shows the RTL schematics of Trunk phase. In this trunk phase if you want to perform 8 input binary operations we require 7 Prefix Element (PE) adders. The connection between these PE adders is shown in Hierarchy 2 & 3.

Technology Schematic of Trunk phase

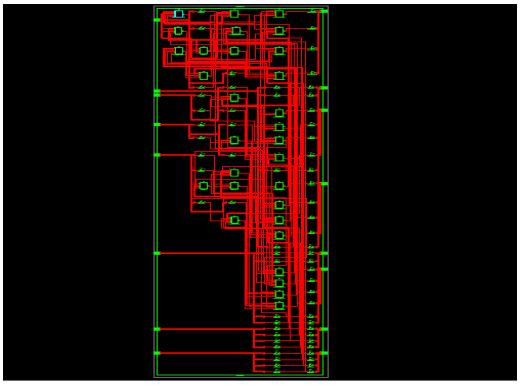


Fig.9: Technology schematic of trunk phase

The technology schematic of Trunk phase having many look up tables (LUTs).These LUTs are used to performed the logic operations.

Simulation result of Trunk phase

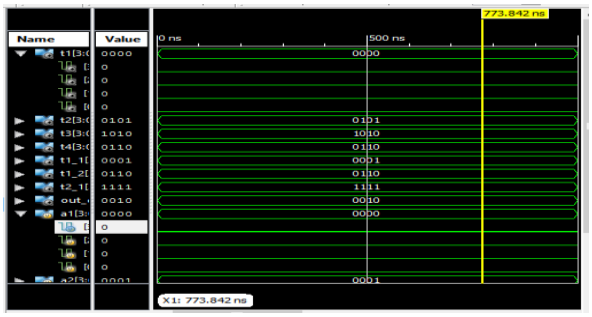
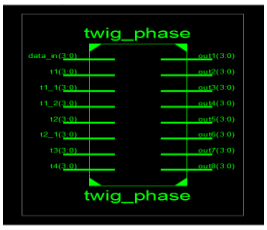


Fig.10: Simulation result of trunk phase

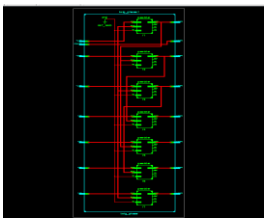
In the trunk phase initially 8 inputs are applied 4 PEs each prefix element having two inputs. The output of each prefix element connected to input of next prefix element. The PE adder performs the addition of left and right side values, resultant output value will be stored at root of the prefix element.

3.3 Twig Phase

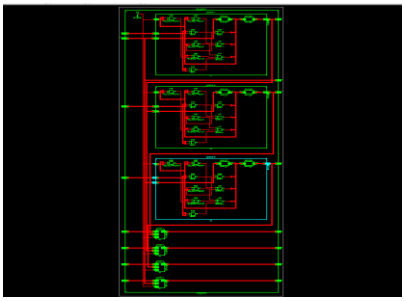
RTL schematic of Twig phase



(a) Hierarchy 1



(b) Hierarchy 2



(c) Hierarchy 3 for RTL schematic of Twig phase

Fig.11: RTL Schematic of Twig Phase

The above figures show the RTL schematics of Twig phase. In this twig phase If you want to perform 8 input binary operation we require 7 Prefix Element (PE) adders. The connections between these PE adders are shown in Hierarchy 2 & 3.

Technology schematic of Twig phase:

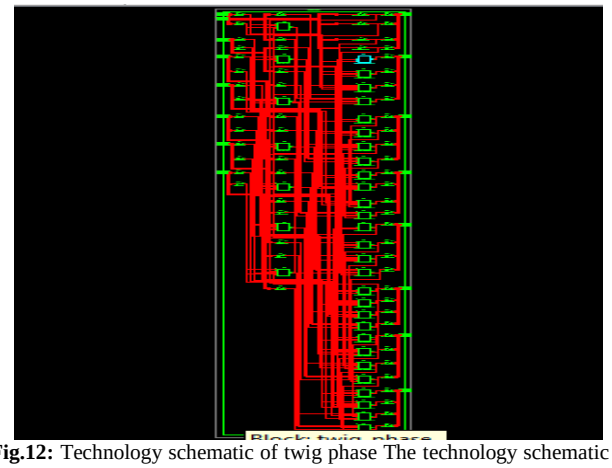


Fig.12: Technology schematic of twig phase The technology schematic of Twig phase having many look up tables (LUTs).

These LUTs are used to performed the logic operations.

Simulation result of Twig phase:

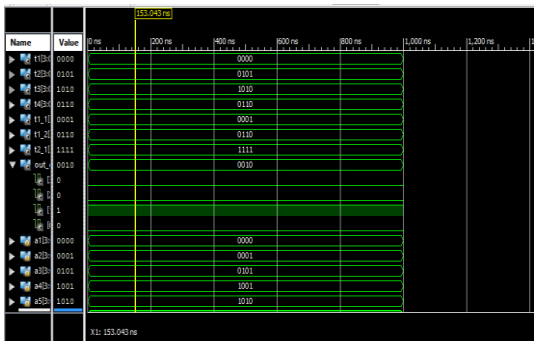


Fig.13: Simulation result of twig phase

The arrived value from this is transmitted towards left child with respect to the condition that it should begin the sum identity element 0 at the root. This value along with the previously saved Lsave will be transmitted towards right child. This process continued up to displayed inputs. The twig phase output shown in above wave forms.

4. Advantages and Applications

4.1 Advantages

- High density of the produced at low cost .
- Compact in size and integrated system approach
- High energy efficiency, long durability of power during function
- Complexity in routing reduces.
- Flexibility in performing physical partitions.
- Suitable to support various non reachable areas like overseas, deep forest regions, desserts...etc.
- Interfacing complexity is very less.

4.2 Applications

Applications of wireless sensor network are in:

- Surveillance applications oriented systems are furnished with image and video sensors in order offer more safety, security and alert the surroundings through warning and the same systems may be used in tracking, identification of vehicles.
- The development of new technologies and communication networks create new needs and functionalities in high speed data internet paths [5].
- Monitoring of industrial activities such as manufacturing, controlling, testing of instruments are done through wireless sensors in order to increase more safety to industrial surroundings and to human lives
- WSN sensors performs accurate monitoring operation on crop management to increase the crop yield and the same will support the farmers in multi-dimensional to improve the quality process in the harvesting.
- Home making appliances are embedded with several WSN sensors to make house in to a smart home and to monitor the activities of home through advanced communication protocols.
- Meteorological department warns and secures the manmade environments and avoids the disasters like natural or manmade disasters i.e. wildfires, sand storms, sea storms.WSN sensors also monitors various chemical or biological hazards and provides early warnings to the surroundings which are in effected zones.

5. Conclusion

We presented a novel approach named as the folded tree architecture for WSN applications of a DSP processor. This design used to exploit the many data processing algorithms by using parallel prefix operations. This approach intended to limit the data set by pre-processing. It also helps in reuse of the binary tree to act as a folded tree. The future Scope of this project is the end of architecture router is included. It is used to reduce the delay as well as congestion.

Acknowledgement

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References

[1] P. Sanders and J. Traff, “Parallel prefix (scan) algorithms for MPI,” in Proc. Recent Adv. Parallel Virtual Mach. Message Pass. Interf., 2006, pp. 49–57.
[2] G. Blelloch, “Scans as primitive parallel operations,” IEEE Trans. Comput., vol. 38, no. 11, pp. 1526–1538, Nov. 1989.
[3] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. Reading, MA, USA, Addison Wesley, 2010.
[4] J. Backus, “Can programming be liberated from the von neumann style?” in Proc. ACM Turing Award Lect., 1977, pp. 1–29.
[5] Shaik. Mahaboob Basha and B. C. Jinaga, “A robust approach for qualitative compression in JPEG 2000 standard,” 2012 Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, Hyderabad, 2012, pp.224-228.