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Research paper

A Comparative Study between Phase Disposition PWM(PDPWM) and Phase Opposition Disposition (PODPWM) for Cascade H-Bridge, Flying Capacitor and Neutral Point Clamped Multilevel Voltage Source Inverters (MVSIs)

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Abstract

In this paper a comparative study between two types of switching PWM signals namely Phase Disposition PWM (PDPWM) and Phase Opposition Disposition PWM (PODPWM) for three types of Multilevel Voltage Source Inverter (MVSI) are conducted. The selected MVSI topologies are cascaded H-bridge, flying capacitor and neutral point clamped MVSI. In general, the THD of the output voltage and current can be improved as the levels of MVSI inverters are increased. However, as the levels of outputs are increased the numbers of circuit components are also increased. As a result, this will increase the circuit complexity for the MVSI to be operated at high levels. From the study, it can be found that cascaded H-bridge inverter required the lowest number of circuit components and has better THD compared to the other two topologies of MVSI for the similar output voltage and current levels. Moreover, the proper selection of PWM control strategy technique between PDPWM and PODPWM for MVSI is also able to reduce the THD in the output waveform. The circuit simulations for the MVSIs are simulated with MATLAB/SIMULINK simulation software.

Keywords: *Use about five key words or phrases in alphabetical order, Separated by Semicolon.*

1. Introduction

AC/DC converters are power electronic device that are commonly used as they found in many consumer electronic devices [1]. They can be grouped into two types: the voltage source inverters (VSIs) and the current source inverters (CSIs) as illustrated in Figure 1. The employment of these two types of inverter depends on their application. Generally, they have to be light and small which mean the components inside the inverter must be less. Besides, they need to produce low harmonics and have a simple switch control to operate at high efficiencies. Over the past, multilevel power inverter have been used in several applications such as motor drive, battery chargers, power factor correctors, active filters and interface with alternative energy sources, among many others [2][3][4]. The three types of multilevel voltage source inverters (MVSI) such as cascade H-Bridge (CHB), Flying Capacitor (FC), Neutral Point Clamp (NPC) have the same problem, which is the rapidly increase in the number of circuit components when increasing the output level of inverter and have complexity in term of circuit controllers[8][9][10][11]. In general, the switching control strategy for MVSI consists of two modulation methods. The methods used are fundamental switching frequency and high switching frequency as shown in Figure 2. The function of modulation control technique for MVSIs is to control the gating signals of the power switches and to reduce the total harmonics distortion at the output voltage and current waveforms [5]. Space vector PWM, Selective Harmonics Elimination PWM and Sinusoidal PWM are in the group of high switching frequency and among these; Sinusoidal PWM is the popular one which is always been used in the design because this PWM method is simple and easy to be implemented in multilevel inverter[6][7]. In this study, two type of sinusoidal PWM technique were been studied and compared namely Phase Disposition PWM (PDPWM) and Phase Opposition Disposition PWM (PODPWM) in order to improve the performance of MVSIs [7].

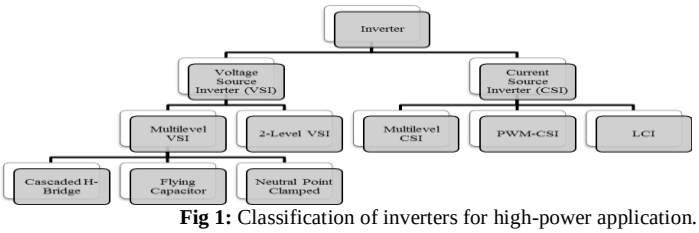


Fig 1: Classification of inverters for high-power application.

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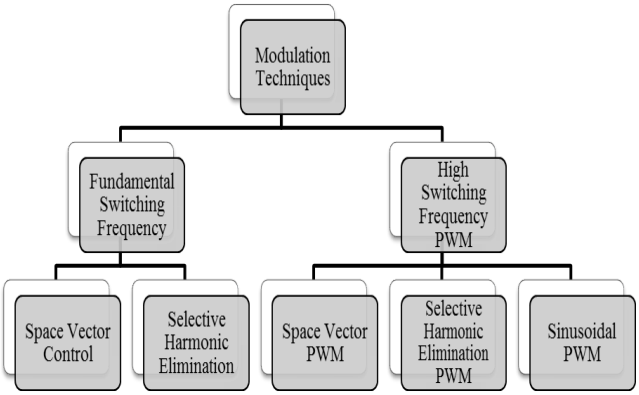


Fig 2: Classification of Multilevel Modulation Methods.

2. Methodology

2.1. 5-level MVSI Circuits for CHB, FC and NPC

Figure 3, 4, and 5 show the circuit structures for three different type of MVSI constructed in MATLAB/Simulink. Figure 3 shows Cascade H-Bridge MVSI, Figure 4 shows Flying Capacitor MVSI and Figure 5 shows Neutral Point Clamp MVSI respectively. These circuits are constructed for the 5-level output voltage. In Figure 3, two identical single-phase H-bridge inverters connected in a string where each of the bridge is separately supplied with a DC voltage sources. At the output voltage side, there are five different voltage output +2Vdc, +Vdc, 0, -Vdc and -2Vdc can be produced by this configurations with different combinations of switching sequences for the eight switches in the inverter. In the analysis, DC voltage for each H-bridge DC voltage is set to be 100V so that the total input is 200V DC.

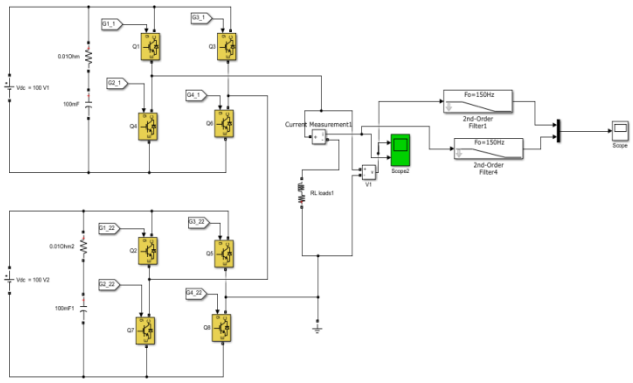


Fig 3: Cascade H-Bridge (CHB) MVSI

From the figures, it can be seen that CHB MVSI topology uses the least number of power electronic switches compared to other two topologies. Hence, it can reduce the switching and conduction losses for the power switches. However, two DC sources employs in this topology greatly increase the cost for the circuit structures. In addition, Figure 4 shows single- phase circuit configuration for single-phase 5-level flying capacitor MVSI. It can be seen that, this topology needs an additional capacitors to be clamped in between switches. These additional capacitors are formed in a ladder structure such that every capacitor branch brings different value of voltages. In Figure 5 shows the neutral-point clamped MVSI configuration for 5-level voltage output. This topology required diodes to be clamped in between switches (upper and lower). In addition, four number of capacitors are required where the value of voltage across them is +Vdc/4. Four series-connected capacitors are function to divide the dc-bus voltage value into four quarter value (Vdc/4). Second order harmonic filter is employed in each topology in this project in order to reduce the harmonic voltages and currents in the converter circuits so that the comparison in term of THD performances can be made for each topology.

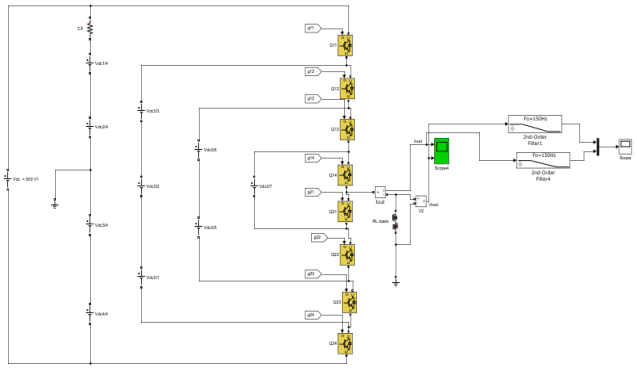


Fig 4: Flying capacitor (FC) MVSI

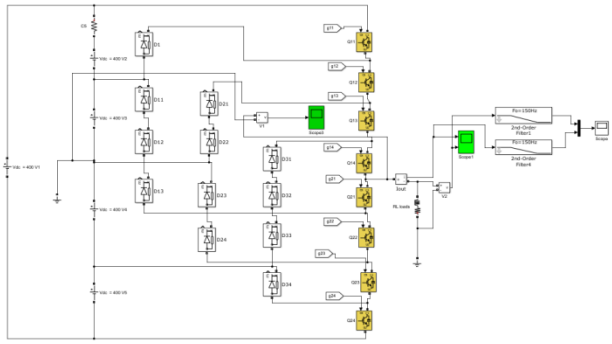


Fig 5: Neutral Point Clamp (NPC) MVSI

2.2. PWM modulation schemes for CHB, FC and NPC MVSI

In this study, high switching frequency SPWM modulation technique with Phase Disposition PWM (PDPWM) and Phase Opposition Disposition PWM (PODPWM) are employed for the MVSI. The performance comparison of THD between these two types of SPWM modulation techniques are made during the analysis. In general, the PDPWM has been widely used in multilevel modulation. In the operation of PDPWM, several carrier signals with single modulating waveform are used [7]. The frequency and the amplitude of all the carrier waves in this method are identical. This technique requires $K - 1$ carrier signals in order to produce K level inverter output voltage. For example, in 5-level inverter, 4 carrier signals are used to apply this type of modulation technique as shown in Figure 6. In PDPWM, the amplitude, carrier frequency and phase for all the carrier wave signals are identical. Figure 6 illustrated the PDPWM controller circuit for 5-level MVSI whereas Figure 7 illustrates the PODPWM controller circuit for 5-level MVSI respectively. In contrast with PDPWM, the PODPWM has phase shift of 180^0 for the carrier waves for the negative cycle operation as shown in Figure 7.

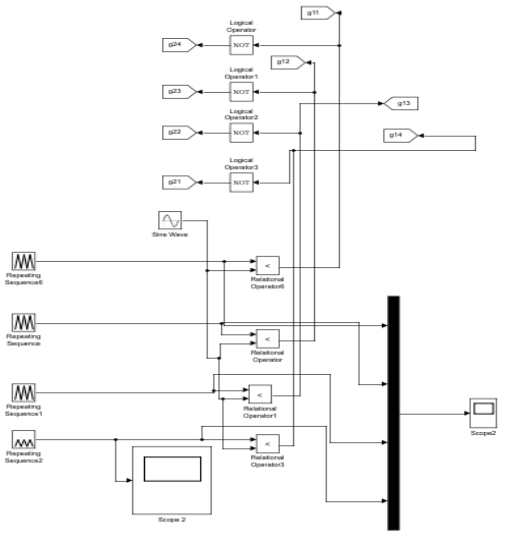


Fig 6: POD PWM 5-level MVSI

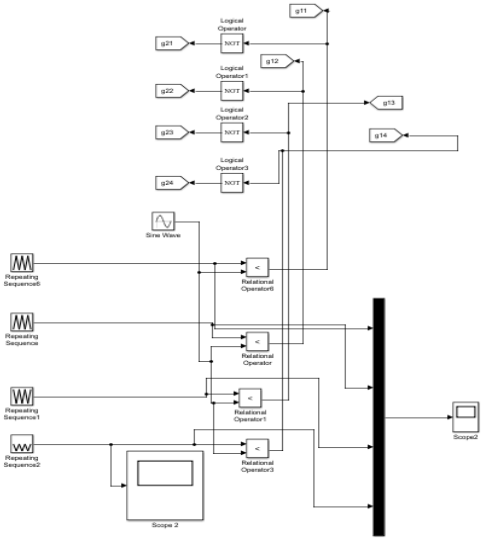


Fig 7: PODPWM for 5-level MVSI

3. Simulation results and discussion

3.1. Different levels of output voltage waveforms

Figure 8, 9, and 10 show the output waveforms for the Cascade H-Bridge MVSI for 5-level, 7-level and 9- level. The waveforms for other topologies for each level of output voltage are identical with these figures. From the figures, it can be concluded that as the level of output voltage is increased from 5-level to 9 - level, the output voltage waveform for the inverter becomes more nearer to sinusoidal waveform. This indicates that, at high level of MVSI, the THD is significantly reduced. Hence a much smaller size of output filter can be used in the circuit. In Figure 11, the sinusoidal output waveform of voltage can be obtained after filtering out the THD by the harmonic filter.

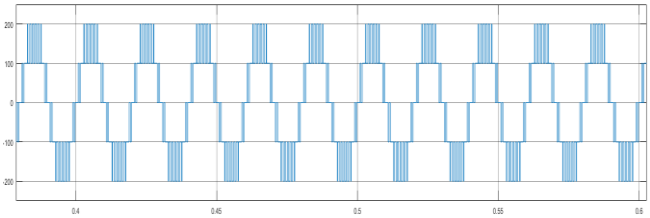


Fig 8: Output voltage waveform of 5-level cascaded H-bridge.

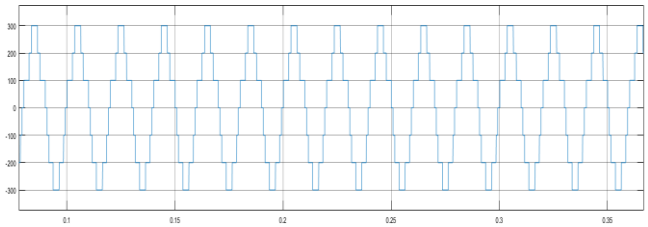


Fig 9: Output voltage waveform of 7-level cascaded H-bridge.

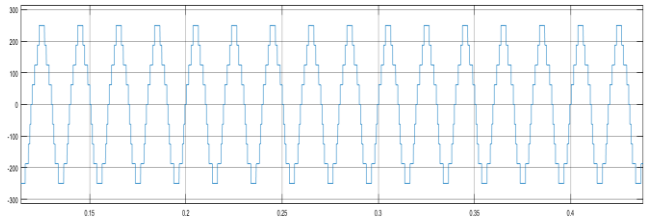


Fig 10: Output voltage waveform of 5-level cascaded H-bridge.

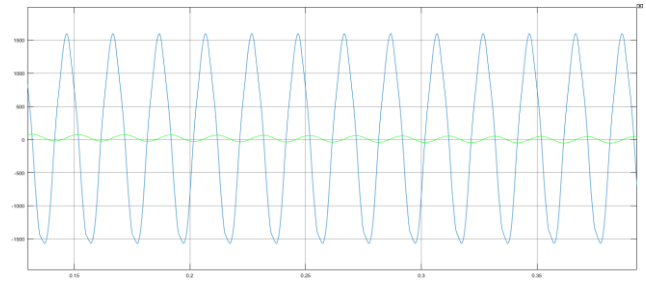


Fig 11: Output voltage waveform after filter.

3.2. PD PWM modulation scheme

Figure 12, 13 and 14 show the carrier waveforms for PDPWM in order to produce 5-level, 7-level and 9-level output current waveforms respectively.

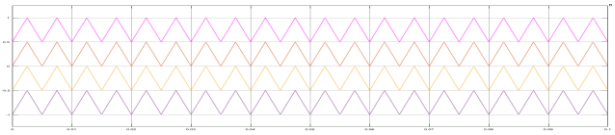


Fig 12: 5-level PDPWM carrier waveforms

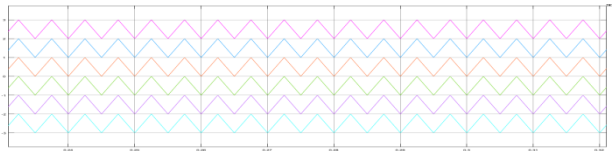


Fig 13: 7-level PDPWM carrier waveforms

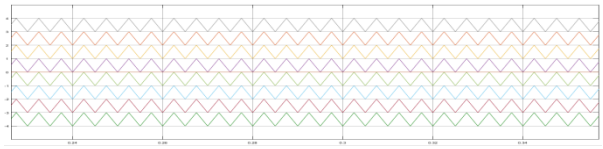


Fig 14: 9-level PDPWM carrier waveforms

3.3. POD PWM modulation scheme

In the PODPWM, all carriers have the same frequency and amplitude however the carriers below zero axes are shifted 180° from the carriers above zero axes. Figure 15, Figure 16 and Figure 17 show the configuration for the carriers waveform for different level of output voltage [6].

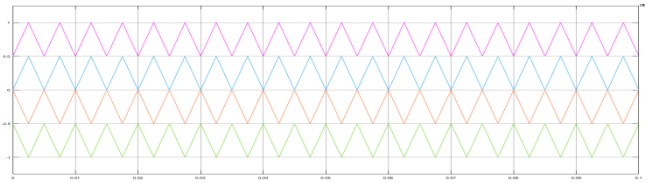


Fig 15: 5-level PODPWM carrier waveforms

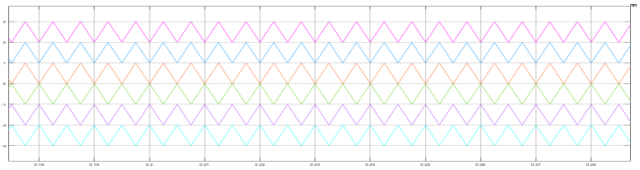


Fig 16: 7-level PODPWM carrier waveforms

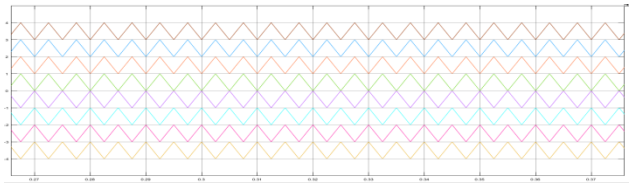


Fig 17: 9-level PODPWM carrier waveforms

3.4. THD level analysis for PD PWM and POD PWM

The THD levels of output voltage for 5, 7 and 9 level are tabulated in Table 1 for each MVSI topology. From the results, it can be seen that by increasing the level of each inverter topology from 5-level to 9-level, the percentage of THD reduced significantly. In term of THD level reduction for the topologies, as can be seen from Table 1 and Table 2, the CHB MVSI has the lowest THD values recorded compare to NPC MVSI and FC MVSI. In addition, it also can be observed that the percentage of THD value for PDPWM is lower than PODPWM for most level of topologies. As conclusion for this analysis, the recorded results show that PDPWM produces better results for THD analysis.

Table 1: THD for PDPWM

Level	CHB (%)	FCM (%)	NPC (%)
5	37.89	37.92	38.07
5 (FILTERED)	1.19	1.24	1.26
7	19.38	21.11	22.03
7(FILTERED)	7.31	7.90	7.89
9	12.61	13.12	12.94
9(FILTERED)	4.05	4.44	4.33

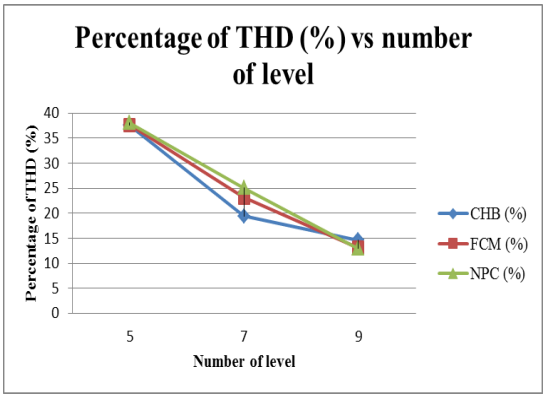


Fig 18: Percentage of THD for PDPWM

Table 2: THD for PODPWM

Level	CHB (%)	FCM (%)	NPC (%)
5	37.51	37.97	37.85
5 (FILTERED)	1.28	1.31	1.39
7	22.28	22.31	22.29
7(FILTERED)	7.40	7.93	7.97
9	13.77	14.47	13.86
9(FILTERED)	4.39	4.55	4.77

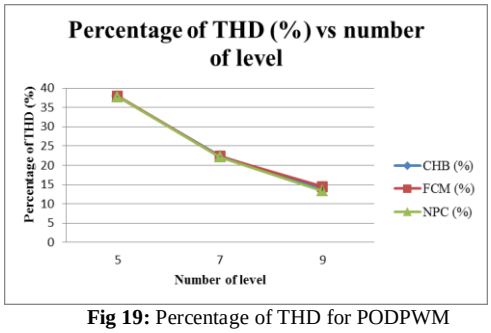


Fig 19: Percentage of THD for PODPWM

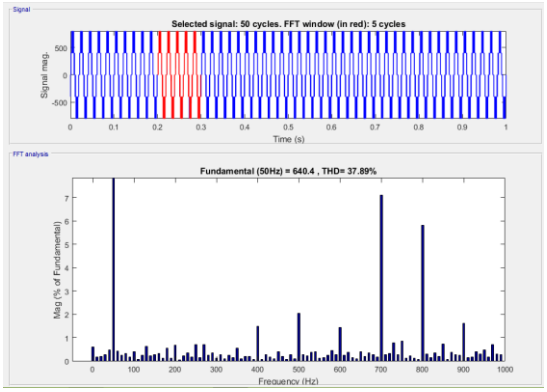


Fig 20: THD for 5-level CHB MVSI before filter with PDPWM

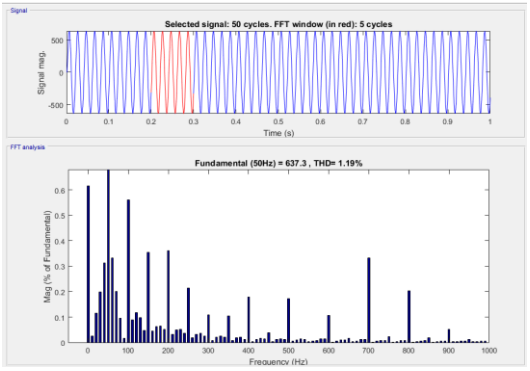


Fig 21: Percentage of THD for 5-level CHB MVSI after filter with PDPWM

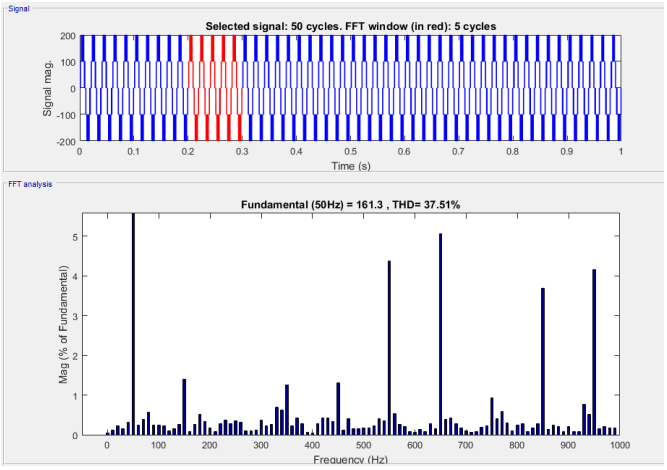


Fig 22: THD for 5-level CHB MVSI before filter with PODPWM

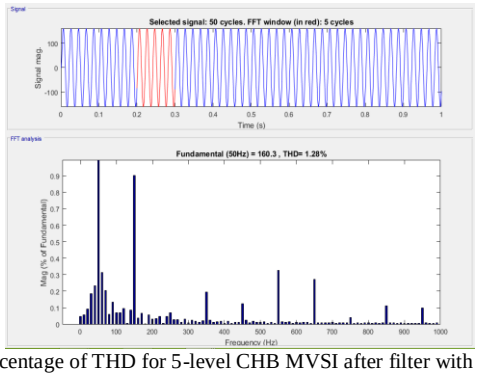


Fig 23: Percentage of THD for 5-level CHB MVSI after filter with PODPWM

3.5. Number of circuit components

Table 3 tabulated the general formulas to calculate the total number of component needed for CHB, FC, and NPC. It can be conclude that from the recorded data in Table 4, Table 5 and Table 6, the number of components in cascaded H-bridge circuit is the lowest compared with other two topologies as the level of output increased from 5-level to 9-level.

Table 3: General formula to calculate no of components

Topology / Components	Cascaded H-bridge	Flying Capacitor	Neutral Point Clamped
Switches	2(k-1)	2(k-1)	2(k-1)
Clamping diode per phase	0	0	(k-1)(k-2)
DC bus capacitors	(k-1)/2	(k-1)	(k-1)
Balancing capacitor	0	(k-1)(k-2)/2	0

Table 4, Table 5 and Table 6 present the total number of components requires for each of topology for 5-level, 7-level and 9-level respectively. As can been seen from the Table 4, for a 5-level inverter, cascaded H-bridge only requires a total of 10 components which is less than the other topologies. In addition, for the higher level of output voltage 7-level and 9-level, the CHB MVSI also has the lowest total component numbers compare to two other topologies.

Table 4: Number of component for 5-level

Topology / Components	Cascaded H-bridge	Flying Capacitor	Neutral Point Clamped
DC source	2	1	1
Switches	8	8	8
Diode	0	0	12
Capacitor	0	4	4
Total	10	13	25

Table 5: No of component 7-level

Topology / Components	Cascaded H-bridge	Flying Capacitor	Neutral Point Clamped
DC source	3	1	1
Switches	12	12	12
Diode	0	0	30
Capacitor	0	6	6
Total	15	19	49

Table 6: No of component 9-level

Topology / Components	Cascaded H-bridge	Flying Capacitor	Neutral Point Clamped
DC source	4	1	1
Switches	16	16	16
Diode	0	0	56
Capacitor	0	8	8
Total	20	25	81

4. Conclusion

The comparative study analysis between the two types of PWM modulation method has been investigated for three types of MVSI topologies. From the results, the level of output THD for PDPWM is better lower the level of THD for PODPWM. As a result, it can be expected that as the level of output voltages are increased to the higher levels, the MVSI topology that employed PDPWM can has better quality of output waveform with lower THD level. However, different topology of MVSI comes with different circuit configurations with different numbers of circuit components for the similar level of output voltage. It also can be predicted that, for the higher output level of MVSI

operation, the number of components are also increase significantly. Hence it will produce circuit complexity issues in term of component numbers, costs and the overall size of inverters. From the analysis CHB MVSI requires less number of circuit components compare to NPC MVSI and FC MVSI topologies and has lowest THD results for the same output voltage level.

Acknowledgement

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