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Research paper

Performance Evaluation of DSSC as Distributed Power Flow Controller in Transmission Network

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Abstract

Converter based FACTS controllers provides power flow control through transmission line. But due to its high cost and low reliability issues, it is not widespread installed over worldwide. Distributed FACTS provides a compensation in cost effective and reliable way in interconnected power system. Distributed static series compensator (DSSC) is one of the member of distributed FACTS family. In this paper, DSSC is demonstrated as distributed power flow controller to realize active power flow through the line. DSSC is a low power, low cost, light weight single phase inverter and it can be directly attached on the existing line with the help of single turn transformer. It injects a very small voltage in the line in quadrature with the line current which gives a negligible change in active power. Multiple devices are needed to provide on the line to get noticeable change in active power. In this work, particle swarm optimization is implemented to find optimum reactance emulated by DSSC to provide secured power system operation and control. Objective is formulated such that no line would carry line current above its thermal limits. Similarly, reactive power generation is minimized using DSSC devices considering main constraint that power flow through each line would be within its acceptable range. Voltage stability is also analyzed on DSSC compensated system. DSSC compensation in capacitive mode of operation is demonstrated for loading margin enhancement. Furthermore, fault current limiting using DSSC devices is demonstrated. MATLAB results validate the work.

Keywords: *Distributed-FACTS; Distributed Static Series compensator (DSSC); fault current limiter; Particle swarm optimization (PSO); Static synchronous series compensator; voltage stability*

1. Introduction

FACTS technology gives a new turning to power system operation and control. Very big and high complex power system urgently requires efficient and fast acting power flow controllers to provide load demand in a secure manner. FACTS technology helps to utilize existing transmission capability to its fullest extent. FACTS controllers are able to alter line impedance, bus voltage and power angle for the purpose of power flow control. Impedance type FACTS controllers uses inductor and capacitor controlled by power electronics devices. Some of the popular conventional FACTS devices are TCSC, SVC, TCPAR, TCVR. To widen control capabilities VSC based FACTS controllers are proposed such as SSSC, STATCOM, UPFC [1]. Reactive power control in power system by FACTS devices provide wide control over bus voltage, line impedance, phase angle which ultimately results in power flow control in line. Static synchronous series compensator (SSSC) is series FACTS device providing direct active power flow control through lines. It injects voltage in series with the line in quadrature to line current. It's structure consists of high power rating inverter with dc link capacitor. It is connected in series with the line through coupling transformer of high power rating [2]-[4]. Moreover, high rating insulation platforms need to provide. Hence these device is very costly and less reliable in operation. Distributed series FACTS concept proposed by Deepak Divan finds a way out to control power flow in cost effective manner. Reliability also finds increased. Distributed static series compensator (DSSC) is one of the device in distributed FACTS family. It consists of a low power series connected inverter which can be directly attached to the existing transmission line. This device is similar to SSSC in circuit and operation. Since it is a low power circuit; it injects a very small negligible voltage in series with the line emulating inductive or capacitive reactance. Effective power flow control can be achieved using number of DSSC devices connected on the line at regular intervals [5]. Distributed power flow controller design with ETO light converter is proposed by Wenchao Song, Alex Q. Huang and Subhashish Bhattacharya [6]. Emitter turn off thyristor is a high power electronic device with the additional breakthrough in turn off capability and low conduction loss and high switching speed. A series compensating distributed power flow controller consists of a ETO light modular voltage source converter of power rating 1-2 MVA to dynamically control line impedance and controls the active power flow. Zhihui Yuan, Sjoerd W.H. de Haan, Braham Ferreira presented distributed power flow controller which acts similar like UPFC [7]. DFPC consists of a shunt converter and multiple series converters. Like UPFC common dc link is not present in DPFC. Power flow between shunt and series converters is through the transmission line at 3rd harmonic frequency component. DC power required by series converters is provided by 3rd harmonic current. It is having the control capabilities to alter line impedance, bus voltage and power angle simultaneously. More studies on DSSC devices including structure, Modelling and control is presented in the literature given in reference [8]-[11].

In this research work, DSSC modeling is presented. DSSC modelling is given in section 2. Section 3 highlights PSO and objective

problem. Fault current minimization is presented in section 4 preceded by results in section 5. In result and discussion section, first DSSC is implemented in single line and active power control is achieved by optimum use of DSSC devices. Optimization problem is formulated with the objective that no line would be overloaded. It gives optimum DSSC MVA to avoid line overloads. Line overloads is also minimized using multiple DSSC devices on the line. Objective of the optimization problem is modified. It is formulated such that no line would be overloaded and it should have minimum reactive power generation. Further, Voltage stability is analyzed in capacitive mode of operation. A fault current limiter using DSSC device is also demonstrated.

2. DSSC Modeling

A distributed static series compensator uses low power single phase inverters which can be directly attached on the line with the help of single turn transformer as shown in fig.1. Multiple DSSC devices are connected on the line at regular intervals. Single turn transformer is used as coupling transformer where transmission line conductor itself acts as one of the winding of transformer. Multiple turns are given on the core which lower down the current in the inverter circuit. Hence inverter of low power rating can be used which ultimately reduces installation cost. A DC link capacitor voltage is regulated using line current itself. It takes some active power from the line to regulate dc link voltage. Inverter injects voltage in series with the line at 90^0 to the line current. If the line current is leading to injected voltage, it emulates capacitive reactance and if line current is lagging to injected voltage, it emulates inductive reactance. Line reactance altered with the help of multiple DSSC devices on the line which changes active power flow.

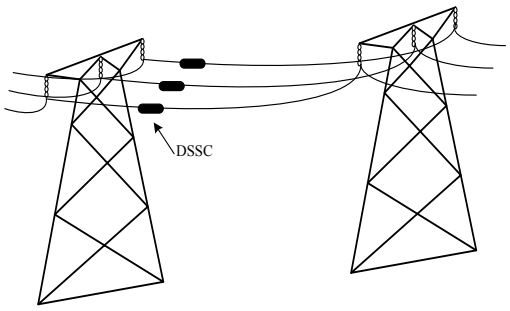


Fig.1. DSSC hanging on transmission Line

DSSC device consisting single turn transformer of high turns ratio n is connected as shown in fig.2. Power required for the control circuitry and power required to regulate dc link capacitor V_{dc} is taken from the line itself.

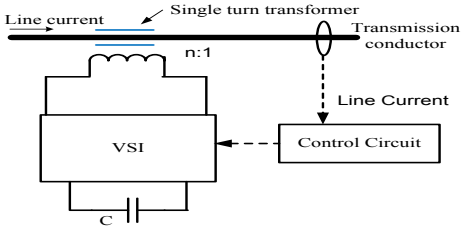


Fig.2. DSSC circuit [5]

Single phase bridge inverter output voltage is given by (1).

$$V_i = \frac{2}{\pi} V_{dc} \tag{1}$$

Fundamental component of single phase inverter output voltage can be written as,

$$V_i' = \frac{2}{\pi} V_{dc} \sin(\varpi t + \theta) \tag{2}$$

Applying instantaneous power theory, AC side instantaneous power is equal to dc side power.

$$i_{dc} V_{dc} = i_L' V_i' \tag{3}$$

where,
V_{dc} is the dc link capacitor voltage
V_i' is the fundamental component of inverter output voltage given by (2)
I_L is the line current flowing through line
I_L' is the transformed line current on dc side
which is given by (4)

$$i_L' = \frac{I_L}{n} \tag{4}$$

Current flowing in dc link capacitor circuit is as in (5)

$$i_{dc} = \frac{I_L}{n} \frac{2}{\pi} \sin(\omega t + \theta) \tag{5}$$

Voltage across dc link capacitor is regulated with the help of this current i_{dc}. Equation eq. (6) shows dc current i_{dc}.

$$V_{dc} = \frac{1}{C} \int i_{dc} . dt \tag{6}$$

Voltage V_{dc} is compared with reference dc link capacitor voltage $V_{dc\ ref}$ gives some deviation and it is forwarded to PI controller. Correction factor is terms of small angle β is obtained. Synchronizing circuit PLL provides synchronizing angle Θ.

$$\beta = \left(K_p + \frac{K_i}{s} \right) (V_{dc\,ref} - V_{dc}) \tag{7}$$

Inverter gate pulses are phase shifted by angle $\Theta + \psi \pm (90^0 + \beta)$, where angle ψ is the phase angle of line current I_L. Capacitive or inductive reactance is emulated by injecting inverter output voltage in leading or lagging to line current. As a result, effective line reactance varies and power flow can be controlled. Since DSSC device is a low power circuit i.e. ~10 kVA, it provides a very small change in the line current. Hence large number of DSSC devices are to be connected to achieve significant change in line current.

3. PSO to Find Optimum Use of DSSC

In complex power network, power system studies show that that some of the lines carrying more power as compared to others. In practical feasible conditions, this may lead to line overloading even some of the lines are still working under loaded. DSSC compensation helps to manage power flows as desired. Distributed static series compensator can be used on multiple lines to control power flow in the lines and provides inductive or capacitive compensation. DSSC devices are low power single phase devices. It injects a very small negligible voltage (~10 -15V) in series with the line at 90^0 to line current in inductive and capacitive mode of operation. Significant active power flow control can be achieved by applying large number of devices on the line. But DSSC devices on multiple lines increases installation cost of compensation. Hence it is expected to apply optimum number of DSSC compensation to make system cost effective. A particle swarm optimiza-

tion can be applied to find optimum number of devices on the line to provide cost effective compensation [12]-[15]. Objective function of optimization is written to find optimum number of devices on the line. The primary objective is to remove the overloading in the line [21],[22].

$$F = \frac{1}{n} \sum_{(Ii \geq I_{Thermal})}^{n} \left(\frac{I_i}{I_{Thermal}} \right)^{100} \tag{8}$$

In the objective function given by (8), current I_i is the actual current through line and $I_{Thermal}$ is the maximum allowable current in the line. Total number of lines is represented by n. Objective function F will be calculated for the line which are crossing their maximum allowable current limit. A small overload in the line also makes objective function higher. PSO is applied to minimize F. Emulating inductive or capacitive reactance by DSSC devices on the multiple lines can result in removing overloading in the line. PSO gives optimal emulating reactance for compensation and provides optimal number of DSSC devices to remove overloading in the line.

4. Fault in the DSSC Compensated System

A simple power system model is shown in fig. 3, it is considered for fault study. Series compensation by DSSC is provided between bus 1 and 2 having voltages V_1 and V_2 respectively. Line reactance is X_L. Voltage Vs is injected by DSSC at 90^0 to line current in order to compensate for reactance of transmission line. In normal condition DSSC injects voltage leading or lagging to line current thereby emulating inductive reactance or capacitive reactance for active power flow variation. In fault condition, DSSC injects voltage leading to line current which emulates inductive reactance thereby increasing effective line reactance. Fault current tends reducing [17]-[18]

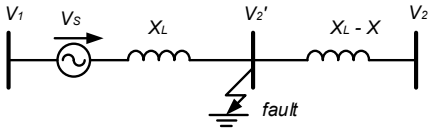


Fig. 3. System for fault studies

In the phasor diagram shown in fig. 4. V_s is the injected voltage by DSSC which is lagging to line current I, it is capacitive mode of operation of DSSC. It increases voltage across physical line. Hence power flow is increased in capacitive operation of DSSC. In normal condition, voltage across transmission line from bus 1 to 2 is given by (9),

$$V_1 - V_2 + V_s = jIX \tag{9}$$

In fault condition, voltage at faulted bus becomes zero and voltage across transmission line increases which increases fault current. In fault condition, voltage across transmission line is given by (10). Consider fault takes place at bus 2'. In fig. 5 (a) I_{fault} is the fault current when DSSC not connected. Phasor diagram in fig.5 (b) shows that if DSSC is operated in inductive mode, voltage across line would reduce which decreases fault current significantly.

$$V_1 + V_s = jIX \tag{10}$$

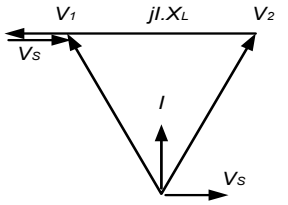
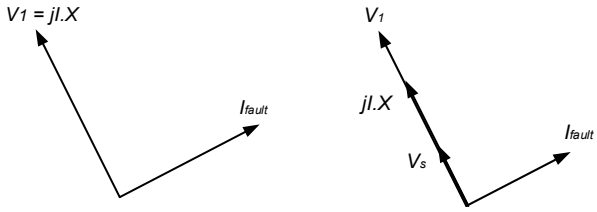


Fig.4. Phasor dia. prior to fault (DSSC in capacitive)



(a) (b)

Fig.5. Phasor diagram of system during fault (a) without DSSC (b) with DSSC in inductive operating mode

5. System Examples

DSSC studies are presented in MATLAB software [19]. DSSC applications are demonstrated and DSSC compensated system results are presented. DSSC devices on single line as well as on multiple line is demonstrated to control active power flow in the line as per system requirement. Optimum number of DSSC devices are applied so that it avoids overloading and provides cost effective power flow control. Results are presented on IEEE-14 bus test system [20]. System consists of five synchronous generators; three generators are clearly used for reactive power generation purpose only. Total load of 259 MW and 81.3 MVAR is connected through 20 transmission lines. MVA base chosen as 100 MVA and kV base 138 kV. Real power losses and reactive power losses are 13.593 MW and 56.910 MVAR respectively. For the demonstration purpose thermal limit of each transmission line is considered as 500 A. A particle swarm optimization technique is applied to find optimum number of DSSC devices on the line. Prior to that some lines are identified for placement of DSSC devices. Lines connecting buses 1 to 2 carrying more current and it is greater than assumed thermal limit of the line. Similarly, lines connecting buses 1 to 5 and 2 to 3 and 2 to 4 are also found very vibrant to change in load and may reach its thermal limit with increasing load. DSSC devices are applied on these lines. In the next part DSSC devices are applied to minimize reactive power generation. Voltage stability is also analysed on optimal placed DSSC system. All these studies are carried out on IEEE-14 bus system. A fault analysis is also studied on IEEE second benchmark system.

5.1. Power Flow Control Using Optimum Use of DSSC

Line 1 connecting buses 1 to 2 is considered for DSSC placement and operating in inductive mode. Considering each DSSC device emulating reactance of 0.000987 p.u. Line 1 is carrying current of 623 A which is higher than assumed maximum allowable current rating. This overloading can be nullified using DSSC devices in inductive mode of operation. Applying PSO maximum compensating reactance is obtained. With increased line reactance line current and active power flow is reduced. Total emulated reactance to remove overloading on line 1 is 0.09573 p.u. Line current is redistributed; Line 1 current becomes 500 A and line 2 current is increased to 421.38 A. Real power loss becomes 13.8730 MW from 13.5929 MW. Reactive power loss changed from 56.9096 MVAR to 70.09 MVAR.

To remove overloading on line 1, DSSC can also be put on line 2 connecting bus 1 to 5 and operating in capacitive mode of opera-

tion. Power flow in line 2 found raised as effective line reactance gets reduced. Reactance of 0.3316 pu is found emulated to remove overloading. Line current and active power flow is increased. Line 1 current redistribute to 499.5 A and line 2 current redistributed to 420 A. Real power loss is changed from 13.5929 MW to 13.8730 MW and reactive power loss is changed from 56.9096 MVAR to 48.88 MVAR.

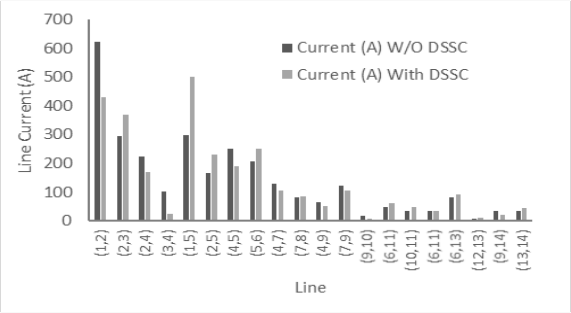


Fig. 6. Line current redistribution after optimal DSSC compensation on multiple lines

Multiple lines are selected for placement of DSSC's. Line connecting buses 1 to 2, buses 4 to 5 are selected for DSSC placement operating in inductive mode. Lines connecting buses 1 to 5, buses 4 to 5, buses 3 to 4 are selected for DSSC placement operating in capacitive mode. Emulated reactances are 49.1694 Ω, 70.3110 Ω, 32.3432 Ω, 73.2752 Ω and 52.4379 Ω. Power loss observed is 13.7302 MW. Total reactive power generation is 114.65 MVAR. Bar chart shown in fig. 6 shows redistribution of current flow in the lines after DSSC compensation on multiple lines. Percentage utilization of lines is observed. It is shown in bar chart in fig. 7. DSSC compensation provides power flow control which helps to get maximum utilization of all the lines.

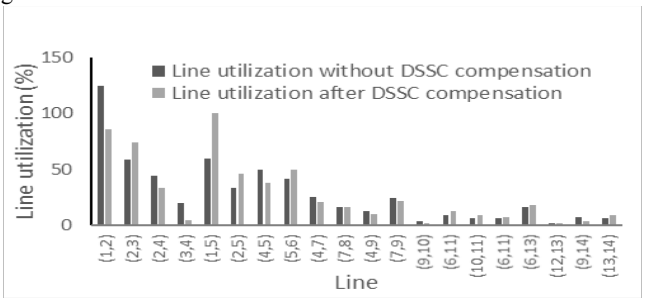


Fig. 7. Line utilization after optimal DSSC compensation on multiple lines

5.2. Voltage stability in DSSC Compensated System

Voltage stability is analysed using continuation power flow [16]. Continuation power flow is run on some of the identified buses of IEEE 14 bus system where voltage collapse may occur. DSSC devices are installed on line connecting buses such that it emulates 40% of line reactance. DSSC devices are connected on line connecting buses 1 to 5 in capacitive mode. It increases power flow through that line and decreases power flow through line connecting 1 to 2.

PV curve of bus number 14 is observed. Bus voltage variation with respect to loading parameter λ is observed as shown in fig. 8. PV curve shows that loading margin is improved in capacitive mode of operation.

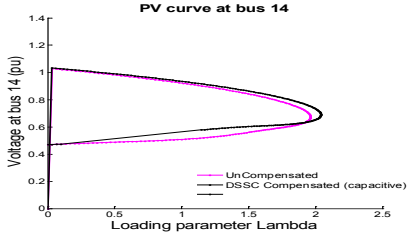


Fig.8. PV curve at bus 14 (with and without compensation)

5.3. Reactive Power Generation Optimization

DSSC helps to reduce reactive power generation and it reduces reactive power losses. In IEEE-14 bus system, out of five synchronous machines, three synchronous machines are providing reactive power generation. Out of 5 machines, generator connected at bus number 2 is supplying more reactive power. To reduce reactive power generation at bus 2, DSSC compensation is provided on line connecting buses 1 to 2 and operated in inductive mode. PSO is applied to find DSSC devices on the line to reduce reactive power generation by generator at bus 2 with the constraint that no line would be overloaded. Objective function written in (8) is modified. It is given in (11) where $Q_{g2Total}$ is the reactive power generation by generator at bus 2 which is to be minimized using PSO. Number of lines are 20 and maximum thermal rating of each line is 500 A assumed. 100 factor is shown in equation to make figure higher.

$$F = \frac{1}{20}\sum_{li\geq 500}^{20}\left(\frac{I_i}{I_{\max}}\right)^{100} + Q_{g2Total} \tag{11}$$

Using PSO, emulated reactance is obtained as 60 % of line reactance. It provides reduction in reactive power generation of generator 2 from 47.93 MVAR to 41.70 MVAR without overloading any of the lines. Table I shows reactive power generation by synchronous machines at 1, 2, 3, 6 and 8.

Table 1: Reactive power generations at buses with and without DSSC compensation

Generator Bus	Without DSSC (MW)	With DSSC (MVAR)
1	-15.23	7.13
2	47.93	41.70
3	27.76	94.20
6	23.03	23.54
8	21.03	21.27

5.4. Fault Analysis on DSSC Compensated System

IEEE second benchmark system shown in fig. 9 is considered for the fault analysis in DSSC compensated system. Transmission line 1 connecting buses 1 to 2 is selected for DSSC compensation. Line is segmented in *n* segments where *n* DSSC devices are connected at regular intervals along the line. For the study purpose, DSSC devices are connected on line 1. LLL-G fault is considered at midpoint of line 1. In the normal operation DSSC devices inject voltage in series with the line in quadrature with line current in leading or lagging mode for transmission line reactance compensation. Power flow control can be achieved significantly. In fault condition, DSSC devices are commanded to operate in lagging mode so that inductive reactance is emulated. As a result, effective line reactance is increased and reduces fault current significantly [17],[18].

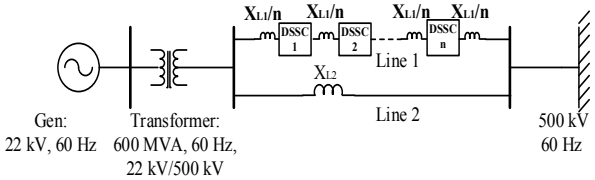


Fig. 9. IEEE second benchmark system for fault analysis

Fig. 10 shows injected voltage by one DSSC device and line current waveform in inductive and capacitive mode. Line current in normal operating condition without DSSC compensation is found 212 A. From t = 0 sec to time t = 0.1 sec, DSSC is operated in capacitive mode i.e. line current leads injected voltage. Injected voltage is 12 V rms. Line current is found 212.2 A. After time t = 0.1 sec DSSC is operating in inductive mode i.e. line current lags injected voltage. Injected voltage is 12 V (rms). Line current is

211.5 A. In inductive mode line current is reduced. Single DSSC device gives a very small change in line current.

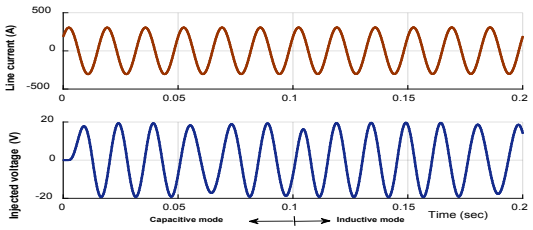


Fig. 10. line current and DSSC injected voltage operating in lagging and leading mode

Fig.11. shows fault current with and without DSSC devices. For demonstration purpose, total voltage injection by number of DSSC devices is represented by voltage 40 kV. Prior to fault, DSSC is operated in capacitive mode, line current leads injected voltage as a result power flow is found increased. Number of DSSC devices are connected injecting total 40 kV in the line. In this mode, line current is increased from 212 A to 340 A. LLL-G fault takes place at t = 0.1 sec. In fault condition DSSC is commanded to operate in inductive mode. Same 40 kV is injected by number of DSSC devices. Fault current is found reduced from 704 A to 578 A. DSSC operated in inductive mode of operation and reduces fault current in the line.

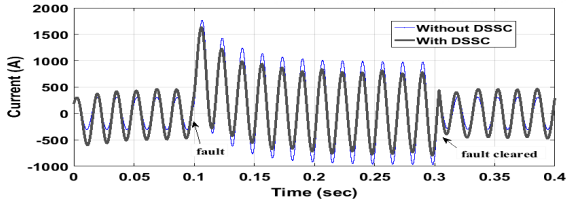


Fig. 12. Fault current with and without DSSC system

6. Conclusion

Distributed static series compensator (DSSC) devices on transmission lines are demonstrated and its performance evaluation is presented. It is proven effective compensation using DSSC. Different DSSC applications are demonstrated. Significant power flow control is obtained by using optimal use of DSSC devices connected on the line. Particle swarm optimization method is used to find optimal MVA by DSSC devices to avoid line overloading. Applied optimum number of DSSC devices on the line, redistributed power flow through lines and utilization of all the lines is found improved. Furthermore, reactive power generation is found reduced in DSSC compensated system. Voltage stability is analyzed on IEEE-14 bus system. Loading margin is found increased in capacitive mode of operation of DSSC devices. It is found that stability margin is improved in DSSC compensated system. DSSC devices on lines proved fault current limiting. Inductive node of operation of DSSC reduced the fault current.

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