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Research paper

Investigation of 6T SRAM Characteristics Using TFET

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Abstract

This paper proposes to design and investigate the SRAM memory cell features using TFET in the InAs/GaSb-InAs platform. This platform lies within the type III (Hetero-junction) alignment in TFET. The word TFET symbolizes to the Tunneling Field Effect Transistor which is related to the MOSFET but follows quantum tunneling switching mechanism. TFET having an advantage over MOSFET such as high speed, energy efficient and low power applications in the field of integrated circuits. The suggested project is the design of 6T SRAM memory cell with 32nm TFET technology. Finally, the performance estimation of the proposed SRAM has been compared with CMOS, FinFET, and CNFET. The study of the competence of the SRAM cell can be done by Hspice tool and Verilog-A language used.

Keywords: *Buffer, CMOS, Hetero junction, SRAM read/write, SRAM, TFET.*

1. Introduction

In this era, all electronics industries try to develop a compact device without their performance degradation according to Moore's law. So most of the IC developers love to design small, highly efficient, low power and compact Integrated circuits. For that, the distance between the gate and drain of the FET should be minimized. But it leads to performance degradation by short channel effects like surface scattering, drain induced barrier lowering (DIBL), power leakage and velocity saturation. These problems of sub-micron technology can be tackled by the alternative device called TFET. The compact structure of the TFET gives subthreshold swing (SS) is less than 60m V/dec. The electron flow in the TFET related to the band bending in the thin tunnel region.

In paper [1], the sub-threshold swing measured at 20m V/dec at which on-current range is 1-10n A/µm. The on-current range is maximum for below sub-threshold < 60m V/dec. Sung Hwan et al proposed a FET device with Germanium (Ge) source and they observed sub-threshold rage is 40m V/dec [2]. The reference [3] examined the characteristics of TFET during charge neutrality level (CNL) and random trap fluctuation (RTF). The researchers used nano wired array TFET and inspected better inverter performance without degradation of V_{out}[4]. The next paper compared conventional n-i-n MOSFET with p-i-p TFET. It concluded that the p-i-p TFET is apt for low power applications [5]. The FET device has two regions namely tunneling dominant and drift dominant. From [6], we state that the tunneling dominant region has a higher sub-threshold swing. This paper is systematized as follows. Section II reviews the TFET technology, its construction and model parameters, and design issues. Section III defines the SRAM cell design by TFET. Section IV synopses the simulation results and graph. At last, the conclusion and future enhancement of the paper explain in section V.

2. TFET Technology

2.1. Structure of the TFET

Tunnel FET (TFET) is a three terminal or four terminal device build on a Silicon surface. The construction of the TFET is same as MOSFET except that the source and drain having a reverse bias. Traditionally it is a PIN diode (p-type, intrinsic, n-type). The p-type as a source, n-type as a drain and the intrinsic semiconductor (Si) surface together formed the PIN diode. In which the electrostatic potential of the intrinsic controlled by the gate element. The conventional structure of the TFET was depicted in figure 1. The source and drain of the TFET are severely doped while the intrinsic semiconductor surface is weakly doped. The PIN diode is having the highest breakdown voltage and having the lowest junction capacitance. The off current of the TFET will be low because of the reverse bias of the PIN diode [7].

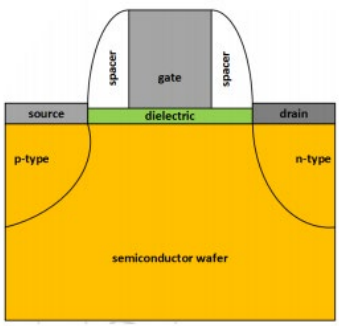


Fig. 1: Structure of the Tunnel-FET(TFET)

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2.2. Working Principle of the TFET

In conventional MOSFET, the intrinsic layer of the device plays as a barrier. So to turn on the device, the suitable voltage is given as a bias to the gate terminal. But in the case of TFET, high voltage charge gradient formed between the semiconductor surface and the p-type source, due to the dielectric region. As a consequence, the electrons from the p-type of the valence band traveled to the intrinsic region of the conduction band. Because of that, a strong band bend is formed under the sufficient gate voltage. This effect is called as a band-to-band tunneling (BTBT) [8]. The structure of the BTBT tunneling effect will be clearly explained in figure 2. The device turn on-current will be the tunneling current. Due to the special structure of the PIN diode, it attains the highest diffusion barrier that can be achieved by degenerate the doping. This is the reason for the easy scaling down of the TFET compared to the MOSFET.

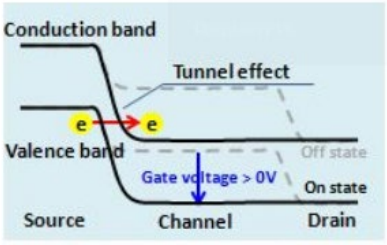


Fig. 2: Band-to-band Tunneling (BTBT)

2.3. Model Parameters of the TFET

The TFET device is using the phenomenon of quantum tunneling instead of thermionic emission. Because of that, it reaches the subthreshold swing less than 60m V/dec. But the traditional MOSFET follows Maxwell-Boltzmann relation is given by,

$$N_i = \frac{g_i}{\frac{\varepsilon_i}{e\,k_t} - \mu} \tag{1}$$

Where ε_i is the Energy of i^{th} energy level, N_i is the number of carriers in the i^{th} energy level, g_i is the degeneracy of the state i, μ is the chemical potential, K is the Boltzmann constant and t is the absolute temperature [9]. Since BTBT tunneling concept used in TFET, it achieved less than 60m V/dec.
The on-current (drain to source) of the TFET device is given by,

$$I_{ds} = \frac{\mu_n . C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 . (1 + \lambda . V_{ds}) \tag{2}$$

Where μ_n refers mobility of the electrons in the channel, C_{ox} is the dielectric capacitance, W & L is the width and length of the channel, V_{gs} is the applied gate to source voltage, V_{th} is the threshold voltage and λ refers to the channel length modulation coefficient.
If the channel length modulation coefficient is zero, the on-current relation of TFET will be,

$$I_{ds} = \frac{\mu_n . C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \tag{3}$$

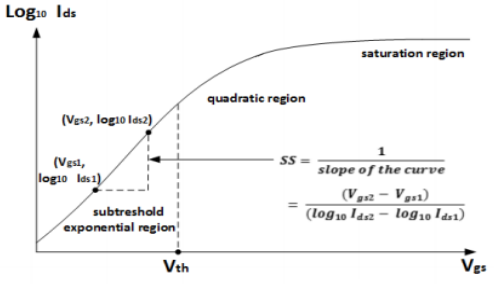


Fig.3: Calculation of Subthreshold Swing

Subthreshold slope (SS) is defined as the gate voltage mandatory for revising the drain to source current by one decade. The subthreshold swing can be determined from the I-V graph by $\log I_{ds}/V_{gs}$ in the subthreshold exponential region shown in Fig 3. The conceptual value of subthreshold swing is assumed by,

$$SS = \frac{\partial \log I_{ds}}{\partial V_{gs}} \approx \frac{2.3\,.n.k_B.T}{q} \tag{4}$$

2.4. Challenges of the TFET

Sometimes in TFET, non-uniformity is occurring due to vacancies and impurities in dopants. The consequences of the non-uniformity add electron/holes in the band gap resulting degradation in steep SS. The next challenging factor is the scaling parameter [10]. The narrow band gap and long gate length provide degradation in steep SS due to the ambipolar leakage power. So, to reduce ambipolar leakage power, the TFET should design with short gate length thereby increasing the band gap. The body thickness is the important factor to reduce short channel effects in TFET. The circuit layout design for non-identical TFET source and drain will be the next demerit. Because in TFET source and drain requires the different doping levels, different doping type, and material. So, the layout designing for TFET will be harder. Finally, unidirectional conduction in TFET causes less reliability in designing technique.

3. TFET SRAM Design

3.1. Overview

SRAM is the semiconductor memory that uses bistable latches circuitry. It is a non-volatile memory unlike DRAM, which requires periodic refresh. The 6T SRAM memory cell consists of six transistors to store the data. Generally, it has three operation modes namely standby mode, read mode and write mode. In standby mode, the device is in an idle position. The word line becomes zero which means not asserted. So, bitline also turned off. Till the power supply last in the device ($N_1 - N_2$), the data will hold in the latch. In read mode, the word line is asserted. So the data in the bitline will be read [11]. The write mode helps to update the contents in the memory. The conventional 6T SRAM structure is shown below in fig 4.

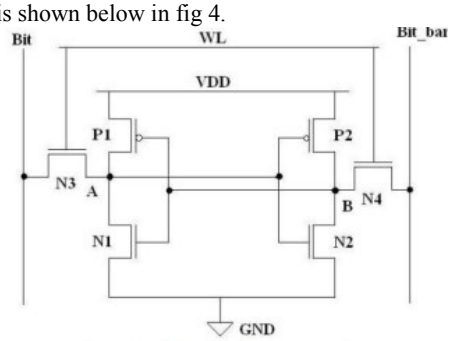


Fig.4: General 6T SRAM Architecture

3.2. Design Challenges

The main drawback of designing SRAM memory cell using TFET is the property of uni-directional behavior [12]. During the read/write operation, the current conduction in the opposite direction it will lead to non-feasible SRAM operation. To avoid that, the bitline voltage should be varied between V_{dd} and GND. So that, a part of transistors connected to the bitline will operate in reverse. But, this will leads to intense power leakage. To optimize the device, it has to allow a wide range forV_{ds}, at which current will be zero and operate at low voltage. When$V_{dd} = V_{ds}$, the leak-

age current will be less[12]. Thus we can improve the device stability, speed, and power performance.

3.3. Performance Parameters

Signal to noise margin (SNM) is the vital performance characteristic in the SRAM design. It is defined as the biggest noise voltage that can be applied to the half cells of the SRAM device and examine which set of cells withstand to that noise voltage. SNM can be periodically measured from the largest square in the butterfly curve [13]. This curve obtained from direct and an inverse voltage transfer curve (VTC) as shown in this fig 5. The next parameter is the 'write delay' and 'read delay'. Write delay defined as the time at which the data can be actually written while applying the word line voltage. Read delay is the delay between word line voltage and the response from the sensor. In other word is the time taking for discharging 10 % of the peak value.

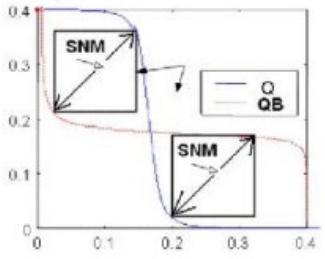


Fig.5: Calculation of Signal Noise Margin (SNM)

4. Result and Discussion

The proposed 6T SRAM memory cell has been designed using 32 nm TFET technology. The simulation result and the netlist are shown below in fig 6 and 7. The SRAM write and read operation waveforms shown in the result and the power analysis of the sane parameter discussed. The power usage of SRAM write is 3.8E-10 and for SRAM read is 1.8E-09. The delay of SRAM write is 9.9E-09 and SRAM read is 1.28E-11. From the power analysis netlist we can clearly understand that the suitable choice for low power application is TFET.

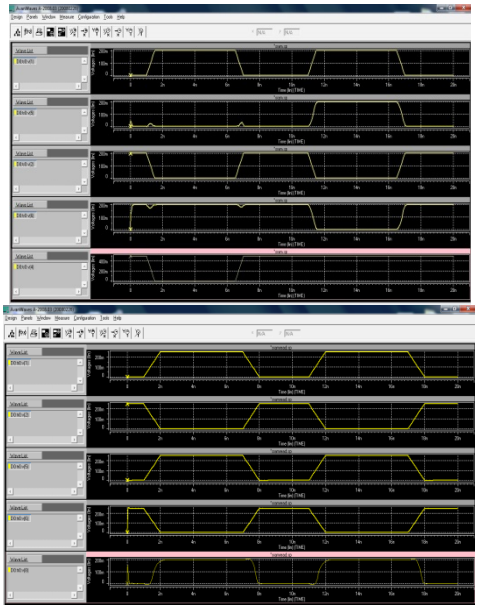


Fig. 6: Simulated Waveform of SRAM Write and Read

```
******
*sram.sp
****** transient analysis          tnom= 25.000 temp= 25.000
******
 max_pwr= 1.7894E-08   at= 6.6100E-09
        from= 0.0000E+00   to= 1.0000E-08
 tphl= 9.9508E-09 targ= 1.1263E-08  trig= 1.3125E-09
 tplh= 1.0177E-08 targ= 1.1365E-08  trig= 1.1875E-09
 tpd= 1.5039E-08

      ***** job concluded
1****** HSPICE -- A-2008.03 32-BIT (Feb 26 2008) winnt ******
******
*va.sp
****** transient analysis          tnom= 25.000 temp= 25.000
******
 max_pwr= 2.8822E-07   at= 1.1100E-09
        from= 0.0000E+00   to= 1.0000E-08
 tphl= 1.8704E-10 targ= 1.6870E-09  trig= 1.5000E-09
 tplh= 9.9780E-09 targ= 7.5220E-09  trig= 1.7500E-08
 tpd= 4.8019E-09

      ***** job concluded
1****** HSPICE -- A-2008.03 32-BIT (Feb 26 2008) winnt ******
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Fig. 7: Netlist for SRAM Write and Read

The performance of the designed cell can be evaluated by comparing the suggested design with CMOS[14], FinFET[15-18] and CNFET[19-20]. The parametric analysis can be done by leakage power, delay, and SNM. The simulation of the investigated design can be done by HSPICE and Verilog-A coding. From the result (table 1), we conclude that the design by TFET having better performance in terms of power and SNM. The lowest leakage power of 0.32 nW and has a better delay of 1.01 E-08

Table 1: Comparison table of Proposed system with the Existing technique

Parameters		TFET	CNFET	FinFET	CMOS
Channel length (nm)		32	32	32	32
Supply voltage (V)		0.25	0.5	0.7	1.8
Threshold voltage		0.05	0.1	0.12	0.53
Total power		Low	low	moderate	High
Processing speed		High	high	moderate	Low
Subthreshold slope (mV/dec)		17	28	42	60
Power dissipation (nW)		0.32	0.6	0.65	1.8
Inverter	Power	3.3 E-09	7.27 E-09	543.103E-.09	6.9E-06
	Dealy	7.0E-11	42.5 E-11	123.01 E-11	750.8 E-11
SRAM write	Power	3.8E-10	17.82 E-10	96.01 E-9	7.04E-07
	Dealy	1.01E-08	2.5 E-08	5.2 E-08	10.0E-08
SRAM read	Power	1.87E-09	0.765 E-08	1.352 E-07	1.4E-05
	Dealy	7.2E-13	7.7 E-13	8.3 E-13	9.53E-13

4. Conclusion and Future Scope

This paper presents designing of SRAM memory cell using 32 nm TFET technology. To reduce leakage power and improve SNM voltage TFET technology has been employed. It is realized from the result in the table 1, the permissible leakage power will be 0.32n W and the improved delay will be 1.01 E-08. The Hspice simulation tool is used to get the simulation results. And Verilog-A coding used to extract TFET 32 nm model parameter. This research can be extended to build a compact and low power processor by using the proposed SRAM memory architecture.

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