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Research paper



VHDL Implementation of low power turbo coded OFDM physical layer for wireless communication

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Abstract

Orthogonal Frequency Division Multiplexing (OFDM) is exceptionally favored system for rapid information transmission over remote channel. In this paper, VHDL implementation of low power turbo-coded OFDM (TCOFDM) Physical layer architecture is presented. In this architecture a low power memory-less pipelined FFT processor and Log-map turbo encoder/decoders are used to provide high throughput and lower complexity. Log-map turbo decoder provides high speed with good error correction capacity, while FFT/IFFT processor with single delay feedback (SDF) memory less architecture provide improved area and power efficiency. Proposed TCOFDM system is implemented using Xilinx ISE Design suite in the simulation results shows that the proposed scheme is having low power, high speed, high throughput and smaller area in comparison to other schemes.

Keywords: *Turbo Coding; OFDM; FFT/IFFT.*

1. Introduction

Because of quick development of remote and sight and sound correspondence, there is an enormous requirement for fast information rate transmission. To enhance the speed and greatest measure of information transmission Orthogonal Frequency Division Multiplexing (OFDM) framework have been produced. These systems likewise require quick execution of countless, which can bring about high power utilization. In this paper, we concentrate on a low power OFDM outline. [1]

OFDM system and its physical layer VHDL implementation using different modulation scheme such as Quadrature Phase Shift Keying (QPSK)[10],Quadrature Amplitude Modulation (QAM)[4], Binary Phase Shift Keying (BPSK)[1] and various channel scheme e.g. Forward error coder (FEC)and Viterbi encoding/decoding based[3,4,5] have already been developed. Recently in order to achieve high throughput of OFDM system using Turbo coding scheme [6-11] has been used. However, for turbo coding SOVA and Map [14] decoding algorithm have been developed. But, Map algorithm improved decoding speed, BER (Bit Error Rate) and system complexity. VHDL implementation of SOVA based and Log-Map based turbo coder have already been reported in [6-9]

FFT processors are the key of OFDM physical layer system. Different architecture of FFT processor has been reported for efficient OFDM. These architecture include parallel [14] and pipelined [12] implementation such as multi-path delay feedback (MDF), single-path delay feedback (SDF)[12],memory based[13] and memory less[12].In [13] an efficient 64 pipelined FFT engine has been introduced using single path delay feedback scheme. In [12] a memory less architecture with low space requirement has been presented. Since the use of turbo coder with FFT provide high throughput therefore a software (matlab) based scheme for TCOFDM physical layer has been reported in [13]

Therefore, in this paper, VHDL implementation of low power Turbo coded OFDM physical layer with efficient FFT/IFFT processor is presented. In this proposed work Turbo coder with Map algorithm and SDF based memory less FFT processor are used to improve the performance of OFDM physical layer. Pro- posed TCOFDM system is implemented using Xilinx ISE Design suite 14.2 and the simulation results compare with [5], [7] and [9]. Comparison results verify the efficiency of proposed system.

The rest of the paper is organized as follow. First, a brief re- view of OFDM system Model in section 2. Proposed Low power TCOFDM architecture details are describe in section 3. System performance, synthesis and simulation results are discussed in section 4. Finally, section 5 concludes the work.

2. OFDM system model

OFDM procedure is one of the multiple subcarrier transmission procedures. The fundamental rule of OFDM is isolate a high information rate stream into low information rate streams and transmit them in parallel [1-2].OFDM, range is isolated into sub bearers every one being regulated at bring down information rates. OFDM system is divided into three main sections: transmitter, receiver and channel. The main component of the OFDM system are encoder/ decoder[9], modulator/ demodulator, IFFT/ FFT, parallel o serial and serial to parallel convertor are shown in Fig- ure 1 .Input data is convert into time domain by IFFT in transmit- ter section and FFT convert output data into frequency domain in receiver section of OFDM system[10-11].

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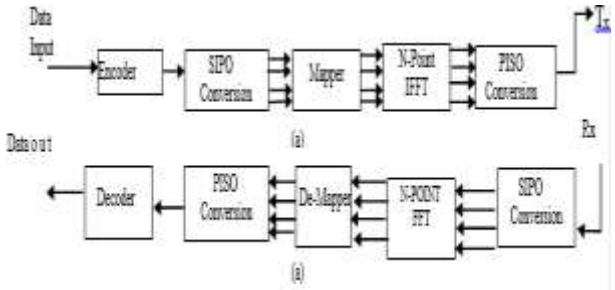


Fig. 1: OFDM Physical Layer System: A) Transmitter, B) Receiver.

In this section the Proposed TCOFDM physical layer system using max-log map algorithm [11] based turbo coder and memory-less pipelined FFT /IFFT processor is presented which is shown in Figure 2 .In transmitter and receiver turbo coding based on Map algorithm and SDF based memory less FFT/IFFT processor is
Planned by consolidating recursive systematic convolutional (RSC) encoders by parallel link strategy, which is isolated by a interleaver [15]. The conventional encoder is chosen as rate 1/3 and coefficients [111-101]. used to improve the performance of OFDM physical layer. FFT/IFFT processer is designed to fulfill the complexity and pow- er. The proposed TCOFDM system also offers multiple ad- vantages such as high speed, high throughput, low complexity and low power.
At transmitter, input data turbo encoder (rate 1/3) first encodes sequence and it produces according to rate systematic bit, parity bit0 and parity bit 1. Then, the encoded data bit is interleav- ed by a block convolution interleaver to minimize burst error probability. A Binary Pulse Shift Keying follows this
(BPSK) constellation mapping, in which interleaved [15] data is mapped to BPSK symbols. The mapped information is changed over into parallel information stream by parallel to serial convertor. The Inverse FFT changes the signs from the frequency domain to the time area. A cyclic prefix [1] of N data bit of IFFT is inserted at the beginning of the data stream, in order to avoid inter-symbol interference (ISI).

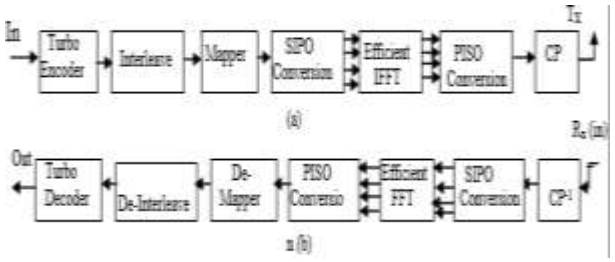


Fig. 2: Proposed Turbo Coded OFDM Physical Layer System Model.

a) Transmitter.
b) Receiver.

At receiver, received symbol streams are first goes through Inverse CP to remove cyclic prefix. Its preamble remove through CP after that it converts serial to parallel. 8 point parallel data is passed through FFT [10]. FFT transforms the data into frequency domain. Next, the information data is de-mapped and de- interleaved. System is being decoded by a turbo decoding process, which is carried out by a soft-decision turbo decoder[14].
This module employs the Max-map algorithm to determine the most likely transmitted sequence given the received sequence.
The detailed explanation of sub blocks used in proposed TCOFDM as follows:-
Turbo Encoder\ Decoder: Turbo encoders are for the most part planned by consolidating recursive systematic convolutional (RSC) encoders by parallel link strategy which is isolated by a interleaver [15]. The conventional encoder is chosen as rate 1/3 and coefficients [111-101].

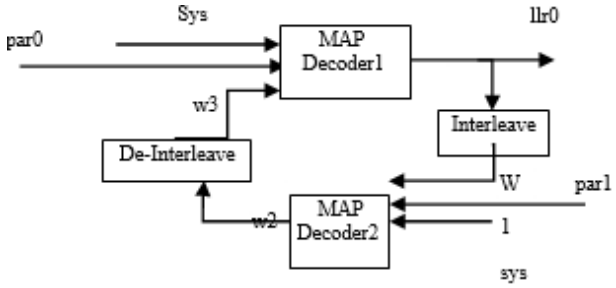


Fig. 3: Block Diagram of Turbo Decoder. Using Map Algorithm.

Turbo decoder comprises of Map decoder to decode sequence of received data bit. Each Map decoder [11] is based on Max-Log Map algorithm [16]. Map decoder1 generate llr0 (extrinsic infor- mation) using three inputs such as systematic bit (sys), parity bit 0(par0) and deinterleaved bit (w3) (starting value is zero).The out
put of Map decoder 1 is interleaved by interleaver and passes to Map decoder 2 .Map decoder 2 operates on the input bits which are input systematic bit (sys),other parity bit 1(par1) and interleav- ed bit (w2). Deinterleaver does inverse Interleaving. Deinter- leaved data (w3) of w2 passes to Map decoder 1.This process is repeated in iterative manner to decode the sequence.
FFT/IFFT Processor FFT/IFFT pipeline architecture is shown in Fig. 4. 8 bit 8 parallel input data sequences from the parallel to

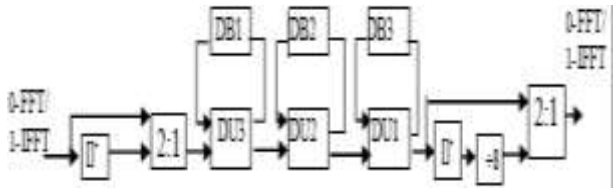


Fig. 4: 8-Point Efficient FFT/IFFT Low Power Processor.

Serial conversion block of TCOFDM system. For FFT operation, Input data is directly applied to mux (2:1) using selection line (0) and passing through a desire element unit (DU3, DU2, DU1) [12] and delay-line buffers (DB1, DB2, DB3) and received at the end of the block mux (2:1). For IFFT operation selection line of mux is [1] and some extra processing units conjugate operation ($[]^*$) is implemented using 2's complement of the imaginary part of a complex value. Moreover, the division by [8] can be substituted with a hard-wired shift manner. Details of the system has been explained in [12-14].

3. Simulation and synthesis results

Simulation of proposed TCOFDM transmitter and receiver are done in Xilinx ISE simulator ISIM 14.2. Simulation results of 80 sub carrier using rate (1/3) coding TCOFDM transmitter is shown in Figure 6 TCOFDM receiver received 80 sub carrier and gener- ate 4 bit output is shown in Figure 8. Simulation results of 8-Point FFT/IFFT processors are shown in Figure 9 and Figure 10 respectively. Turbo encoder and decoder are shown in Figure11 and Figure 12.

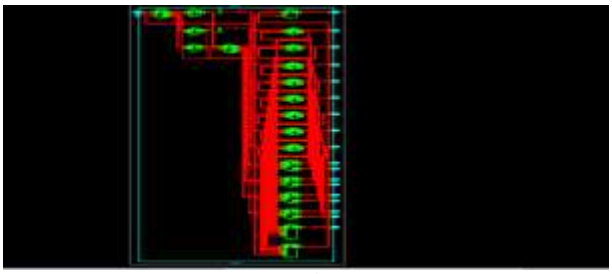


Fig. 5: Synthesis Result of TCOFDM Transmitter.

Figure 5. and 6. shows synthesis and simulation result of Turbo coded OFDM transmitter. If clock=0, reset=0 or 1, output of vari-

ous blocks of OFDM transmitter will be zero. Various blocks of OFDM transmitter produces a value only when clock is high and reset is 0. 4 bit binary input is given to Turbo encoder it produces 4 bit systematic ,parity0 and parity1 output. Input value consid- ered here is 0111.Output of IFFT is 64 bits of real and imaginary components and it is given to Cyclic Prefix block. Output of cy- clic prefix block is of 80 bits and it is given to Output module block.

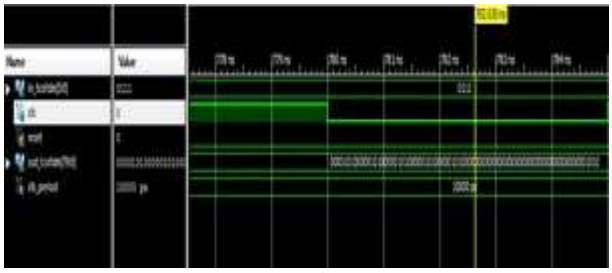


Fig. 6: Simulation Result of TCOFDM Transmitter.

Figure 7 and 8 shows synthesis and simulation result of turbo coded OFDM Receiver. If clock=0, reset=0 or 1, output of various blocks of OFDM receiver will be zero. Various blocks of TCOFDM receiver produces a value only when clock is high and reset is 0. TCOFDM Transmitter output is given to Inverse Cyclic prefix block. At Inverse Cyclic prefix block, those bits which are added at the transmitter are removed. Output of Inverse Cyclic prefix block consists of 64 bits of data. These 64 bits are given to FFT block. Then converts 64 bit data to a 12 bit data using other block . Extra 52 bits are removed at this stage. 12 bit data is given to turbo decoding block. At this block original input data is recov- ered. Input 0111 is given at transmitter and it is recovered at re- ceiver as shown in Figure 8.



Fig. 7: Synthesis Result of TCOFDM Receiver.

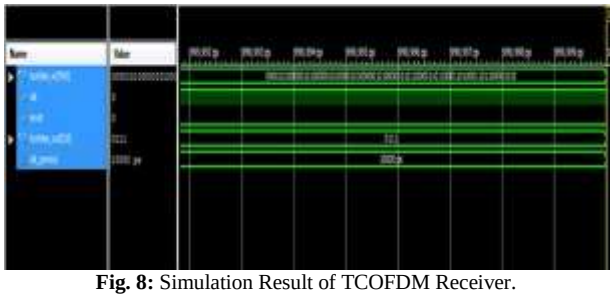


Fig. 8: Simulation Result of TCOFDM Receiver.

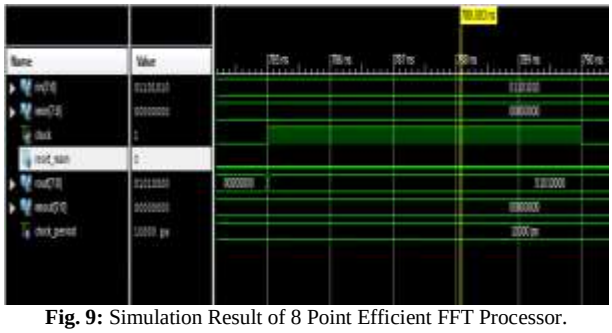


Fig. 9: Simulation Result of 8 Point Efficient FFT Processor.

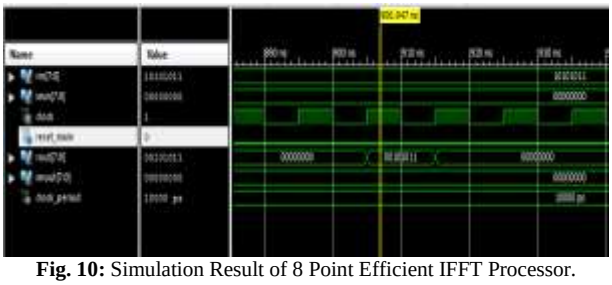


Fig. 10: Simulation Result of 8 Point Efficient IFFT Processor.

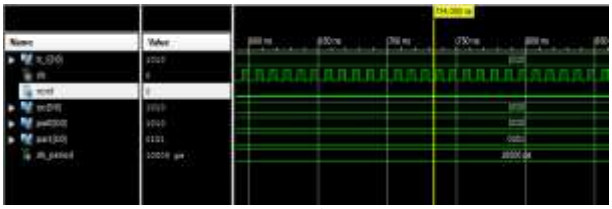


Fig. 11: Simulation Result of 1/3 Rate Turbo Encoder.

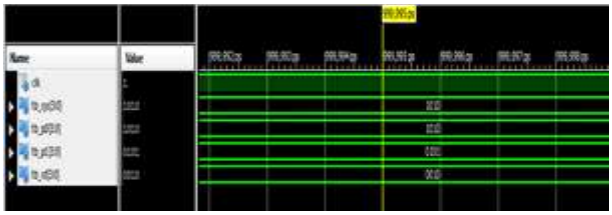


Fig. 12: Simulation Result of Turbo Decoder.

The performance evaluation of the system is given in Table I. Simulation results of the proposed system are compared with con- ventional architecture and summarized in Table.1 It is clear for the proposed design is having 4.078 delay and 1.3mW power.

4. Conclusion

In this paper, VHDL implementation of low power and high data TCOFDM system model is presented. Area efficient and high speed 8 point radix-2 FFT low power processor and turbo decoder are design to investigate. The simulation results shows that pro- posed TCOFDM architecture is high speed and consumes low area. Proposed design is suitable to be used in wireless communication.

Table 1:

Design	Specification		
	Hardware Number of LUTs	Time Delay	Power
[5]	-	-	2.4 mW
[7]	-	-	3.43 mW
[9]	-	100 µs	-
Proposed	1353	4.078 ns	1.3 mW

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