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Research paper

High Gain Multistage Power Amplifier for Internet of Things (IoT) Applications.

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Abstract

This paper presents the design of a linear power amplifier (PA) with high gain and low power consumption for Internet of Things (IOT) application. The gain of the PA is boosted with driver stage integration. The effect of C_{gs} capacitance is mitigated by utilizing a passive linearizer, which improves the efficiency and linearity of the PA while delivering gain of 19dB from 2.4GHz to 2.5GHz. The designed PA exhibits gain of 19.6dB with PAE of 29.71% at maximum output power of 15.9dBm. The corresponding OIP3 is 21dBm at drain voltage of 18.V. The designed multistage PA with passive linearizer acts as a method to improve linearity and gain of the 180nm CMOS power amplifier without trading-off the efficiency and maximum output power at the operating frequency.

Keywords: *CMOS; power amplifier; multi stage; Internet of Thing (IoT).*

1. Introduction

IoT has been tremendously developing from convergence of wireless communication systems. IoT has the ability to transfer data over network without requiring human-to-human or human-to-computer interactions. The development of wireless communication systems enhanced the industrial turnover in recent years. The IoT is a communication network of Internet enabled objects, together with web services that interact with these objects. The critical technologies of the IoT are smart sensors, RFID, smart phones, and intelligent wireless transmission. The IoT is the most demanding technology trend after the Internet. It is necessary to design an efficient and high-gain wireless transmitter with a low cost power amplifier in order to satisfy the multi-standard demands.

Usually, power amplifiers for battery operated IoT devices should be highly efficient and linear across wide range of power levels to ensure precise and efficient interchange of data between the RF transmitter and receiver. The stringent requirement of linear signal transmission in modern wireless communication system challenges the realization of CMOS PA implementation as compared to Gallium Arsenide (GaAs) PAs [1] – [4]. Maximum power transfer can be achieved by using impedance matching between the input and the driver stage as well as between the main stage and output. The designed PA should provide good reverse isolation between the input signal and the output signal. Since PA is a part of the transceiver, a design of low power consumption, small chip area, acceptable gain, PAE, and return losses is preferred [5].

However, CMOS PAs facing various obstacles in commercialization due to the intrinsic disadvantages of standard CMOS processes. The disadvantages include high substrate losses, low quality factor, low transconductance, and low breakdown voltage of active devices. Lot of exertions is directed to the development of high power generation techniques as well as on linearity and efficiency enhancement techniques, so that the drawbacks of CMOS technology PAs can be overcome [6]. To realize highly efficient power amplifier in CMOS process, the limitation in terms of process technology has to be comprehended [7]. Therefore, continuous efforts are being carried out by researchers to enhance the efficiency, linearity and output power, as well as the operating frequency of the PA in order to realize single-chip CMOS integrated circuit [8]-[9].

In this work, a high gain, low power consumption linear PA for IoT application is designed. The content of this research paper is as follows. Section 2 present the design methodology of this work. Section 3 delineates the post layout results of this CMOS PA. Finally, the conclusion is presented in Section 4.

2. Power Amplifier Design Methodology

In this design, the linearity of the PA was enhanced by employing a linearity improvement circuit to the gate of the main PA which is known as the passive linearizer. Main PA consumes quiescent current of 15mA when biased at Class AB. The driver stage, on the other hand, produces additional gain in which improves the overall gain of the designed PA.

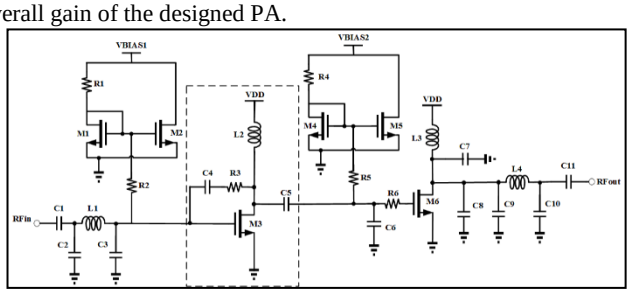

Fig. 1: The schematic design of proposed high gain multistage amplifier.

The passive linearizer consists of R_6 and C_6. The C_{gs} cancellation is shown in equation (2) while equation (1) represents transistor's

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input impedance with relation to Cgs before the implementation of passive linearization at location Z in Figure 1.

2.1. Equations

Before llinearization the multistage power amplifier defines as below,

$$Z = R_g - j\omega C_{gs} \tag{1}$$

After linearization,

$$Z = \frac{\omega[R^2_6 + \omega^2 C_6][\omega R_6(1+C_6)]}{[\omega R_6(1+C_6)]^2 - [R^2_6 - \omega^2 C_6]^2} + j\frac{\omega[R^2_6 + \omega^2 C_6][R^2_6 - \omega^2 C_6]}{[\omega R_6(1+C_6)]^2 - [R^2_6 - \omega^2 C_6]^2} \tag{2}$$

C_1, C_2, L_1 and C_3 delineate the input impedance transformation network. On the other hand, the output impedance transformation network is denoted by C_9, L_4, C_{10} and C_{11}. Inductor L_3 and C_7 will minimize the effect of parasitic drain-source capacitance, C_{ds}, which improves efficiency of the dual-stage PA. C_8 is the decoupling capacitor. The IMD3 (third order non-linear) component that rises due to the DC source is shunted to ground by this capacitor. This mitigates the effect of the non-linear components from DC supply with the multistage PA. The phase response before and after linearization is shown in Figure 2.

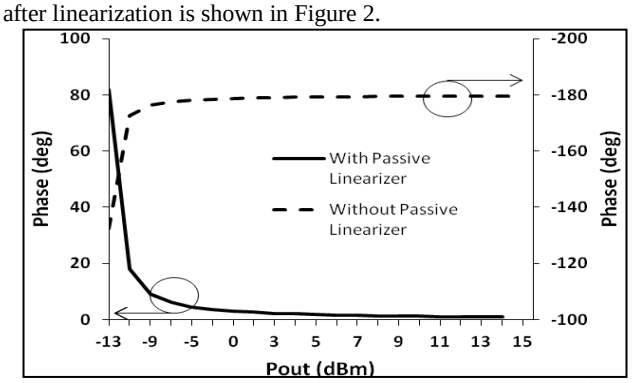


Fig. 2: The Phase response of high gain CMOS power amplifier.

As shown in equation (2), the passive linearizer provides a positive opposite phase response which reduces the side lobe generation [10]. Equation (3) represents efficiency of the PA in terms of PAE in relation with the gain and power consumption.

$$PAE = \frac{G}{P_{DC}} * 100\% \tag{3}$$

3. Validation Results

Figure 3 shows the s-parameters of the PA. The gain provided is 19.6dB at 2.45GHz, with corresponding S_{11} of -13.9dB and S_{22} of -8.5dB.

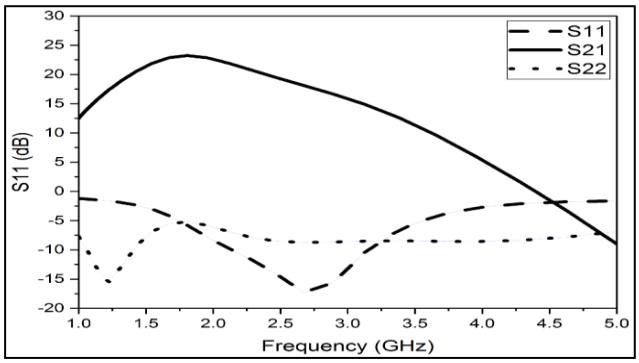


Fig. 3: The S-Parameter for designed multi-stage power amplifier.

Figure 4 depicts the stability factor, Kf of the PA. The stability factor is more than one up to 5GHz which shows it is unconditionally stable.

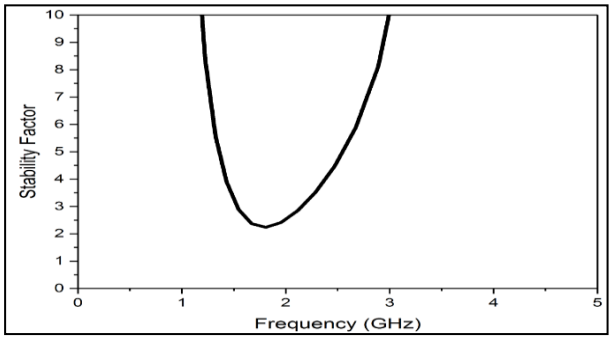
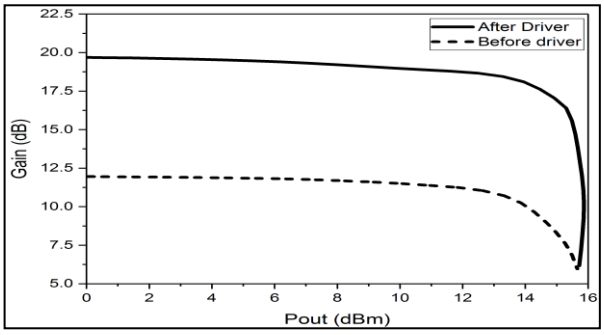


Fig. 4: The stability factor of multistage PA,which is more 1 up to 5GHz.

The power gain plot before and after driver stage implementation is depicted in Figure 5. The passive linearizer generates a flat gain response while the driver stage improves the gain by more than 8dB. The maximum output power achieved is 15.9dBm. The 1dB



compressed output power (P_{1dB}) of 10.7dBm is produced by the designed PA.

Fig. 5: Power gain plot before and after driver stage implementation.

Figure 6 shows the power added efficiency (PAE), power gain, and OIP3 of the multistage PA. The third order intercept point (OIP3) is utilized as the parameter to measure the linearity. The peak PAE achieved is 29.71% obtained at 2.45GHz with corresponding OIP3 of 21dBm, tested with two tone signal with crude 1MHz spacing.

Table 1: Post Layout Simulation Results High Gain Multistage PA.

	The synoptic of the PA performance	
		Parameter
1.	Operating Frequency	2.5Ghz
2.	Bandwidth	100Mhz
3.	Power Gain, S21	19.6 dB
4.	Input Return Loss, S11	-13.6 dB
5.	Output Return Loss, S22	-8.5dB
6.	Peak PAE	29.71%

7.	Maximum Output Power	15.9 dBm
8.	OIP3	21 dBm
9.	Power Supply Voltage	1.8V
10.	Technology	CMOS 180nm

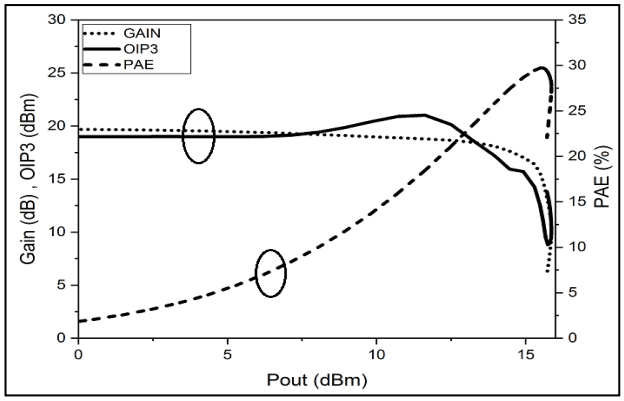


Fig. 6: The PAE, power gain, and OIP3 performance of the multistage PA.

4. Conclusion

In this paper, a driver stage is utilized to enhance the gain of the PA and a passive linearizer is used to improve the linearity of the PA. The PA is designed in 180nm CMOS process. This multistage PA achieved maximum PAE of 29.71% as well as output power of 15.9dBm. OIP3 of 21dBm was produced. Hence, the designed high gain and linear multistage PA can be utilized for low power IoT applications.

References

[1] A. Shehhi, Badreyya, and M. Sanduleanu. "An 800uW Peak Power Consumption, 24GHz (K-Band), Super-Regenerative Receiver with 200p J/bit Energy Efficiency, for IoT." 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), 2016

[2] X. Sun, F. Huang, X. Tang and M. Shao, "A 0.7–6GHz broadband CMOS power amplifier for multi-band applications," 2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Shenzhen, 2012, pp. 1-4.

[3] X. Yu, S. P. Sah, H. Rashtian, S. Mirabbasi, P. P. Pande and D. Heo, "A 1.2-pJ/bit 16-Gb/s 60-GHz OOK Transmitter in 65-nm CMOS for Wireless Network-On-Chip," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 10, pp. 2357-2369, Oct. 2014.

[4] IEEE 194 RF - 1 - © 1994-99 D. B. Leeson “Microwave Amplifiers”

[5] B. Koo, Y. Na and S. Hong, "Integrated Bias Circuits of RF CMOS Cascode Power Amplifier for Linearity Enhancement," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 2, pp. 340-351, Feb. 2012.

[6] S. Jin, B. Park, K. Moon, M. Kwon and B. Kim, "Linearization of CMOS Cascode Power Amplifiers Through Adaptive Bias Control," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 12, pp. 4534-4543, Dec. 2013. Fauci AS, Braunwald E, Kasper DL & Hauser SL (2008), Principles of Harrison’s Internal Medicine, Vol. 9, 17thedn. *McGraw-Hill*, New York, NY, pp.2275–2304.

[7] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 1974-1987, Sept. 2015.

[8] K. Oishi et al., "A 1.95 GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier Using Timing Alignment Technique for WCDMA and LTE," in IEEE Journal of Solid-State Circuits, vol. 49, no. 12, pp. 2915-2924, Dec. 2014.

[9] G. Indumathi and S. Keerthana, "Design of cascode topology based CMOS power amplifier for wireless applications," 2014 IEEE International Conference on Computational Intelligence and Computing Research, Coimbatore, 2014, pp. 1-4.

[10] G. Jeong, B. Koo, T. Joo and S. Hong, "Linearization of RF CMOS power amplifiers," 2015 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Sendai, 2015, pp. 154-156.