International Journal of Engineering & Technology, 7 (4.39) (2018) 393-395

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper



A Novel Approach to Design a BCD Adder Using Complimentary Logic Gate

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Abstract

A complimentary Logic gate is most broadly research area look into existence from couple of decades. It has numerous applications in different technologies, for example: - Nano figuring, Bio sub-atomic calculations, Spacecraft, Quantum PCs, DNA registering, Field programmable Gate Array (FPGAs) in CMOS technology. The fundamental reason for planning BCD adder by utilizing complimentary gates is to diminish quantum cost and the quantity of waste outputs. The fundamental motivation behind the paper is to portray the correlation in Quantum cost, undesired output in the middle of BCD Adder using complimentary logic gates.

Keywords: *Complimentary logic, Garbage outputs, Quantum cost, BCD adder, Complimentary gate.*

1. Introduction

In the present condition the power consumption because of data misfortune is a main problem, so to eliminate this problem complimentary logic gates are utilized in logic gate implementation. Here BCD adder can implemented using complimentary logic gates to eliminate the power dissipation problem because of loss of information or loss of data. The power dissipation is directly depend on loss of information or loss of data. According to Landauer's [1] hypothesis, one bit data losses have power dissipation of KT*ln(2) joules, where K is represented as Boltzmann constant and T is represented as total temperature. In the present planning computers play out a logic task for eradicating data bits and this logic activity is known as complimentary logic and this system is having more power dissipation.

For reducing the power dissipation an elective technique is utilized which is known as complimentary logic. It is the method which speaking to balanced mapping in the middle of the input and output vectors. In 1973 C. H. Bannett [2] power dissipation that it is conceivable to maintain a strategic distance from KT*ln (2) joules of power dissipation by actualizing complimentary circuits. In 1973 he define and demonstrated that if the complimentary model calculation is done then the power dissemination can be zero in any gadget. He demonstrated it by utilizing turing machine and this machine is calculation representative model.

Gordon.E.Moore [3] in 1965 predicted that on the single chip the parts numbers will twofold in each multi month. This forecast is legitimate today because of development in the integrated circuit's technology. This forecast is known as the Moore's law, so it demonstrates that the quantity of segments on the chip
builds the power dissipation. Henceforth the power dissipation is main target for the present engineers.

In the year 1994 Shor[4] made a complimentary calculation for extensive number factorization with better proficiency in contrast with the established processing hypothesis. Edward Fredkin and Tommaso toffoli [5, 6] presented Fredkin and Toffoli complimentary gates on the idea of reversibility. These gates are utilized as widespread gates with zero dissipation.

This paper composed in different areas:- Section1 define the introduction of complimentary logic and the design issues, Section 2 provides the important complimentary logic gates with their logic diagrams and logic functions. section 3 discussed the design issues in complimentary BCD adder with the proposed BCD adder using the complimentary logic gates, section 4 provides the result in which the comparison between the proposed design and the literature survey are discussed, and section 5 concludes the research paper and provide the future scope at the present work.

2. Complimentary Logic Gates

To implementation of BCD adder using complimentary logic gates, some basic complimentary gates will be-

2.1 Feynmann Gate:-

In Feynmann gate [7], the sources of info are meant as input vectors (X,Y) and the outputs are indicated as output vector (P,Q) as appeared in the figure.1.In this gate, input bit (X) goes about as control signal. So if X=0 at that point input Y is trailed by the output Q. on the off chance that X=1 then the output Q flip the input Y. It is otherwise called controlled NOT (I-NOT) or Quantum XOR. Feymann gate works in as replicating gate by duplicate the principal contribution at output when second input is zero.

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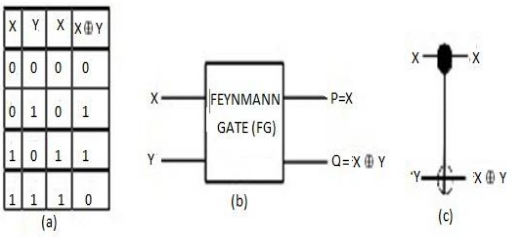


Fig 1: Feymann gate.

2.2 TSG Gate

It is (4,4) complimentary gate and it is utilized for separately working in as complimentary full adder, so a single gate can execute the complimentary full adder. TSG gate [8] accomplishes the significant worry about limiting the quantity of complimentary gates and trash output by which TSG gate is low power complimentary circuit with high speed.

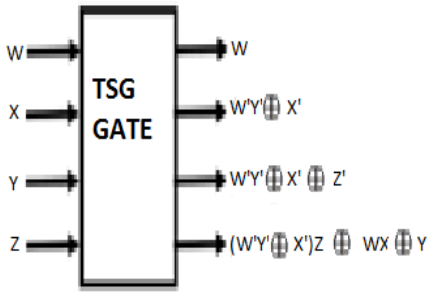


Fig 2: TSG gates.

2.3 New Gate:-

The New gate[9] is a universal gate which is used to implement the basic operation.

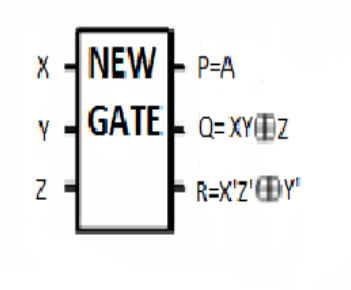


Fig 3: New gate.

3. Proposed Circuit

This section represent the conventional BCD adder and Carry select BCD adder with their complimentary implementation.

3.1 Conventional BCD Adder:-

The ordinary BCD adder includes two BCD digits in parallel and gives a total digit at output which is likewise in BCD. The adjustment logic ought to likewise incorporate into the interior development of BCD adder. The best four bit binary adder included two decimal digits with input carry to give the output of binary sum. The binary sum is included nothing when the output carry (Cout) is equivalent to zero. At the point when the output carry (Cout) is equivalent to one at that point base binary adder added binary 0110 to the binary sum. The base binary adder output carry (Cout) is overlooked and the output carry terminal is as of now has its supply data. The graph of traditional BCD adder is appeared in figure.4.

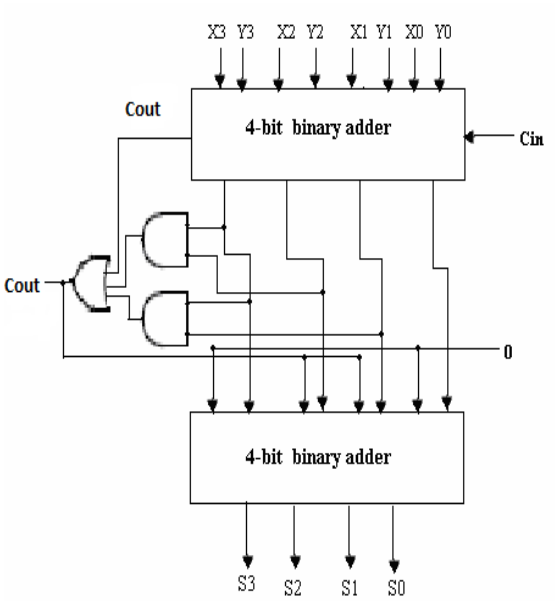


Fig 4: Conventional BCD adder.

Complimentary logic representation of Conventional BCD adder:
The Complimentary execution of the regular BCD adder is appeared in the figure.5.here TSG gates are utilized to upgrade the BCD adder. The BCD adder utilizing the TSG gate as far as number of complimentary gates and trash output delivered is greatly improved than the engineering of ordinary BCD adder in [10].
The proposed BCD adder has just 11 complimentary gate and gives just 22 rubbish output and the BCD adder engineering [10] has 23 complimentary gates and gives 22 trash outputs.

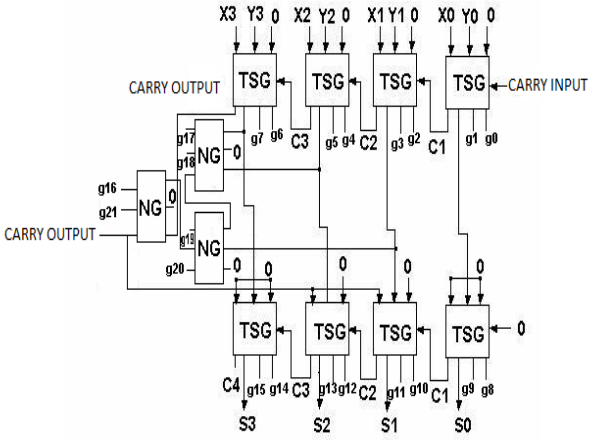


Fig.5: Complimentary implementation of conventional BCD adder

3.2 Carry Select Adder:-

The carry select plan has the quicker handling of result as opposed to the carry skip plot. The carry select plan gives the decrease in deferral by choosing pre-figuring total and carry output contingent upon the info carry. The figure define the carry select plan. The essential issue looked in accelerating carry propagation in the carry select plan is the quick handling recently carry input. The last entirety and carry has the accompanying conditions

$$Si = Ck.S0i + Ck.S1i \quad (1)$$

$$Ci+1 = Ck.C0i+1 + Ck.C1i+1 \quad (2)$$

So the carry select addition requires two full adders for Clk=0 and Clk=1 and two 2:1 multiplexer for every sum bit and carry out selection.

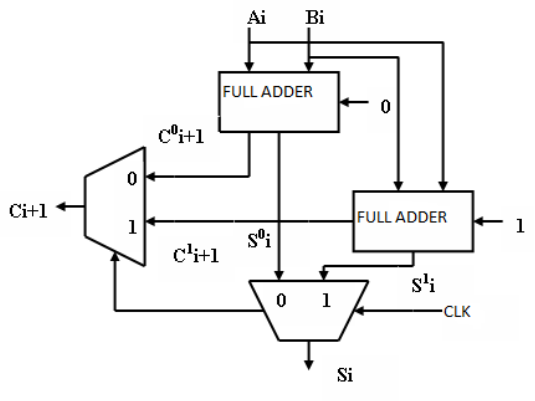


Fig.6: Carry select BCD adder

Complimentary Logic implementation of carry-select BCD adder:- In the complimentary carry select BCD adder five complimentary gates are utilized to frame a block. Here two TSG gates are utilized to goes about as full adder to register whole and carry for the two potential outcomes in input carry. One input bit is given to the Feynmann gate to copy it in light of the fact that the fan-out isn't permitted in complimentary logic. Here Fredkin gates are utilized in the place of two multiplexer to choose the proper aggregate and carry which is relying on the input carry. In the complimentary carry select BCD adder, four blockss are structured and the BCD activity is performed by utilizing the complimentary gates i.e. TSG and New gates. The quantity of complimentary gates in complimentary carry select BCD adder is twenty seven and the waste output is thirty-nine.

4. Result

Comparative Study of the Complimentary BCD adder:-

Table 1

S.No.	Circuits Name	Number of compli-mentary gates used	Number of Garbage produced
1.	Complimentary BCD Adder[10]	23	22
2.	Proposed convention-al BCD adder using complimentary logic	11	22
3.	Proposed carry select BCD adder using complimentary logic	27	39

In carry select BCD adder, it provides the pre-computed sum and its carry depends upon in input carry. This circuit provides the delay 476.223 nanosecond. The speed up path of that circuit is from input carry to output carry and from input carry to Si.

5. Conclusion and Future Scope

In the present planning, the PCs squander a lot of power and stor-age capacity limit these circuits depend on ircomplimentary logic gadgets which waste millions of bits and billions of times each second. The best way to restrain the power wastage is complimen-tary figuring. This paper proposed novel plans of regular BCD adder and Carry select BCD adders. These models are intended for appropriate execution of complimentary logic blend. This paper gives a base to assemble complex framework, for example, the BCD ALU of crude quantum CPU.

Reference

[1] R. Landauer,"Irreversibility and heat generation in the computational process",IBM Journal of research and development,5,pp.183- 191,1961.
[2] Bannett C.H.,"Logical reversibility of computation",IBM J. research and development, pp.525-532,1973.
[3] Gordon.E.Moore,"Cramming more components onto integrated circuit electronics, Volume 38, Number 8, April 19,1965.
[4] P.Shor," Algorithm for quantum computation:discrete log and factoring", Proc. 35th Annual symp. On found of computer science (1994),IEEE computer society, Los Alamitos,124-34.
[5] E.Fredkin, T.Toffoli,"Conservative logic", International journal of Theor,physics, 21(1982),pp.219-253.
[6] T.Toffoli,"Complimentary computing",Tech memo MIT/LCS/TM-151,MIT Lab for computer science(1980).
[7] Feynmann R.,1985."Quantum mechanical computers",optics news,11:11-20.
[8] Himanshu Thapliyal and M.B. Srinivas,"A novel complimentary TSG gate and its application for designing complimentary carry look ahead and other adder architecture ",accepted in Tenth asia pecific computer architecture conference,singapore,october24-26,2005.
[9] Azad khan Md. M.H. 2002: "Design of full adder with complimentary gate ",International conference on computer and information technology, Dhaka,Bangladesh,pp.515-519.
[10] Hafiz Md. Hasan Babu and Ahsan raja chowdhury,"Design of a complimentary binary coded decimal adder by using complimentary 4-bit parallel adder",VLSI Design 2005,pp.255-260,Kolkata,India,Jan 2005.