International Journal of Engineering & Technology, 7 (4.36) (2018) 306-310

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design of Arm Processor's Elements Using QCA

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Abstract

Quantum dot Cellular Automata is one of the promising future nano-technology for transistor-less computing which takes advantage of the coulomb force interacting between electrons. The aim of this paper is to consider the logical circuits of ARM processors and further reducing their size in nanometres like 2:1 multiplexer , D Flip Flop, scan Flip Flop, 2:1 multiplexer with enable, encoder, decoder, SR FF, shift register, memory cell and program counter are designed using QCAD tool . Their cell count, area, kink energy are taken in consideration to calculate power and energy dissipation.

Keywords-*QCA Quantum Dot Cellular Automata, Complementry Metal Oxide Semiconductor*

1. Introduction

Quantum- dot cellular automata (QCA) is emerging as a potential nano-scale computing technology that may provide an alternate to the current CMOS Technology [1]. In QCA, binary information is stored in quadratic cells. Each cell is having square nanostructure consisting of four quantum dots and can possess a single electron per dot. Every cell is charged with two electrons and two polarizations are possible by columbic repulsion. The QCA cells are used for computation, storage and communication purpose. A number of consecutive QCA cells connected in series can act like a wire that can propagate the signal [2]. There are four clock phases to control the signal flow and cells are refreshed on every cycle[3]. The transistor based conventional computing circuit consume high power due to leakage currents in comparison to QCA cells. In contrast, Quantum dot Cellular Automata for electronic circuits is provides the advantages of high density, low power consumption and fast speed compared to current computing technology.

2. Arm processor

ARM is known for Advanced RISC Machine which belongs to the reduced instruction set computing architectures for computer processors. These processors can be configured for various environments. Processors having RISC architecture require fewer transistors than those with a complex instruction set computing architecture, which in turn improves the cost, power consumption and energy dissipation. Figure 1 shows the Architecture of ARM processor.

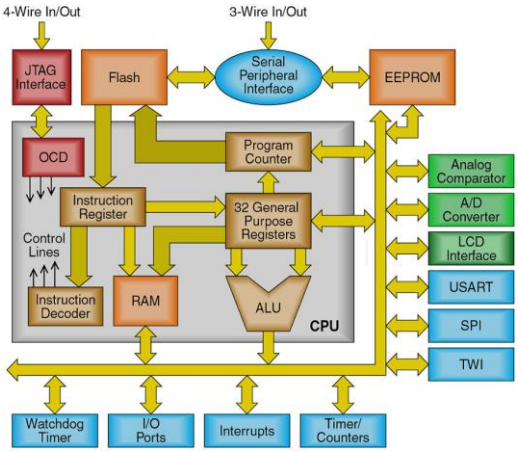

Figure 1: Architecture of ARM processor

It is a very high speed, more efficient processor. It is a 32-bit multi-core processor and it is also of very small size circuit integrated into a tiny chip. The size, operating time and factors related to power and energy can be reduced by designing it using QCAD tool. In this paper some of the peripheral elements in this ARM architecture are designed which are Multiplexer, few flip flops, scan flip flop, encoder, memory, decoder, instruction register and counter parts.

3. Qca designs of arm7 elements

(1) 2:1 & 4:1 Multiplexers- The multiplexer can be designed using 3 majority voter gates as shown in figure 2 [4]. Figure 3 represents the circuit design of 2:1 multiplexer and Figure 4 shows the circuit design of 4:1 Multiplexer using QCA.

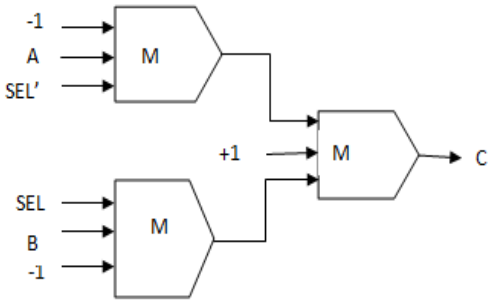

Figure 2: Majority gate implementation 4:1Mux

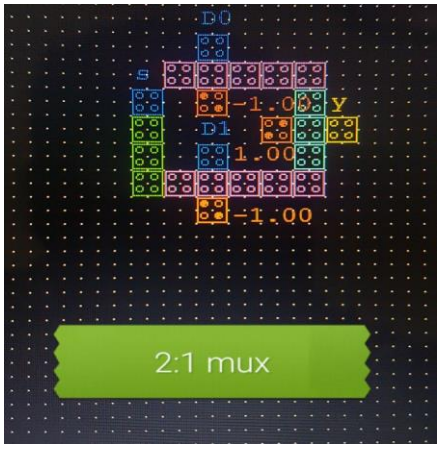

Figure 3: 2:1Mux QCA layout

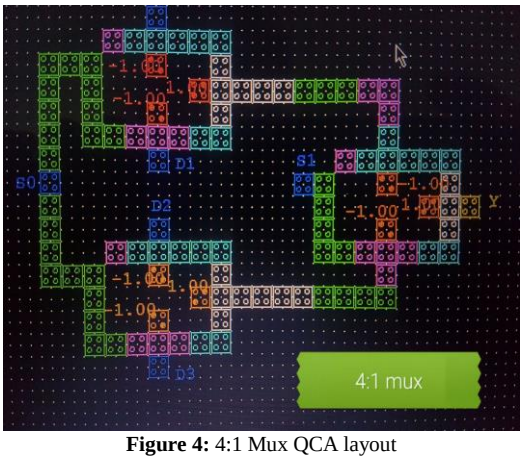

Figure 4: 4:1 Mux QCA layout

The following equation fits for 2:1 multiplexer,
Y = MV [{MV (A, SEL',-1)}, {MV (B, SEL,-1)}, 1]
2) 2:1 Multiplexer with enable – The multiplexer to select one input from two inputs by just one selection line as on figure 5 [5]. The circuit has five majority gates as shown in figure 6. We can use a enable pin to activate or deactivate the multiplexer, when it is low the multiplexer is selected and when the enable pin is one the outputs of all the multiplexer is zero Irrespective of the value on selection line.

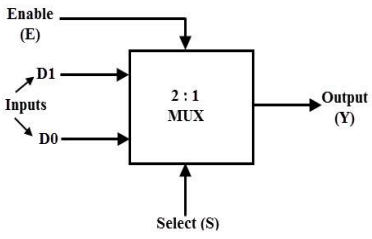

Figure 5: 2:1 Mux with enable logic

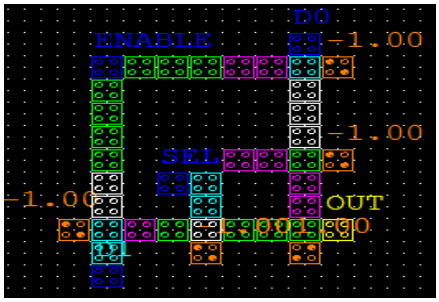

Figure 6: 2:1 Mux with enable QCA layout

(3) D Flip Flop – The D- FF puts the value of the D input at the rising edge of the clock, which comes at the output. At others times the output does not change. The D-FF used as a memory cell to store data. D flip flop is named as delay flip flop because input data appears at the edge of the clock. In the quantum dot circuit of D flip flop shown in figure 7, six majority voter gates are taken with six NOT gates. This is the circuit of positive edge triggered D-flip flop [6][7].

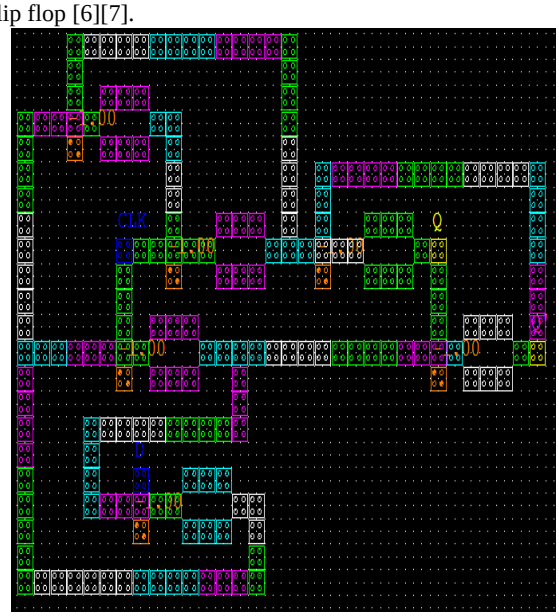

Figure 7: D Flip Flop QCA layout

(4) Priority Encoder- It is a circuit to compress many binary inputs and to convert into less number of outputs. The output of this priority encoder comes as binary of the original number starting from zero of the most significant input bit. Ten switch system is very common device in most digital systems for numerals ranging from 0 to 9. The switches go to 1 or 0 logic-levels to function as Off/On. A number is fed to the circuit in BCD code and the switch according to number matrix is marked. More number of inputs if made high at any instant of time, input which has more priority is obtained.

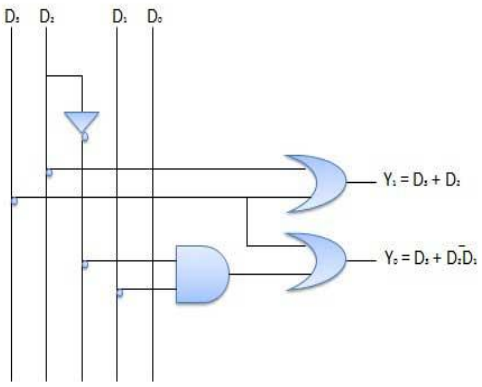

Figure 8: Priority encoder circuit

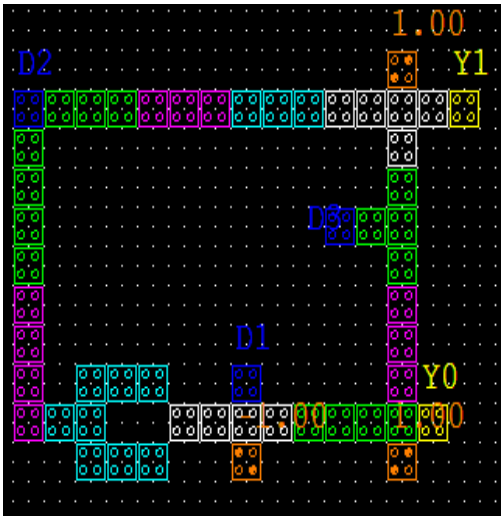

Figure 9: Priority encoder QCA layout

The gate level circuit of priority encoder shown in figure 8 is designed using quantum dot as shown in figure 9. The circuit implementation requires three majority voters and one NOT gate.

(5) Scan Flip Flop -Scan flip-flops can be distributed among any number of shift registers, each having a separate scan in and scan out pins. Test sequence length is determined by the longest scan shift register. Just one test control (TC) pin is essential. Scan chain testing is a method to detect faults on the silicon chip. This circuit is a common method to be implemented in circuits for testing purpose. Testing becomes very simple by setting and observing all the FFs in an IC. Scan FF's basic circuit consisting of D, SE and SI signals to control and observe the scan technique . The scan flip flop is shown in figure 10 and the quantum implementation of the scan logic is shown in figure 11.

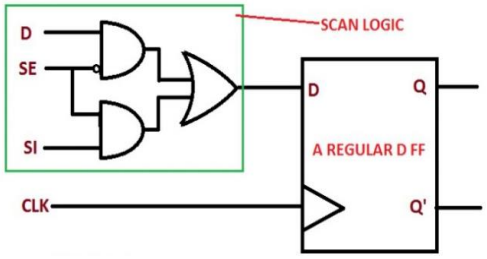

Figure 10: Scan Flip Flop logic

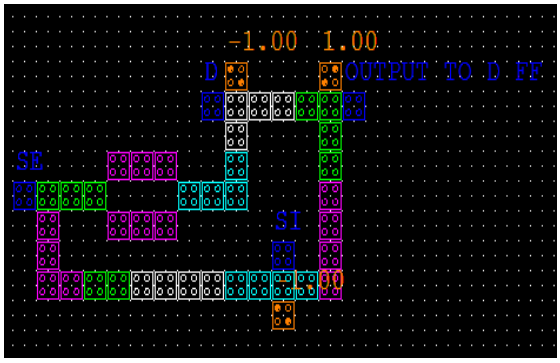

Figure 11: Scan FF QCA layout

(6) SR Flip Flop- SR- FF using NAND gate are mostly used, because it is a universal one. So it can be made to mimic any of other standard logic function, cheaper to construct. The SR latch with NAND gates is implemented on quantum dot as described in figure 12. The operation of the basic SR latch can be modified by adding control clk- input that determines when the state of the latch can be changed as in figure.

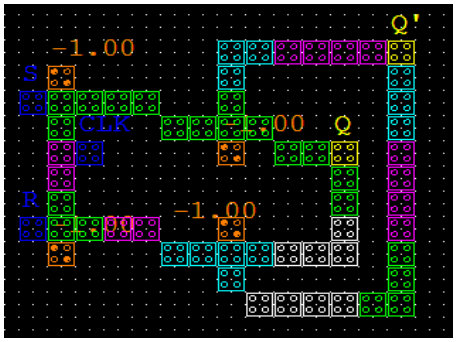

Figure 12: SR latch QCA layout

(7) Four bit Shift Register - The register shifts its binary information in one or both directions. Clock pulse is common to all FF's. In the figure 13 the shift register is implemented using D flip flop which are connected in cascade, The diagram shows implementation of two D FF's in cascading which is to be repeated to design a four bit shift register.

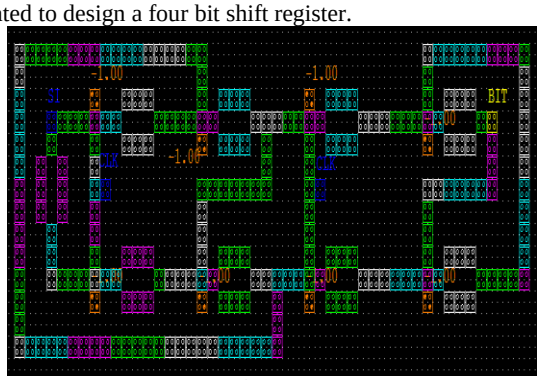

Figure 13: Shift register QCA layout

(8) Program Counter - Counters are sequential circuits that cycle through some states which can be implemented using flip flops. There are two categories of counters synchronous and asynchronous. Single bit shift is there from one flip-flop to next one for generating unique timing signals. If we feed the initial value of register with 1000, then pattern repeating will be one bit shifted to the right: 1000, 0100, 0010, 0001, 1000…. Figure 14 shows the QCA implementation of Program counter.

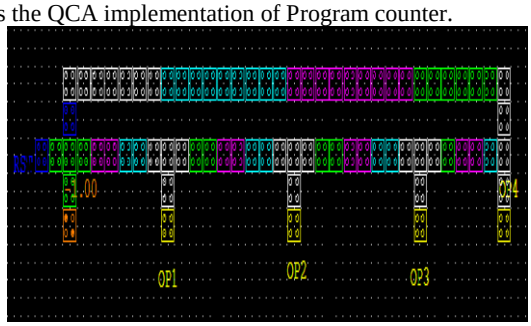

Figure 14: Program Counter QCA layout

Table 1

Sr. No.	Design	Number of cells	Area	Kink Energy
1	2:1 Mux	23	19044.00 nm^2	41.65 x10^{-29} J
2	4:1 Mux	103	132924.00 nm^2	186.53x10^{-29} J
3	2:1 Mux with enable	40	48832.00 nm^2	72.444x10^{-29} J
4	D Flip Flop	200	283824.00 nm^2	362.20 x10^{-29} J
5	Priority Encoder	53	75460.00 nm^2	95.98 x10^{-29} J
6	Scan Flip Flop	46	88560.00 nm^2	83.31 x10^{-29} J
7	SR Flip Flop	61	70560.00 nm^2	110.47x10^{-29} J
8	4 Bit Shift Register	246	266324.00 nm^2	445.51 x10^{-29} J
9	Program Counter	76	64484.00 nm^2	137.64 x10^{-29} J

4.Simulation Results

All the circuit simulations using QCA are obtained by using bi-stable approximations and results of 2:1 multiplexer, Multiplexer with enable, D Flip Flop, Priority encoder, Scan Flip Flop, SR Flip Flop and Counter are shown in figures 15, 16, 17, 18, 19, 20 and 21 respectively and these results are verified by truth tables. Also the Area in nanometers of circuit implementation and Kink energy [8]-[10] is calculated and listed in Table1.

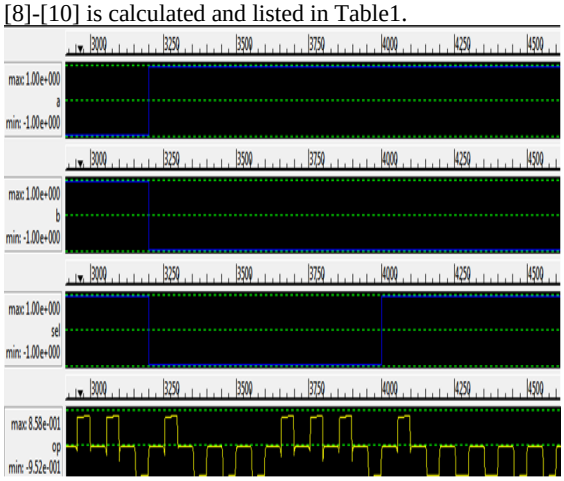

Figure 15 Simulation result of 2:1 Multiplexer

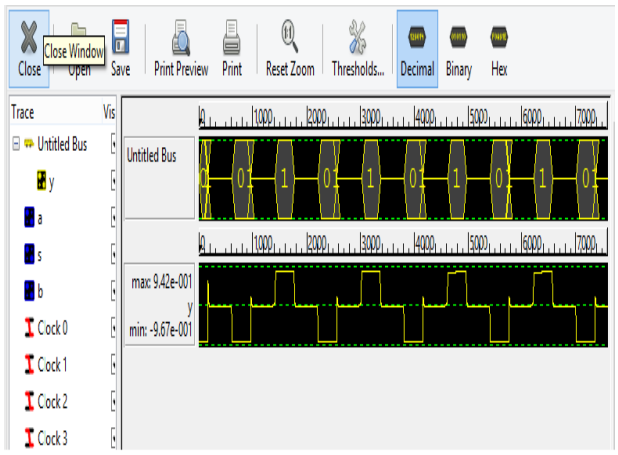

Figure 16 Simulation result of Mux with enable

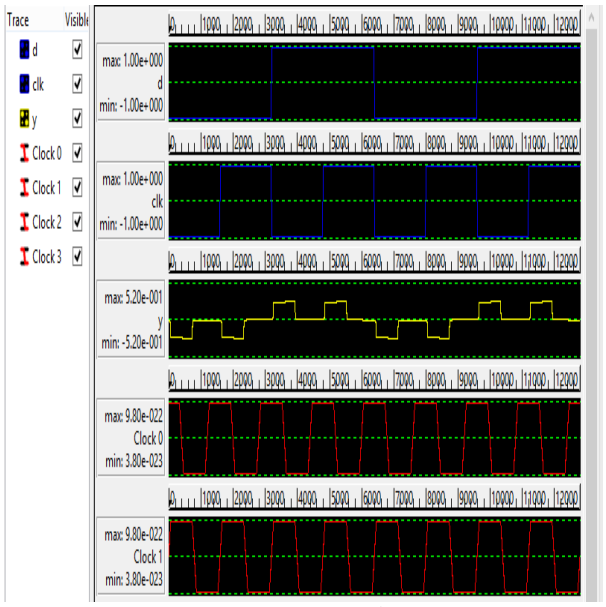

Figure 17 Simulation result of D Flip Flop

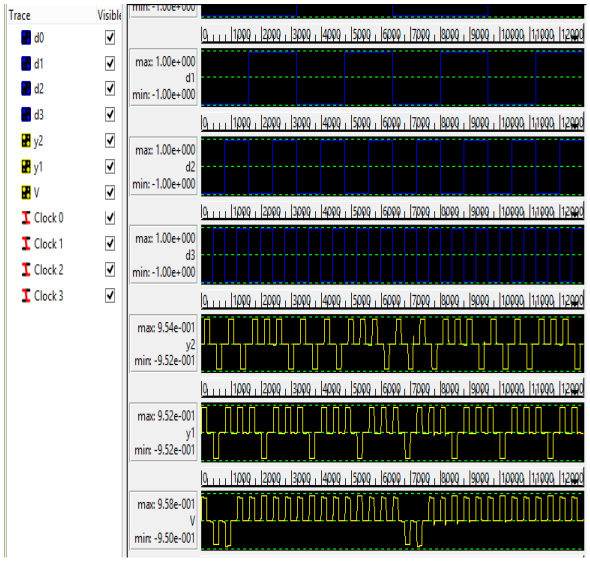

Figure 18 Simulation result of Priority Encoder

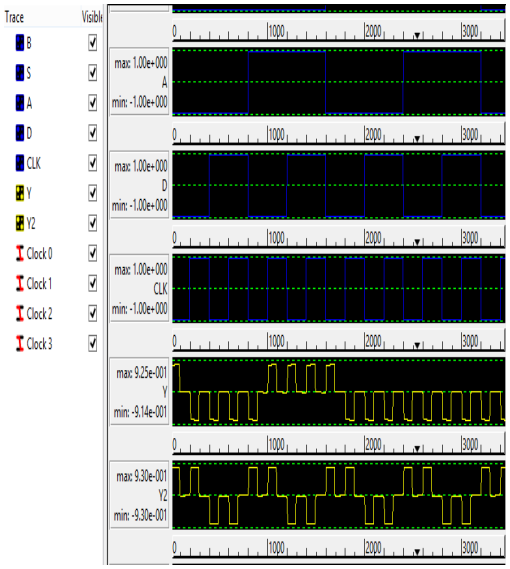

Figure 19 Simulation result of Scan Flip Flop

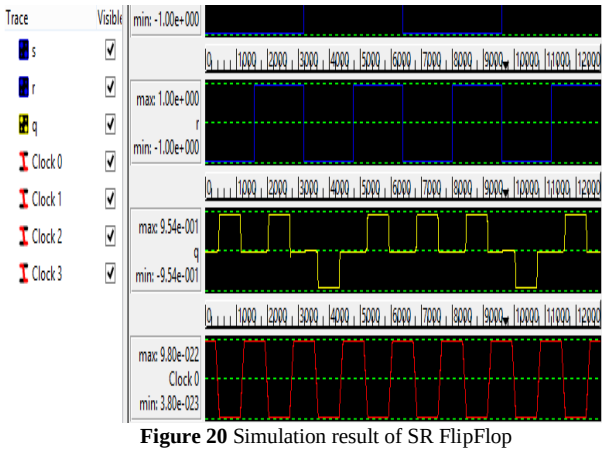

Figure 20 Simulation result of SR FlipFlop

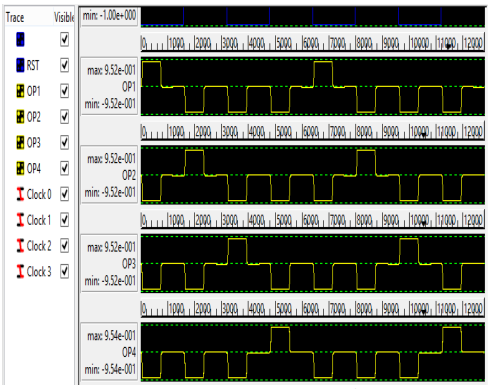

Figure 21 Simulation result of Counter

5. Conclusion

The conventional QCA is an upcoming trending nanotechnology. Using this nanotechnology some peripheral elements of our ARM processor are designed. After generating the QCA layouts their cell count, area used, delay obtained, their efficiency, power and energy dissipation and the number of clocking provided are derived by Hamilton matrix equation and Kink energy exhibits energy in the form of 10^{-29} Joules. It can be observed that some of the elements are more optimised when compared with previous design.Thus the result obtained in comparison with cadence is , the area usage is optimised by 30%.

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