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Research paper



A novel design of low-power reversible carry selects adder employing MPFA

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Abstract

In VLSI technology, power dissipation is of major concern next to speed. Due to development in technology, the necessity of fast an efficient high performance processing units has become inevitable. The circuitry of Carry Select Adder (CSLA) promises rapid dispensation in ALU and furthermore optimization can be accomplished. The proposed work encompasses the makeup of reversible design of Carry Select Adder using Modified Peres Full Adder (MPFA) and Fredkin Gate (FG). It is observed that the proposed CSLA is area efficient and attained 70% low power dissipation. The reversible CSLA is synthesized in Xilinx environment and simulated by means of ISE simulator. The reversible CSLA proposed showed multi fold advantages in terms of area- power – delay.

Keywords:*CSLA, Fredkin Gate (FG); MPFA; Garbage Outputs; and Delay*

1. Introduction

The major concerns for designing circuits, owing to the fast emerging mobile engineering are not merely faster units but also that of being area efficient and low power. Fast Adders are significant mechanism of many processing circuits including DSP (Digital Signal Processing) and ALU's (Arithmetic Logic Unit) chips [20, 25]. In the midst of a range of adders, the carry-select adder (CSLA) is intermediary concerning area and speed extensively used in mobile industry [2]. Carry Select adders with exceptionally great sizes can be designed hierarchically by merging minor 'block' adders [1]. Fig. 3 depicts the traditional (CSLA) Carry Select Adder by means of two ripple carry adders in each block , one for the input carry Cin = 1 and the further one with Cin =0 except in block 1. As an alternative of using two Ripple Carry Adders, Chang et.al anticipated a 29% decreased area Carry select adder by replacing one of the ripple carry adder to an add-one circuit with almost 6% speed penalty [3]. A bundle of work has been made to diminish larger area of Carry select adder with negligible speed trade-off and small area [4-8]. This paper propose an area efficient design of carry select adder employing reversible gates with smaller delay.

There are a range of adders, Ripple carry adder (RCA) is one of the proficient adder which is simple to analyse and devise but sluggish in processing. In order to attain greatly more speed, carry look a-head adder is worthwhile but main disadvantage of this is that it consumes additional area [11]. As a result of keeping these two most important shortcomings, Carry select adder is suitable however it is necessary to optimize in definite characteristic since in CSLA more over delay or area can be optimized,nevertheless not both owing to employment of multiple RCA pairs to produce carry and partial sum by taking into account Cin= 0 in one stage and Cin= 1 in other stage. Absolute results can be achieved by making use of multiplexers. In view of this point, the proposed work used single stage reversible carry select adder with reversible gates that eradicate the use of ripple carry adder, where area is diminished and in addition the power dissipation is also reduced.

The proposed flow of Reversible Carry select adder using MPFA elucidated in this manuscript is sorted into five segments. Segment 1 elaborates the importance and reversible logic gates .Segment 2, converse about reversible logic gates, Segment 3 give details of conventional CSLA design. Segment 4 describes the proposed CSLA using MPFA reversible gate, Segment 5, shows the simulation results of proposed work along with transistor implementation and the power comparison and Segment 6 conclusion.

2. Reversible logic gates

An n-input and output logic gate with one-to-one mapping is a reversible circuit. This helps to choose the outputs from the inputs and in addition the inputs can be inimitably traced back from the outputs. Moreover in the synthesis of reversible logic direct an-out is not permissible since one–to-many model is not reversible. A reversible logic circuit must be designed with least number of gates and following are the parameters that determine complexity and performance of circuits [8 - 10].

The Parameters are as follows:

i) Constant inputs (CI): In order to synthesize the particular logical function, the Constant Inputs refers to the number of inputs that are to be retained constant at either 0 or 1.

ii) Garbage outputs (GO): The number of unused outputs in a reversible gate is Garbage Output. One cannot get rid of garbage outputs as these are very necessary to attain reversibility.

iii) Quantum cost (QC): The cost of a primitive gate used in the reversible circuit is inferred as Quantum Cost. The number of primitive reversible logic gates is identified by calculating (1*1 or 2*2) essential to implement the circuit.

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iv) Gate levels (GL): The number of levels in the logic circuit which are vital to realize the specified logic functions is referred to as Gate Levels [16].

2.1. Fredkin gate

Fig.1be evidence for a 3 * 3 Fredkin gate. This is a fundamental concept in reversible and quantum computing. Fredkin gate is inverse and it is its converse. The input has three variables I(A,B,C) , the output has three variables O(P,Q,R) and the output is defined by P = A, Q = A'B+AC and R=AB+A'C. It is also called as CSWAP (Controlled Swap gate) and is universal. Like universal NAND and NOR gate, any gate can be realized using Fredkin gates alone. In this proposed work, Fredkin gate act as a 2x1 multiplexer.

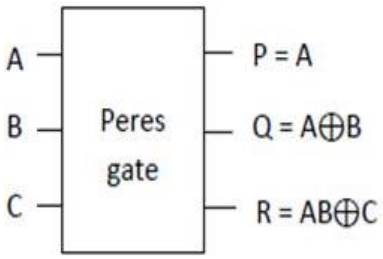


Fig. 1: Reversible 3x3 Fredkin Gate.

2.2. Peres gate

Fig.2 shows a 3-input and 3-output Peres gate [9]. The input vector has three variablesI (A, B, C) and the output vector has three variables O (P, Q, R). The outputs are defined by P = A, Q = A⊕B and R=A.B⊕C. The Quantum cost of a Peres gate is known to be 4; because of its lowest quantum cost, the Peres gate is usedin the realization of the proposed design.

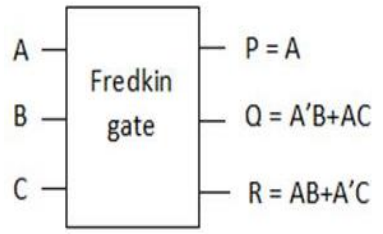


Fig. 2: Reversible3x3 Peres Gate.

2.3. MPFA

A full-adder realized using two Peres gates is as shown in Fig.7.

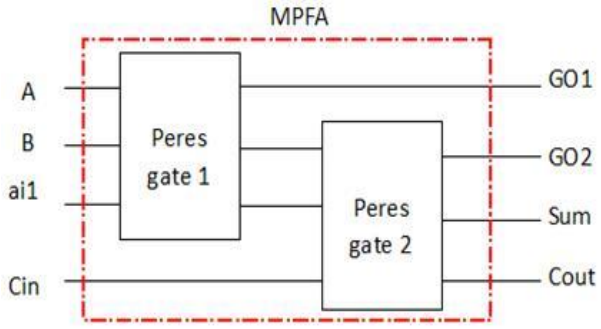


Fig. 3: Reversible 4x4 MPFA Gate.

The quantum cost of this MPFA is 8, since two Peres gates are used. The MPFA reversible gate can act as a Full adder with one Ancilla input ai1 and two garbage outputs GO1 and GO2. The full adder using MPFA is obtained with C=0 and D= Cin and its quantum cost is calculated to be equal to 6.

3. Conventional CSLA

In implementing any digital system using reversible circuit, the number of gates, the Ancilla inputs, quantum cost and garbage outputs are the key parameters for analyzing any reversible circuit as defined in [21]. In this paper the above parameters are analyzed and tabulated in section VI for proposed circuit. As per the conventional Carry Select adder architecture [15], it clearly implies that due to the existence of Ripple carry adder in each and every stage, it absorb more area and also take considerable amount of time to process, since the carry from each stage as to propagate from one stage to another stage where it takes a little time to propagate. By keeping this as main point in mind [12, 13, 14] RCA's in the conventional circuit is replaced by reversible full adders i.e MPFA to realize lower area and a smaller amount power dissipation by dipping number of gates.

The Fig.4 elucidates conventional 4 – bit carry select adder. In the work proposed by Ming-Cui Li &Ri-Gui Zhou, a four-bit reversible Ripple adder optimizing low latency has been developed with three reversible gates TEPG (triple extension of Peres gate) ,RMUX21 (reversible 2-to-1 multiplexer) and NPG (new Peres gate) are anticipated and used to devise adder counterparts[21]. The design concentrates only on the quantitative analysis based on the reversible gates used.V. Shiva Prasad Nayak et.al [24] anticipated the a reversible carry select adder using D-latch, the study shows the increase in area and ecessity of a enable signal making the design more complex.

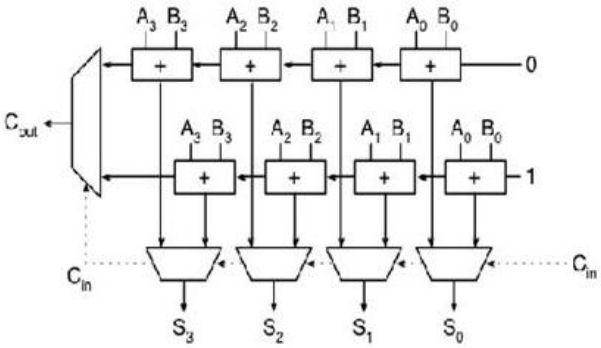


Fig. 4: Conventional 4-Bit CSLA.

4. Proposed CSLA

In order to replace the N bit Ripple carry adder, at first single stage carry select adder is designed as illustrated in Fig.5. The proposed 1-bit CSLA is designed using two MPFA gates and two Fredkin gates. The input carry Cin to the one of the reversible full adder (MPFA) is 1 and 0 to the otheri.e the output sumand carry is computed with both the conditions (Cin = 0 &Cin=1) from MPFA1 and MPFA2. The Fredkin gate acts as a 2x1 mux with select input as Cin. When Cin is equal to 0, sum S1 and carry C1 are selected as adder's SUM and COUT outputs respectively.

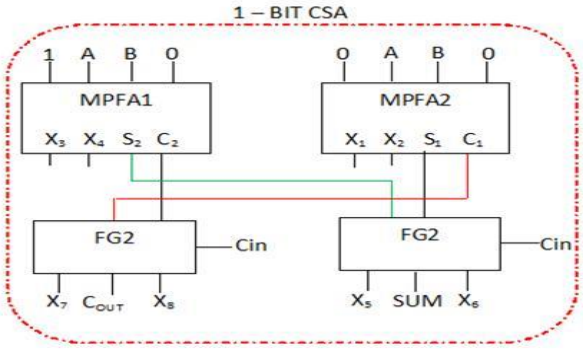


Fig. 5: Modified CSLA with MPFA.

When Cin is equal to 1, sum S2 and carry C2 are selected as adder's SUM and COUT outputs respectively. i.e just the once all the intervening sums and carries are premeditated, the absolute sums are calculated by means of multiplexers having nominal delay. Exploit of the vital unit through the 2-to-1 multiplexer therefore achieves quick incrementing deed with abridged gate count. Consequently, the proposed CSLA outclass the usual CSLA,in terms of power and speed by tumbling the propagation latency of carry.

5. Transistor implementation

Reversible logic computing [16], [17] is an important area to explore which is characterized as a result of having only deterministic computational models. The power dissipation caused by the loss of information is an inspiration for using these deterministic models. In the respite of this segment will spotlight on how reversible gates can be implemented in CMOS. At first, the basics of transistor implementation using CMOS is briefed and then the implementation of the reversible gates used in this design is elaborated briefly. A pass transistor logic is one where either an pMOS or a nMOS transistor is employed unaccompanied as a switch, but none of them act as faultless switches. A nMOS transistor isideal (or strong) for fleeting a false low-voltage signal between its source (i/p) and drain (o/p), but very poor (or weak) for fleeting a true high-voltage signal. On the other hand, pMOS transistor, passes a weak low-voltage and a strong high-voltage.

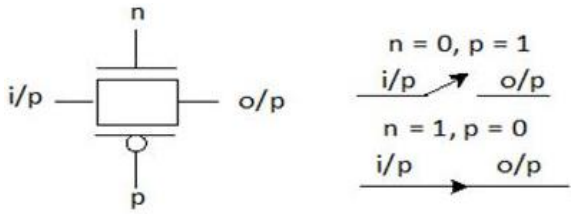


Fig. 6: CMOS Pass Transistor logic.

To overcome the drawback of using nMOS and pMOS transistors separately,both transistors can be usedanalogous to each other to create a logic so as to pass both a strong high-voltage and a strong low-voltage signal as elucidated in Fig.6. This logic of using both nMOS and pMOS transistors in parallel is known as pass transmissiongate.

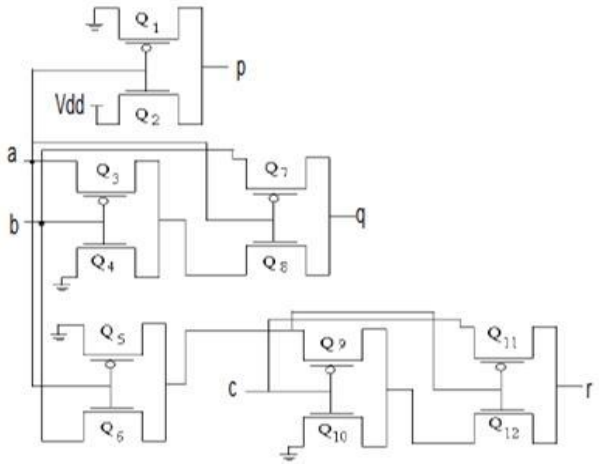


Fig. 7:CMOS Pass Transistor Implementation of Peres Gate.

The nMOS and pMOS transistors can be used autonomously, however while implementing circuits by means of pass transistors there are two signals; one is n-control and other one is p-control which is the complement of n-control. Therefore there are two complementary lines for all the signals and therefore the name CPL(Complementary Pass Transistor Logic) or DPL (Dual-line Pass-transistor Logic).

The pass transistor realization of Peres gate is as illustrated in the Fig 7. Assuming the inputs to be a=1, b=0, c=0, the transistor Q2, Q4 are OFF and Q1, Q3 are ON. Hence the input "a" is passed on to pi.e p=1; now the second output Q = a xor b, therefore q=1; finally the third output r is reliant on all the three inputs a, b and c. In this case the transistors Q5,Q10 and Q12 are OFF and Q6, Q9 and Q11 are ON making the output r=0.

The Fig.8 represents pass transistor implementation of Fredkin gate which act as a 2 X 1 Multiplexer, the q and r swap between the inputs b and c if input a is 0 or 1. Assuming that a=1,b=0 and c=1, the supply voltage Vdd is passed on to output p making p=1.so that the transistors Q2,Q4 and Q6 are ON. The input c is routed through Q4 and input b is routed through Q6 forcing the output q=1 and r=0. The pass transistor implementation of 1bit carry select adder is as elucidated in Fig.9.

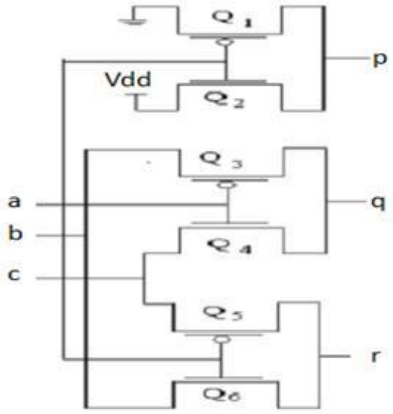


Fig. 8:CMOS Pass Transistor Implementation of Fredkin Gate.

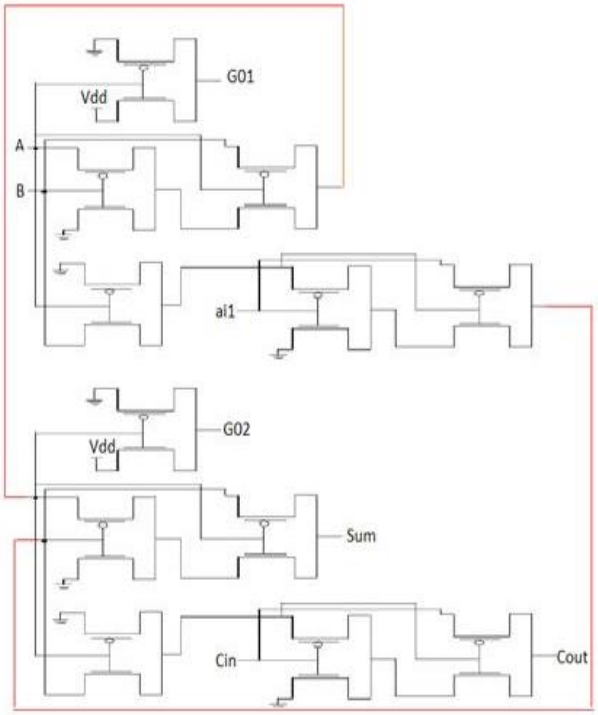


Fig. 9:CMOS Pass Transistor Implementation of MPFA Gate.

6. Synthesis and verification

The complete Design is modeled in Pure Verilog HDL. The syntax of the RTL design is synthesis and simulated using Xilinx tool for functional verification of the design. The design is verified both at a block level and top level Design. Test cases for the block level are generated in Verilog HDL by both direct and random way. The complete design along with all timing constraints, area utilization and optimization options are described using synthesis

report. The adder design is synthesized at Spartan-3 (XC3S200-5ft256), 90nm process technology.

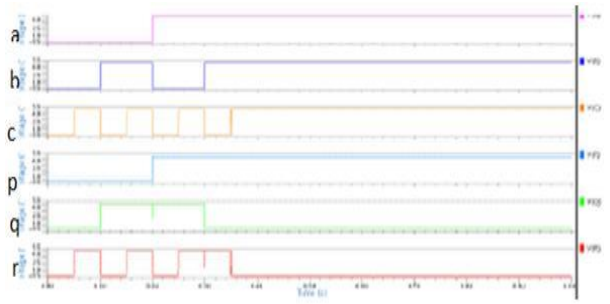


Fig. 10: Peres Gate Simulation Output.

The simulation result of Peres gate figured out in fig 10 with inputs a=1, b=0, c =0 produces an output of p=1, q=0 and r=1.

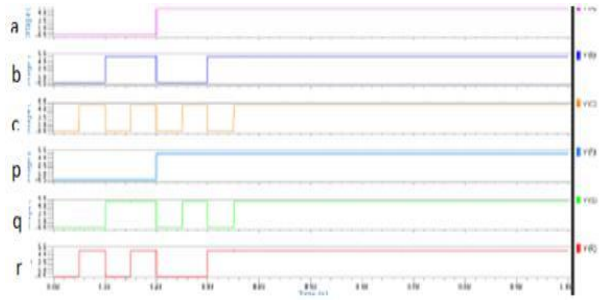


Fig. 11: Fredkin Gate Simulation Output.

The above simulation output in fig 11 represents the Fredkin gate output with a= 0, b=1 and c=1 produces an output ofp=0,q=1 and r=1.

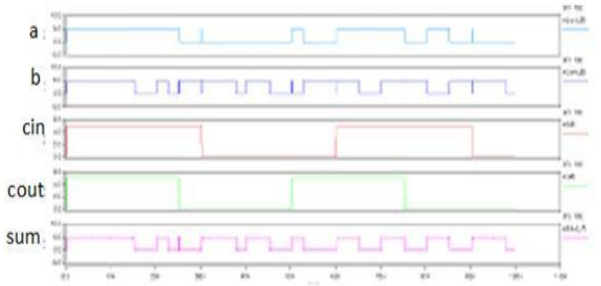


Fig. 12: Simulation Output of 1-bit CSA.

The proposed 1 bit Carry Select Adder designed using MPFA gate and Fredkin gate when simulated produced an output of Sum =1 and carry = 0 , when the inputs are a=1, b=1 and c=0 as shown in fig 12.

The area utilization summary in terms of number of transistors and power comparison of the existing 4-bit CSA [18] and proposed CSA is briefly shown in Table 1. The number of Ancilla inputs and number of garbage outputs are compared for the conventional and proposed carry select adder are tabulated for CMOS and pass transistor logic family in Table 2. The area synthesis report shows that with the Modified CSA with MPFA has lesser area as compared with CSA. The graphical representation of the area utilization is shown in Fig. 13. It can be observed that in proposed CSA the number of transistors and power dissipation are lesser than that of existing CSA.

Table 1: Power Comparison

Reversible circuit	Logic family	No/-of Transistors	Power dissipation
4-bit CSA [18]	CMOS	391	360.16mW
4-bit CSA [18]	Pass Transistor	162	118.56mW
Proposed 4-bit CSA	CMOS	256	21.7mW
Proposed 4-bit CSA	Pass Transistor	144	1.66mW

Table 2: Comparison of Reversible Carry Select Adders Based on AncillaInputs and Garbage Outputs

Circuit Design	No/-of Reversible gates	No/-of Ancilla Inputs	No/-of garbage outputs
4-bit CSA [20]	4 FG +8TSG + 8F = 20	20	24
4-bit CSA [19]	8FG + 8FTFA = 16	16	40
Proposed 4-bit CSA	8FG + 8MPFA= 16	8	36

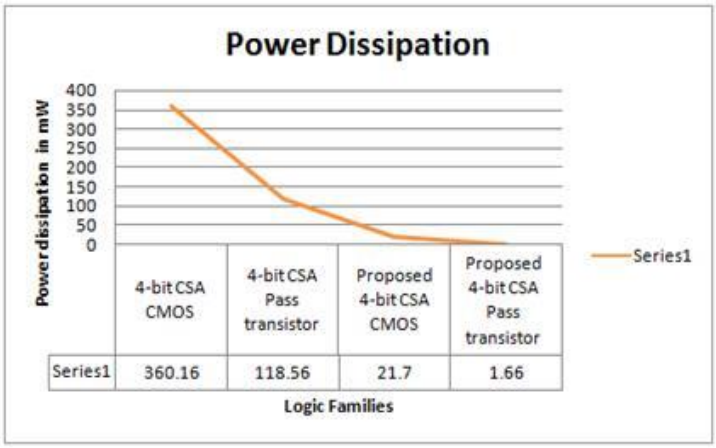


Fig. 13: Power Comparison Chart.

7. Conclusion

In this work, a four – bit carry-select adder with new reversible gate i.e MPFA has been proposed to reduce the number of transistor count, Ancilla inputs, garbage outputs and power dissipation with improved speed. The reversible Carry Select Adder is designed in both transistor level with pass transistor logic and CMOS logic and evaluated their parameters. When realized in CMOS logic the number of transistors used is reduced by 35.5% and the propagation delay by 93% for 4 inputs in contrast with the existing CSA [18]. Moreover, when realized in pass transistor logic the number of transistors used is reduced by 11.11% and the delay by 98.6% for n = 4 as compared with the existing CSA [18]. Compared to existing CSA [18], the proposed reversible carry select adder is implemented with fewer number of transistors with extremely no reduction in speed. The Pass transistor logic proves optimization in number of transistors and the delay compared with the CMOS logic. The pass transistor logic provides appreciable outputs only for few higher values of L/W ratio. The use of transmission gate logic can overcome the above problem.

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