International Journal of Engineering & Technology, 7 (4.15) (2018) 301-303

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Serially Concatenated Low-density Parity Check Codes as Compatible Pairs

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Abstract

Low-density parity checks (LDPC) codes are considered good performance error correction codes. However, decoder complexity increases with increasing code length. In this study, we introduce short-length serially concatenated LDPC codes. The proposed technique uses pairs of compatible LDPC codes that act as outer and inner serially concatenated codes. In this code pair, the inner code takes input that is the same length as the outer LDPC encoder output. This study examined two cases of LDPC codes as compatible pairs with low numbers of iterations and compared bit error rate (BER) performance to a standalone LDPC code with an additive white Gaussian noise channel. We also considered the quadrature phase shift keying QPSK, 16-quadrature amplitude modulation (QAM), and 64-QAM system modulation schemes. Simulation results demonstrate that the proposed system has good BER performance compared to a standalone LDPC code, the results summarized in table and performance curves.

Keywords: *AWGN, LDPC; 16-QAM, 64-QAM, QPSK;serially concatenated code*

1. Introduction

Low-density parity check (LDPC) codes are a class of codes first introduced by Gallager in 1962 [1]. These codes were later rediscovered by MacKay and Neal in 1996[1]. This class of codes has near-ideal performance BER that close to Shannon's limit. These codes are linear block codes that construct a sparse binary matrix H distinguished by relatively few "1s" spread among many "0s." The LDPC decoder includes an iterative decoding algorithm; however, this algorithm was beyond the capabilities of electronic processors available in 1962 [1]. Thus, these codes were not considered until 1996. Even the attempt done by Tanner in 1981 to apply LDPC as error correcting codes [2].

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The first construction of a sparse binary matrix H for LDPC codes included a fixed number of 1s per row and per column, and this is referred to as a regular LDPC code. However, the number of 1s per row and column can be varied to construct an irregular LDPC code. Generally, the bit error rate (BER) performance of irregular LDPC codes is better than that of regular LDPC codes [1]. Note that there are several methods for constructing irregular LDPC codes [3].

2. Serially concatenated LDPC codes

LDPC codes in a communication system act as error correction codes. Serially concatenation of LDPC codes has been described in the literature [4]. In that study, the communication system included a single LDPC code concatenated with a differential modulation scheme, and they concentrated on the design of effective LDPC for differential modulation. Another approach employs serial concatenation between Reed–Solomon codes as an outer encoder and an LDPC code as an inner encoder [5]. The serial concatenation of two LDPC codes has been proposed previously [6]. That system is shown in Fig. 1 [6].



Fig. 1: Serially concatenated LDPC codes.

The search [6] focuses on the use of identical short-length codes Cb (10,000, 7071) where Cb stands to LDPC code of (N, K) where N output code word length and K input data length, reduce encoding complexity, and the search includes 100 decoding iterations for each LDPC decoder process on the receiver side. And compare the serially concatenated LDPC code system performance with long length LDPC code of (14000, 7000). The simulation results show significant reduction in performance and that a single family of serially concatenated (10,000, 7071) codes to reduce encoding and decoding complexity leads to a dramatic reduction of system performance [6]. The search explains two aspects of the poor performance of serially concatenated LDPC codes. The first is decoding each stage individually and passing information from one encoder to another. The second point is that the search uses regular LDPC codes; however, we can expect improved system performance with irregular LDPC codes.
To overcome this poor system performance [6], another system model has been proposed [7] (Fig. 2).

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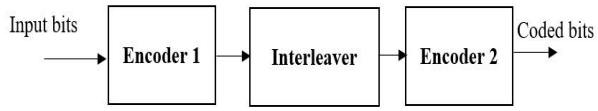


Fig. 2: Encoding scheme proposed in [7].

In Fig. 2, both Encoder 1 and Encoder 2 are of the same type, i.e., Cb (576, 384), and they use a random interleaver. Here, using the random interleaver improves system performance relative to burst errors effect reduction. The receiver side of the system is shown in Fig. 3 [7].

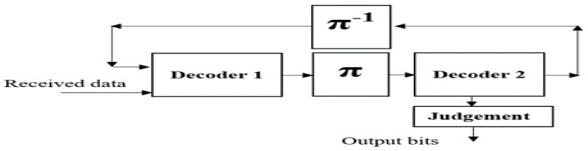


Fig. 3: Decoder scheme [7].

The system receiver uses a feedback process to improve performance. This process includes extra iterations, i.e., the number of iterations for decoding in the search simulation is eight, and that for the outer feedback iterations is four. Thy also include comparison with LDPC code Cb (576, 288). When using a feedback process in the receiver [7], simulation results show improvement with serially concatenated LDPC codes compared to a single large-length LDPC code.

3. Proposed system

The proposed system for serially concatenated LDPC codes includes two non-identical LDPC codes. The process begins by generating irregular LDPC codes (rate 1/3) and selecting a pair of LDPC codes. One code is selected as the outer encoder with a small code length, and the second code is compatible with the outer encoder output length and acts as the inner encoder. Note that this pair of LDPC codes is coupled using a random interleaver. The proposed system encoder is shown in Fig. 4.

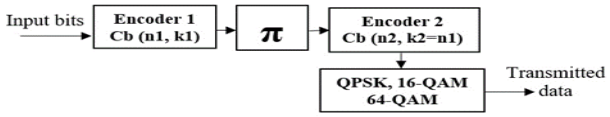


Fig. 4: Proposed encoder scheme.

In this study, we simulated quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (QAM), and 64-QAM modulation schemes. The channel includes AWGN. Pairs of LDPC codes for two case studies are given in Table 1.

Table 1. Ldpc Code Pair

Case study	Outer encoder	Inner encoder
First	Cb (72, 24)	Cb (216, 72)
Second	Cb (360, 120)	Cb (1080, 360)

Note that no feedback process is employed on the receiver side, i.e., only the inner decoder iteration is performed. Here, the number of decoder iterations is 10. The system receiver is shown in Fig. 5. The decoder complexity is varied relative to the selected LDPC encoder on the transmitter side. Note that using a short-length outer LDPC coder can reduce decoder complexity.

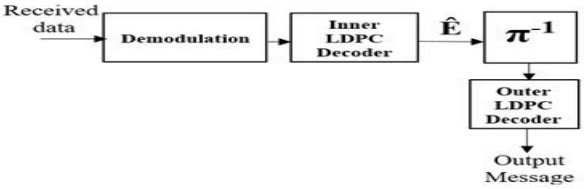


Fig. 5: Proposed serially concatenated LDPC receiver.

The receiver side performs a process that is reciprocal to that performed on the transmitter side. The demodulation process is first stage for the received symbols, and then the inner LDPC decoder decodes the input data. However, the inner LDPC decoder uses a soft decision process such that it provides the estimation output of decoded data, this estimation then passed to receiver next stage. The random de-interleaver enhances system performance relative to the BER verses the signal-to-noise ratio. Finally, the outer LDPC decoder makes a hard decision in binary data form.

4. Simulation results

The simulation test examined two cases. The first case examined the serial concatenation of two irregular LDPC codes Cb (72, 24) as the outer LDPC encoder and LDPC codes Cb (216, 72) as the inner encoder. The simulation examined three modulation schemes independently, i.e., QPSK, 16-QAM, and 64-QAM. The second case considered concatenation between Cb (360, 120) as the outer code and Cb (1080, 360) as the inner encoder. The simulation focused on system performance enhancement relative to BER with serially concatenated LDPC codes rather than a single LDPC code (10 iterations for each LDPC decoder). The abbreviation SCC refers to Serially Concatenated Codes.
The simulation results are shown in Figs. 6–11.

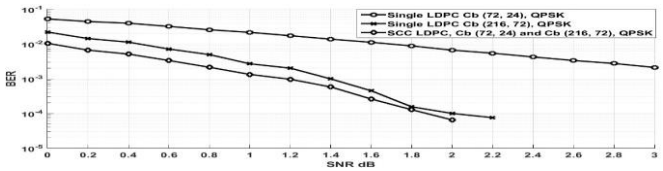


Fig. 6. SCC LDPC codes with QPSK Cb (72, 24) and Cb (216, 72).

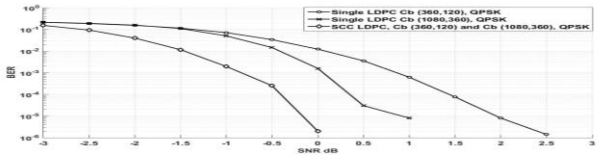


Fig. 7. SCC LDPC codes with QPSK Cb (360, 120) and Cb (1080, 360).

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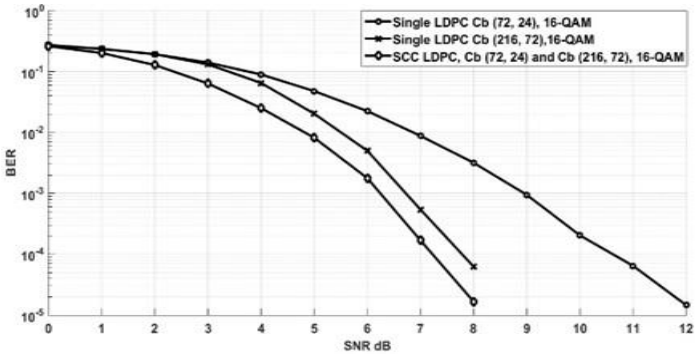


Fig. 8. SCC LDPC codes with 16-QAM Cb (72, 24) and Cb (216, 72).

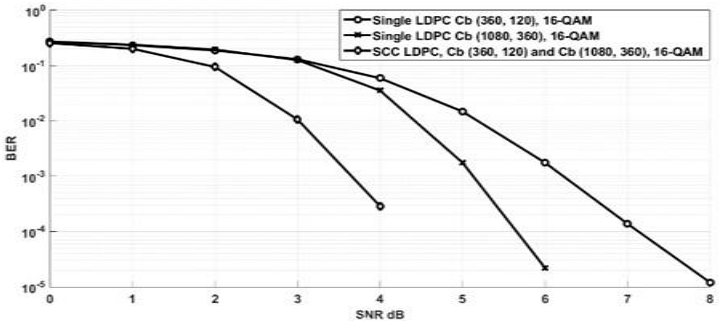


Fig. 9: SCC LDPC codes with 16-QAM Cb (360, 120) and Cb (1080, 360).

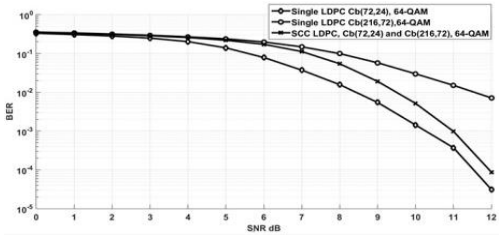


Fig. 10: SCC LDPC codes with 64-QAM Cb (72, 24) and Cb (216, 72).

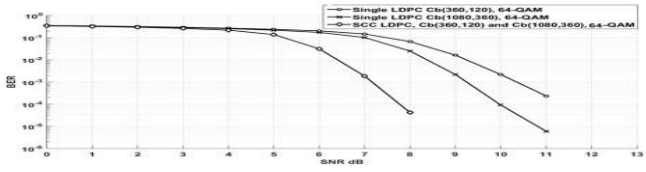


Fig. 11: SCC LDPC codes with 64-QAM Cb (360, 120) and Cb (1080, 360).

Table 2. Summarize simulation results comparison between different modulation schemes

Modulation Type	LDPC code (N, K)	SNR dB	BER
QPSK	C_b(72, 24)	3	0.0020958
QPSK	Cb(216, 72)	2.2	7.5008×10^{-5}
QPSK	SCC LDPC Cb(72, 24) and Cb(216, 72)	2	6.4583×10^{-5}
QPSK	Cb(360, 120)	2.5	1.4003×10^{-6}
QPSK	Cb(1080, 360)	1	8.0051×10^{-6}
QPSK	SCC LDPC Cb(360, 120) and Cb(1080, 360)	0	2.0003×10^{-6}
16-QAM	Cb(72, 24)	12	6.4583×10^{-5}
16-QAM	Cb(216, 72)	8	6.2506×10^{-5}
16-QAM	SCC LDPC Cb(72, 24) and Cb(216, 72)	8	1.6667×10^{-5}
16-QAM	Cb(360, 120)	8	1.2002×10^{-5}
16-QAM	Cb(1080, 360)	6	2.2014×10^{-5}
16-QAM	SCC LDPC Cb(360, 120) and Cb(1080, 360)	4	0.00028805
64-QAM	Cb(72, 24)	12	0.0071646
64-QAM	Cb(216, 72)	12	8.7509×10^{-5}
64-QAM	SCC LDPC Cb(72, 24) and Cb(216, 72)	12	3.125×10^{-5}
64-QAM	Cb(360, 120)	11	0.00023604
64-QAM	Cb(1080, 360)	11	6.0038×10^{-6}
64-QAM	SCC LDPC Cb(360, 120) and Cb(1080, 360)	8	4.2002×10^{-5}

5. Conclusion

In this study, we have proposed the use of a pair of different serially concatenated LDPC codes rather than two identical LDPC codes. The proposed code pair has matching code length. Irregular LDPC codes (rate 1/3) were generated and tested using a serial concatenated code. In addition, a feedback process is avoided on the receiver side, which reduces the number of iterations and system complexity. Our simulation considered three modulation schemes (QPSK, 16-QAM, and 64-QAM) because these are important standard modulation schemes in long-term evolution applications. The serial concatenation of LDPC codes as a pair allows for a short-length LDPC code in the outer encoder. The low number of iterations used in the simulation (i.e., 10 iterations). The simulation results demonstrate improved system performance compared to a standalone LDPC code all values listed in Table 2. In addition, the results show enhanced system performance when using a pair of LDPC codes of greater length. Note that the selection of code length in a pair of serial concatenated LDPC codes should consider the tradeoff between system performance and complexity. Longer code lengths lead to greater decoder complexity. Practical implementation of proposed system LDPC as compatible pairs could be achieved by using FPGA.

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