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Research paper

A Study on the Advanced Logic State Diagnosis of Logic Lab-unit for Digital Education

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Abstract

Background/Objectives: In this paper, a method to distinguish +3.3*V* logic state from the 4-level logic state (i.e., 0*V*, open, +5*V* and high-voltage) diagnosis circuit of the logic lab-unit was proposed.
Methods/Statistical analysis: It is theoretically verified that the conventional logic state diagnosis circuit is difficult to distinguish the +3.3*V* logic state; the proposed method can distinguish logic state clearly.
Findings: In order to verify the performance of the proposed method, the 6-chanel diagnosis circuit was set up to measure the output for each logic state. In the conventional method, it is possible to distinguish between open state and +3.3*V* logic state within the 0.43*V* under the ideal condition. However, it cannot distinguish them under the noisy condition.
Improvements/Applications: On the other hand, the proposed method is measured 1.96*V* (i.e., increased by 455%) between the open state and the +3.3*V* logic state without affecting other states. In addition, the robustness of the measurement was verified in a noise environment. Since the proposed method is used by the microcontroller and analog multiplexer, it can be implemented with only one tri-state buffer or one transistor. Therefore, the proposed method is economically advantageous, as well.

***Keywords*:**logic-lab, digital logic, education kit, logic level, 5-level, logic display

1. Introduction

Electronic devices have been digitalized due to the development of microprocessors and other digital technologies, and these trends have been accelerating. In contrast to electronic devices designed with analog circuits in the past, the proportion of digital circuits in electronic devices has been increasing in recent years. For example, the DC power supply has changed to a compact, high capacity, high efficiency switching mode power supply (SMPS)[1,2]; television has changed from analog composite type to digital smart-TV; phono-record and cassette tape were replaced by CD and MP3. The microprocessor which is the ultimate in digital circuit handles determination functions and complex sequences. In addition, various communication interfaces such as Internet, Wi-Fi, HDMI, and USB have been standardized in combination with digital communication technology. New digital fields such as Internet of Things (IOT)[3,4], big data, and Block-chain have emerged based on the microprocessor. For this reason, demand for engineering education and research on digital circuits also increase in educational institutions and research institutes. Furthermore, digital education equipment and laboratory equipment are required to adapt to rapid change environments.

One of the essential digital devices used by educational institutions is the logic lab unit (digital circuit training kit), which provides the basic functions that a learner can carry out a digital circuit practice. Although it is a device used by a novice who is not familiar with circuits, equipment protection against learner mistakes is not robust. The conventional logic state display circuit for indicating the output state of the circuit is simply configured to turn on the LED when the input is at +5*V* and turn off at otherwise[5]. Because it is configured to only operate on the +5*V* input, the GND short or high-voltage cannot be protected by the mistake of user.

In order to solve this problem, Lee et al.[6,7] proposed a method to detect and display four states: open (i.e., no-connection), logical-Low, +5*V* logical-High and high-voltage. Meanwhile, conventional digital circuits have been designed based on +5*V* TTL level, but recent digital circuits have been widely used +3.3*V* systems for speed and power consumption. For example, microprocessors such as AVR[8], PIC[9], ARM processor[10] and TFT color LCD module[11] are configured to operate at + 3.3*V*. In addition, the 74LV series[12] is configured to be compatible with +3.3*V*system, and convertible elements[13] are used with conventional +5*V* system. This trend leads to +3.3*V* logic in the logic lab-unit for educational practice. Lee et al.[14] analyzed the possibility of distinguishing +3.3*V* logic from the 4-level logic state diagnosis circuit and concluded that it is difficult to distinguish between open state and +3.3*V* logic due to the tolerance of the devices. In fact, there were some mathematical errors in the paper, but modified mathematical analysis results in a rather difficult to distinguish of it.

In this paper, a methodology to clearly distinguish +3.3*V* logic input is proposed in 4-level logic diagnosis circuit. The principle of the convectional 4-level logic state diagnosis circuit is analyzed and the state of +3.3*V* logic input to this circuit is theoretically analyzed. Two methods are proposed that can clearly distinguish +3.3*V* logic. A better method is selected by comparing the proposed methods. The proposed method is verified through experiments.

2. 4-Level Logic State Diagnosis Circuit

2.1. Principle of 4-Level Logic State Diagnosis Circuit

The 4-level logic state diagnosis is based on circuit in figure 1[6,7]. The largest voltage difference in each state is

$$R_1 = R_2 = 2 \cdot R_3 \quad (1)$$

In the figure 1, a Zener diode is used to cut off the overvoltage and minus voltage.

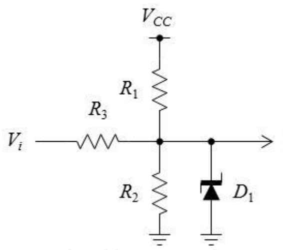


Figure 1: 4-level logic state diagnosis circuit

If this circuit is configured with the same conditions as equation (1), divided voltage by R_1 and R_2 appears in the open state; V_o becomes half of V_{CC}. The output voltage of the circuit for 4-logic states and 8-bit analog-to-digital conversion (A/D C)[15] values are shown in table 1. HV (High Voltage) is a voltage greater than +5V.

Table 1: Output voltage for each logic state

Input	V_o [V]	8-bit A/D C
H.V.	5	255 (0xFF)
+5V	3.75	191 (0xBF)
Open	2.5	127 (0x7F)
0V	1.25	63 (0x3F)

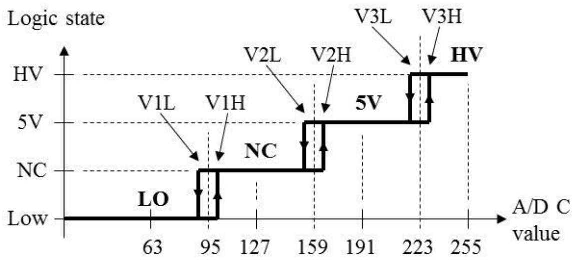
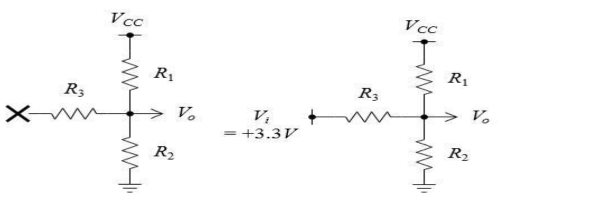


Figure 2: Discriminant boundary of logic state

The boundary of each logic state is defined based on table 1. In order to prevent unstable state at the boundary point, 4-level logic states can be distinguished by software hysteresis as shown in figure 2.

2.2. Distinction between Open State and + 3.3V Logic State

In order to analyze that the diagnosis circuit of the figure 1 can distinguish between open state and +3.3V logic state, equivalent circuit of open state and +3.3V logic state are shown in figure 3[14].



(a) Open state **(b) +3.3V logic state**
Figure 3: Equivalent circuit of open state and +3.3V logic state

The output voltage in open state as shown in the figure 3(a) can be expressed by equation (2).

$$V_{o,NC} = \frac{R_2}{R_1+R_2} \cdot V_{CC} \quad (2)$$

When +3.3V logic state of the figure 3(b) is analyzed by superposition principle [16], the output voltage is

$$V_{o,3} = \frac{R_2 \cdot R_3 \cdot V_{CC} + R_1 \cdot R_2 \cdot V_3}{R_1 \cdot R_2 + R_1 \cdot R_3 + R_2 \cdot R_3} \quad (3)$$

Therefore, the difference voltage between the two states can be calculated by

$$V_{diff} = \frac{R_2 \cdot R_3 \cdot V_{CC} + R_1 \cdot R_2 \cdot V_3}{R_1 \cdot R_2 + R_1 \cdot R_3 + R_2 \cdot R_3} - \frac{R_2 \cdot V_{CC}}{R_1+R_2} \quad (4)$$

If equation (1), V_{CC}=+5V, and V_3=+3.3V are substituted into equation (4), V_{diff} = +0.4V can be obtained. It is notice that the voltage difference between open state and +3.3V logic state is only 0.4V, i.e., 8% of V_{CC} = +5V. Therefore, it is necessary to verify that the microprocessor can accurately determine the state in worst conditions (i.e., errors in devices and voltage sources).

2.3. Error Analysis

Simulation studies are performed to verify that open state and +3.3V logic state can be accurately distinguished regardless of the elements error in the 4-level logic state diagnosis circuit. The simulation is shown in figure 4 when errors occur within ±5% for all the parameters in equation (4).

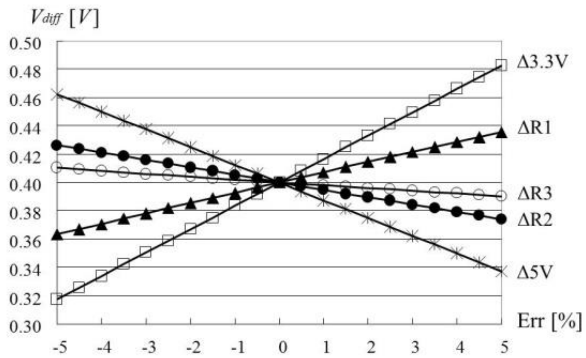


Figure 4: Simulation results of differential voltage with error of 4-level logic state diagnosis circuit parameters

The smaller the R_1 is set, the less the voltage difference become, while the larger the R_2 and R_3 is set, the less the voltage difference become as shown in the figure 4. Especially, the change of +3.3V and +5V is the most dominant factor. If all the conditions are the worst (i.e., -5% for R_1 and +3.3V, +5% for R_2, R_3, and +5V, respectively), the differential voltage is 0.1845V(3.69% of V_{CC}) based on equation (4). Because the 8-bit A/D C value is only 9, it can be diagnosed within a limited condition. However, this result is possible on the assumption that there is no noise at all. In order to minimize the influence on the circuit to be diagnosed, each resistance element should be used at least 100$K\Omega$. Since the input line is open as shown in the figure 3(a), noise can cause misdiagnosis. It is noted that the circuit is vulnerable to noise by long wire disconnection. In addition, since the variation range of hysteresis is limited, unstable state can occur at the threshold as shown in the figure 2.

3. Improved Diagnosis Circuit for Logic-Lab Unit

In this paper, two methods for clearly distinguishing between open state and +3.3V logic state are proposed, and a better method is selected by comparative analysis.

3.1. Switched Pull-Up Type

Figure 5 shows the first proposed circuit. U_1 is a switch consisting of a tri-state buffer or a transistor. If the power supplied to the pull-up resistor R_1 is turned off by U_1 or Q_1, the equivalent circuit of the open state and the +3.3V logic state can be shown in figure 6.

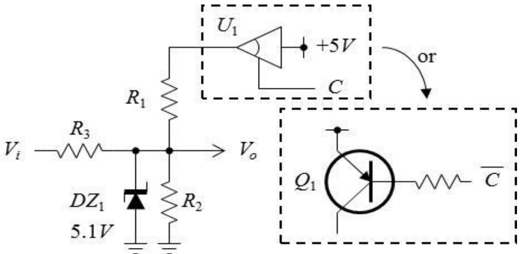
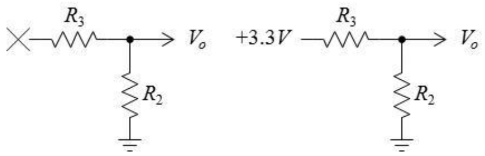


Figure 5: Proposed diagnosis circuit-I (Switched pull-up type)



(a) Open state **(b) +3.3V logic state**

Figure 6: Equivalent circuit of the open state and the +3.3V logic state for C = off in switched Pull-up type

In the figure 6(a), the output voltage is 0V, because the pull-up resistor is ignored in the open state. The equivalent circuit of the +3.3V logic state is a voltage divider as shown in the figure 6(b). Therefore, output voltage is calculated by equation (5).

$$V_{o,3} = \frac{R_2}{R_2+R_3} \cdot 3.3 \tag{5}$$

Substituting equation (1) into equation (5) yields

$$V_{o,3} = \frac{2 \cdot R_3}{3 \cdot R_3} \cdot 3.3 = 2.2\ [V] \tag{6}$$

Thus, the voltage difference from the open state is obtained, i.e.

$$V_{diff} = V_{o,3} - V_{o,NC} = 2.2\ [V] \tag{7}$$

3.2. Switched Pull-Down Type

Figure 7 shows the second proposed circuit. If the power supplied to the pull-down resistor R_2 is turned off by U_1 or Q_1, the equivalent circuit of the open state and the +3.3V logic state can be shown in figure 8.

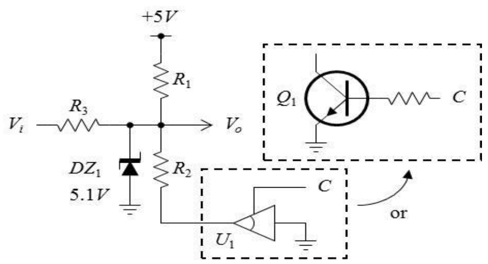
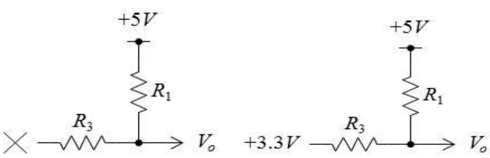


Figure 7: Proposed diagnosis circuit-II (Switched pull-down type)



(a) Open state **(b) +3.3V logic state**

Figure 8: Equivalent circuit of the open state and the +3.3V logic state for C = off in switched Pull-down type

In the figure 8(a), since the pull-down resistor is ignored in the open state, the output voltage is 5V. Like switched pull-up type circuit, the equivalent circuit of the +3.3V logic state is a voltage divider as shown in the figure 8(b). Therefore, output voltage is calculated by equation (8).

$$V_{o,3} = \frac{R_3}{R_1+R_3} \cdot (5 - 3.3) + 3.3 \tag{8}$$

Substituting equation (1) into equation (8) yields

$$V_{o,3} = \frac{R_3}{3 \cdot R_3} \cdot 1.7 + 3.3 = 3.867\ [V] \tag{9}$$

Thus, the voltage difference from the open state is

$$V_{diff} = V_{o,NC} - V_{o,3} = 1.133\ [V] \tag{10}$$

Comparing the results of equation (7) and (10), it is more advantageous to design the switched pull-up type because the voltage difference is larger. The results of the switched pull-up type are summarized in table 2.

Table 2: Output voltage using switched pull-up type

Input	C	V_o [V]	8-bit A/D C
+12V	**1**	5	255 (0xFF)
+5V	**1**	3.75	191 (0xBF)
+3.3V	**1**	2.9	148 (0x94)
	0	2.2	113 (0x71)
N.C.	**1**	2.5	127 (0x7F)
	0	0	0 (0x00)
0V	**1**	1.25	63 (0x3F)

3.3. Flowchart of Detection Process

Figure 9 shows a flowchart of software to determine the logic state using the proposed method.

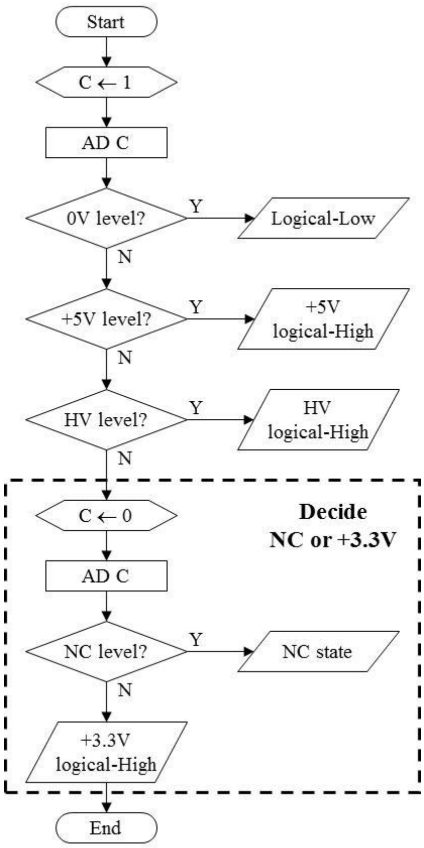


Figure 9: Flowchart of diagnosis logic state for logic lab-unit

Before the determination, the pull-up switch is set to on (C ← 1) to diagnose the state using A/D C. If the open state is diagnosed, the pull-up switch is set to off (C ← 0) and A/D C is used to distinguish between open state and +3.3V logic state.

3.4. Expansion of Multiple Inputs

In general, the digital lab unit has at least eight logic circuit inputs. Since conventional devices use discrete elements, multiple identical circuits should be used.

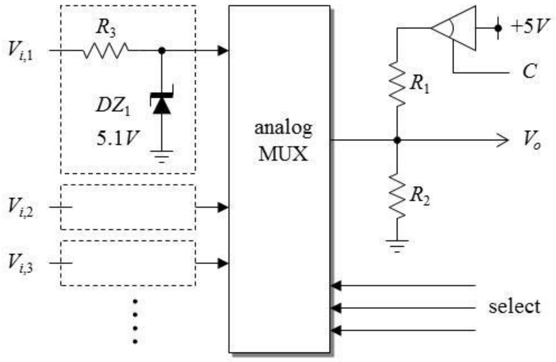


Figure 10: Example of channel expansion for diagnosis circuit

In contrast, proposed circuit design is simple that R_1 and R_2, and open-collector gates is used with only one set, because an analog multiplexer (MUX)[17] is used and controlled by a micro-controller as shown in figure 10.

3.5. Performance Verification

An experimental circuit was setup as shown in figure 11 in order to verify the performance of the proposed method.

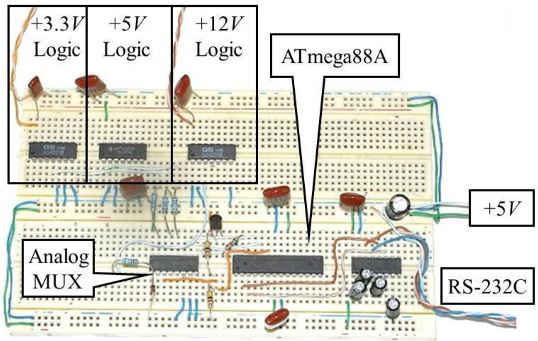
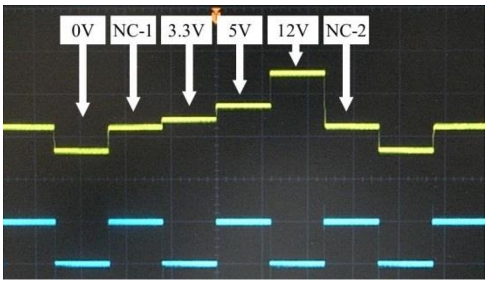
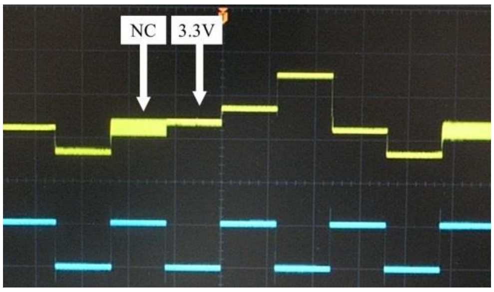


Figure 11: Diagnosis circuit for experiment

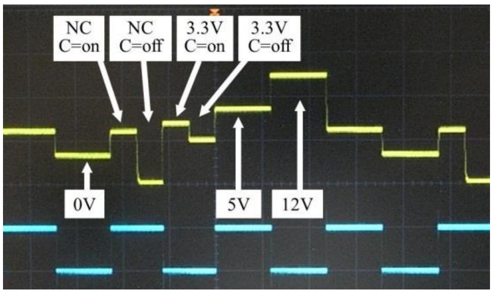
The experimental setup consists of: 1) ATmega88A micro-controller[18]; 2) 4051 CMOS analog MUX[17] for multi-channel; 3) output of logic gate with +3.3V, +5V, and +12V. Micro-controller is configured to execute A/D C while switching each channel and to transfer data to PC by RS-232C. Figure 12 shows the output of the analog MUX. The Ch2 waveform at the bottom is generated by the micro-controller to check when the channel is switched. Each channel is connected to 6 states of 0V, NC-1, +3.3V, +5V, +12V, and NC-2 and it is configured to scan periodically in the micro-controller.



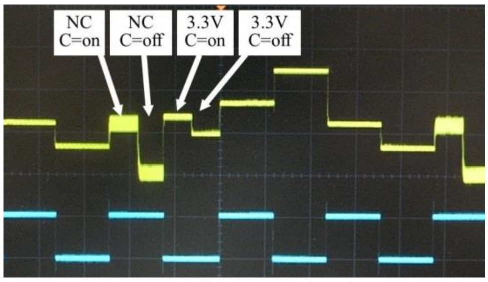
(a) Disabled pull-up control



(b) Disabled pull-up control with noise



(c) Active pull-up control



(d) Active pull-up control and noise

Figure 12: Experiment result of diagnosis circuit for logic lab unit (Time/Div = 2mS, Volt/Div: Ch1 = 2V, Ch2 = 5V)

Figure 12(a) shows the output waveform when the pull-up is not controlled. The open state and the +3.3V logic state have similar value. Figure 12(b) shows that noise is applied to the input connected to NC-1 and +3.3V logic without controlling pull-up, and misdiagnosis occurs between open and +3.3V logic. The noise generation setup is as follows; 30Cm wires are connected to the NC-1 input and +3.3V logic input respectively, and the square wave from the signal generator is close to the input line. The +3.3V logic input is not much affected by noise due to the output impedance of the logic gate, but open state is affected by noise.

Figure 12(c) shows the output waveform with controlled pull-up. When C = off, the open state voltage and +3.3V logic voltage can be clearly distinguished from the micro-controller. Figure 12(d) shows the output waveform with controlled pull-up and noisy environment. When C = off, it is noted that the open state voltage and +3.3V logic voltage can be clearly distinguished from the micro-controller.

The voltage and A/D C values of each state measured in the case study are shown in table 3 and figure 13. When C = off (i.e., pull-up is off), micro-controller can clearly distinguish the open state from the +3.3V logic state in spite of the noisy environment.

Table 3: Theoretical output and measurements output according to each state by proposed method

C	Input	Theoretical		Experimental		
		V_o [V]	A/D C	V_o [V]	A/D C	V_{diff} [V]
On	+12V	5	255	4.69	239	-
On	+5V	3.75	191	3.39	173	-
On	+3.3V	2.9	148	2.69	137	0.43
	N.C.	2.5	127	2.26	115	
Off	+3.3V	2.2	113	1.96	100	1.96
	N.C.	0	0	0	0	
On	0V	1.25	63	1.18	60	-

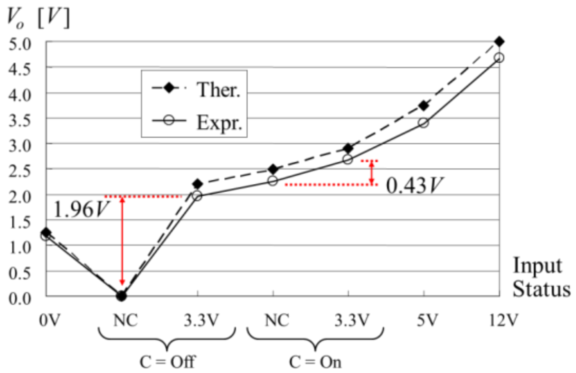


Figure 13: Theoretical output and measurements output according to each state by proposed method

4. Conclusion

In this paper, a method to distinguish +3.3V logic state from the 4-level logic state (i.e., 0V, open, +5V and high-voltage) diagnosis circuit of the logic lab unit was proposed. It is theoretically verified that the conventional logic state diagnosis circuit is difficult to distinguish the +3.3V logic state; the proposed method can distinguish logic state clearly.

In order to verify the performance of the proposed method, the 6-chanel diagnosis circuit was set up to measure the output for each logic state. In the conventional method, it is possible to distinguish between open state and +3.3V logic state within the 0.43V under the ideal condition. However, it cannot distinguish them under the noisy condition. On the other hand, the proposed method is measured 1.96V (i.e., increased by 455%) between the open state and the +3.3V logic state without affecting other states. In addition, the robustness of the measurement was verified in a noise environment.

Since the proposed method is used by the microcontroller and analog multiplexer, it can be implemented with only one tri-state buffer or one transistor. Therefore, the proposed method is economically advantageous, as well.

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