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Research paper

Optimization of PFC SEPIC Converter Parameters Design for Minimization of THD and Voltage Ripple

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Abstract

This paper discusses the current total harmonic distortion (THD_i) and voltage ripple minimization of SEPIC converter based on parameters design optimization. This conventional PFC SEPIC converter is designed to operate in discontinuous conduction mode in order to achieve almost unity power factor. The passive components, i.e., inductor and capacitor are designed based on switching frequency and resonant frequency. Meanwhile, the ranges of duty cycle for buck and boost operations are between 0<D<0.5 and 0.5<D<1, respectively, for the output voltage variation of the converter. The principle of the parameters design optimization is based on the balancing energy compensation between the input capacitor and output inductor. The experimental results show that, the current THD is reduced to 2.66% from 70.9% after optimization process is conducted. Furthermore, it is confirmed that the output voltage ripple frequency is always double from the input line frequency, $f_L = 2f_{out}$ and the output voltage ripple is always lower than the maximum input voltage ripple. Therefore, the designed parameters of the experimental converter is confirmed with approximately 65 W of the converter output power.

Keywords: *Optimization Parameter Design; Output Voltage Ripple; Power Factor Correction; SEPIC Converter; Total Harmonic Distortion.*

1. Introduction

In recent years, portable electronic equipment has advanced from a power converter and has the advantages of high efficiency, small in size and possess a wide input and output voltage ranges [1]–[3]. On the other hand, the conventional power converter is not able to operate a wide operation range and at the same time maintaining high efficiency; especially when the step up and step down voltage conversion need to be achieved [2], [4], [5]. Besides, battery voltage decreases as the battery discharges and lead to various difficulties if there is no voltage control. Therefore, the most effective method of regulating voltage through a circuit is by using a DC/DC converter. SEPIC converter can be used as a DC voltage regulator due to the ability of the converter to stepping-up or stepping-down the voltage. For example, a 48 V nominal output voltages from a single input voltage source is useful in various cases such as electrical machines, LED applications, solar energy systems, electric vehicle, data communication and telecom power systems [6]–[8].

Some power application systems requires an AC supply as an input. Meanwhile, rectifier and DC/DC converter are used to convert AC to DC accordingly to the load requirement. Nevertheless, the use of bridge rectifier, transformer, inductor, and capacitor can produce DC output voltage without distortion but will cause the input current to be extremely distorted. Hence, an AC/DC conversion are totally required in PFC converters to ensure the input voltage and input current are purely sinusoidal. Several circuit topologies; boost, buck-boost, SEPIC, and Cuk converter have been developed for PFC applications.

Generally, a conventional PFC converter circuits consist of combination between full-bridge rectifier and SEPIC converter. The circuit structure usually has integration issues. Basically, the output voltage from full-bridge rectifier is not a constant DC voltage. Therefore, the energy from the output full-bridge rectifier must be transferred to the SEPIC converter effectively without any 'extra' energy. If the energy is not effectively transferred, the input current THD can be affected at the input side and increase the output voltage ripple.

Thus, in order to solve the problems, conventional PFC SEPIC parameters require to be optimized where minimization current THD and the output voltage ripple are considered. The parameters design is based on the standard of IEC 61000-3-2 [9]–[11]. The PWM signal given to the switch is generated by using Altera DE2 as in [12], [13].

2. PFC SEPIC Converter

A PFC SEPIC is a type of conventional PFC converter that allows the step-up and step-down of the output voltage. Figure 1 shows the full-bridge rectifier part that requires four standard-diode as a bridge, meanwhile large inductor and large capacitor are required to filter the harmonics for the SEPIC part. The operation of SEPIC is same as the conventional buck-boost converter, which the polarity of the output voltage is always positive.

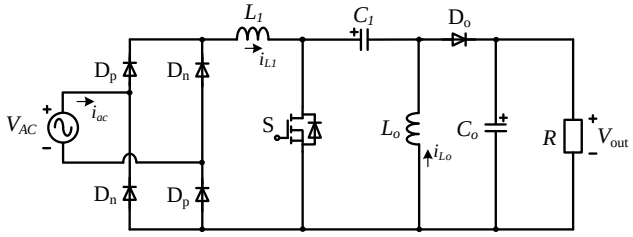

Fig. 1: PFC SEPIC converter circuit

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Generally, the characteristics of the conventional PFC SEPIC converter and SEPIC converter are different, where the output voltage of SEPIC converter can be stepped-up or stepped-down with designed components and the output voltage ripple is always low. When the same specifications and parameters of the SEPIC converter are applied in the conventional PFC SEPIC converter, the current THD and output voltage ripple become high. Therefore, the output inductance and output capacitance are required to be optimized in order to reduce the current THD and output voltage ripple.

2.1. Basic principle of SEPIC converter

Theoretically, when a duty cycle approaches unity, the DC gain will reduce towards zero [14]. The switching frequency need to be considered for parameters optimization purpose. Once the duty cycle increases, the switching frequency decreases which results the ripple current on the inductor to decrease. Figure 2 shows the DC gain characteristics for the SEPIC converter. Besides, the structure as depicted in Figure 1, it consists of buck and boost operations whereby for the buck operation, the duty cycle is less than 0.5 and the duty cycle is greater than 0.5 for the boost operation.

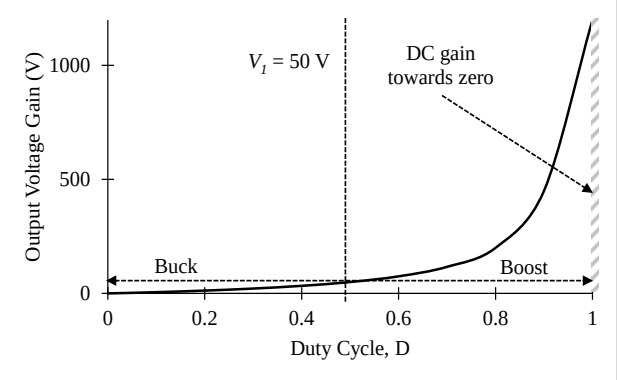


Fig. 2: DC gain characteristics for the SEPIC converter

2.2. Operation of PFC SEPIC converter

The PFC SEPIC converter circuit with single switch is controlled by duty cycle. This circuit can be divided into six operating modes and consist of positive and negative half cycles. Figure 3 shows the operation modes during the positive and negative half cycles.

Mode-1 and Mode-4: Mode-1 is positive half cycle while mode-4 is negative half cycle. When switch S is turned-on, the energy is stored in L_1. At the same time, C_1, L_o, and C_o are discharged. During this interval, diode D_o is turned-off and the power supplied to the loads is shown in Figure 3 (a) and 3(b).

Mode-2 and Mode-5: Mode-2 is positive half cycle while mode-5 is negative half cycle. When the switch S is turned-off, the inductor L_1 recharges the capacitor C_1, inductor L_o, and capacitor C_o through the freewheeling diodes D_o and supplies power to the loads as shown in Figure 3(c) and 3(d).

Mode-3 and Mode-6: Mode-3 is positive half cycle while mode-6 is negative half cycle. During the same state when the switch S is turned-off, the capacitor C_1 stores energy through the discharging inductors L_1. Inductor L_o, and capacitor C_o are discharging. During this interval, the diode D_o is turned-off and the power supplied to the loads is shown in Figure 3(e) and 3(f).

2.3. Parameter design of PFC SEPIC converter

Table 1 shows the specifications to design the passive elements which are the capacitors and inductors. Based on the operation mode, the passive elements are estimated based on the DCM condition.

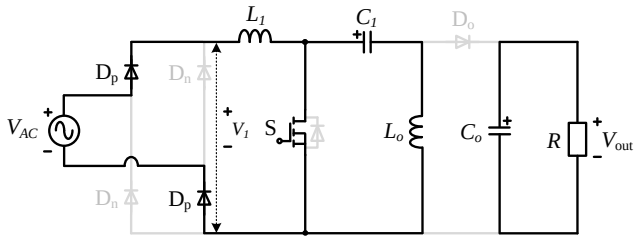
Table 1: Specifications

Parameters	Values
Input voltage, V_{AC}	(50-100) V
Frequency line, f_L	50 Hz
Period of line voltage, T_L	0.02 s
Output voltage (DC), V_o	48 V
Output power, P_{out}	65 W
Switching frequency, f_s	50 kHz
Maximum input current ripple, Δi_{L1}	< 25% of fundamental current
Output voltage ripple, ΔV_o	< 5% of V_o

2.3.1. Input inductor determination

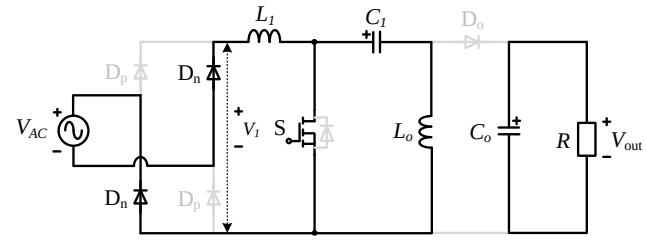
The input inductors (L_1) are expressed in Eqn. (1) with input voltage (V_{AC}) is in positive and negative half cycles.

$$L_1 = \frac{V_{AC}(t) \cdot D}{\Delta I_{L1} \cdot f_s} \quad (1)$$



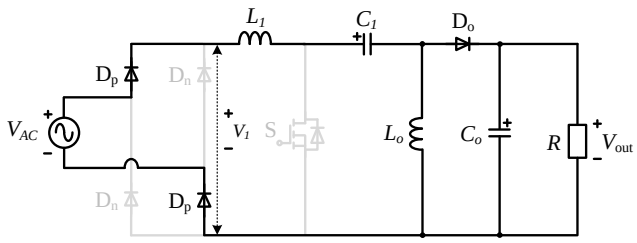
Mode-1: Positive half cycle during t_{on}

(a)



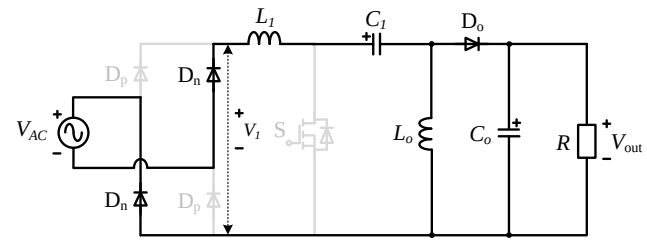
Mode-4: Negative half cycle during t_{on}

(b)



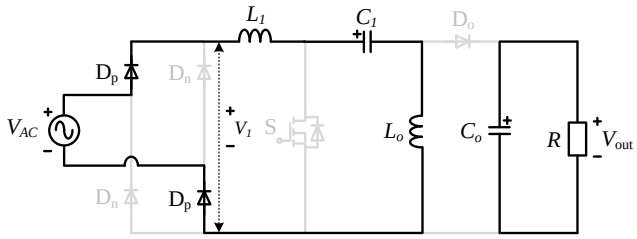
Mode-2: Positive half cycle during t_{off}

(c)

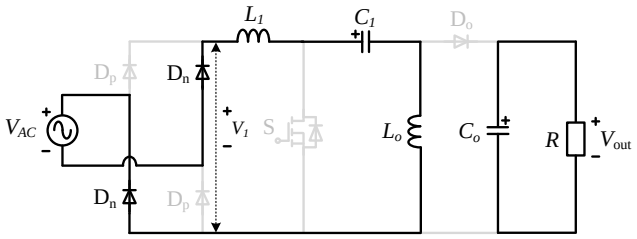


Mode-5: Negative half cycle during t_{off}

(d)



Mode-3: Positive half cycle during t_{off} (e)



Mode-6: Negative half cycle during t_{off} (f)

Fig. 3: Mode operation during positive and negative cycle (a) Mode-1, (b) Mode-4, (c) Mode-2, (d) Mode-5, (e) Mode-3, and (f) Mode-6

2.3.2. Output inductor determination

The voltage conversion ratio M in terms of the rectifier parameter can be obtained by applying the power-balance principle [9]:

$$M = \frac{V_o}{\sqrt{2} \cdot V_{AC}} \tag{2}$$

The value of $K_{e\text{-}critical}$ can be evaluated by:

$$K_e < K_{e-critical} = \frac{1}{2(M+2)^2} \tag{3}$$

To ensure the operation is in DCM, the following value of K_e is selected:

$$K_e = 0.85 \times K_{e-critical} \tag{4}$$

Thus, by evaluating the parameter K_e gives an equivalent inductance L_e value of

$$L_e = \frac{K_e \cdot R_L}{2 \cdot f_s} \tag{5}$$

The value of L_o can be expressed as follows:

$$L_o = \frac{2L_1 \cdot L_e}{L_1 - L_e} \tag{6}$$

2.3.3. Input capacitor determination

The input capacitors C_1 and C_2 will not cause a low-frequency oscillations with the converter inductors. Thus, the energy transfer from capacitors C_1 and C_2 are determined based on the inductor L_1 and L_o such that the line frequency (f_L) should be lower than the switching frequency (f_s). Thus, a better initial approximation for choosing the resonant frequency (f_r) is given by [5]:

$$f_L < f_r < f_s \tag{7}$$

$$f_r = \frac{1}{2\pi\sqrt{C_1(L_1 + L_o)}} \tag{8}$$

2.3.4. Output capacitor determination

The output voltage ripple frequency of the converter is two times of the input frequency. Therefore, C_o can be obtained as follows:

$$C_o = \frac{P_o}{4 f_L \cdot V_o \cdot \Delta V_o} \tag{9}$$

2.4. PFC SEPIC converter optimization

Figure 4 shows the optimization parameters of L_o and C_1 with current THD, however the allowable current THD range must be within 1.8% to 4% in order to estimate L_o and C_1 for optimization purpose. Energy of L_o and C_1 must be compensating each other. Otherwise, the remaining energy of L_o will be transferred to the source and consequently the quality of input current line will be affected. As aforementioned problem, 2% current THD level is used as a reference to ensure the efficiency of the proposed converter is high and current THD is low, according to the standard of IEC 61000-3-2.

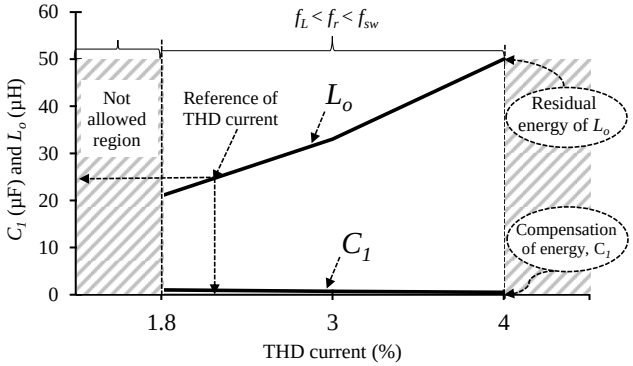


Fig. 4: Optimization parameter of L_o and C_1 with current THD

The capacitor ripple current Δi_c and capacitor voltage ripple ΔV_c are expressed by Eqns. (11) and (12). In addition, the output voltage ripple is expressed by Eqn. (14).

$$\Delta i_c = \Delta i_L = \frac{V_L}{L_o} DT_s \tag{10}$$

$$\Delta V_c = \frac{1}{C}\int i_c dt \tag{11}$$

$$\Delta V_{ESR} = \Delta i_c \cdot ESR \tag{12}$$

$$\Delta V_o = \Delta V_c \cdot \Delta i_{ESR} \tag{13}$$

Based on Eqn. (10), the output voltage ripple is reduced when the capacitance is increases. After all the parameters are optimized by considering availability of market, the PFC SEPIC converter specifications are listed as shown in Table 2.

Table 2: Optimization parameter design of passive element

Parameters	Values
Input inductor, L_1 and L_2	2.2 mH
Output Inductor, L_o	22 µH
Coupling capacitor, C_1 and C_2	1 µF
Output Capacitor, C_o	2400 µF

3. Results

Referring to the Table 2, the simulation and experimental results are discussed by focusing on the minimization of current THD and output voltage ripple.

3.1. Minimization of current THD

During the simulation of the converter circuit, all the switching devices and components are assumed ideal with no losses. Figure

5(a) and Figure 5(b) show the input source voltage and input source current, respectively for PFC SEPIC converter. The quality of the input current is poor compared to the input line voltage, Figure 5.

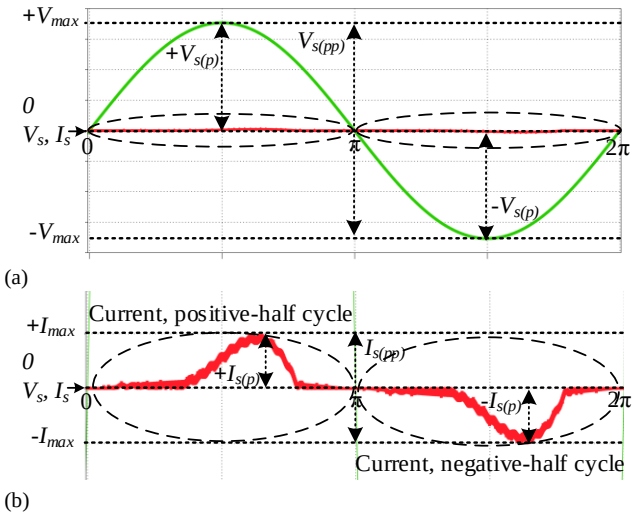


Fig. 5: Input source (a) voltage, (b) current

This means that the current THD is very poor in this condition and the percentage of the current THD in the input line current is 70.9%. Figure 6 shows the frequency spectrum of current THD where the percentage current THD is the worst. In other words, the single harmonic distortion in the input current is not the same as the single harmonic distortion in the input line voltage which is a pure sinewave. However, it does not mean this structure could not meet the IEC 61000-3-2 standards. The optimized parameter is needed to ensure the harmonic limits is always within the range of IEC 61000-3-2 standards.

The parameters for hardware experiment are listed in Table 1 and 2 are constructed to evaluate the performance of the proposed circuit as shown in Figure 1. The value of current THD is measured by using power analyser and all data are tabulated in one graph. In addition, the values of the switching frequency used are 50 kHz and 10 kHz with a fixed value of output capacitor which is 2400 µF to observe the current THD in terms of the ripple current as shown in Figure 7. From Figure 7(a), the current THD of 10 kHz switching frequency is used and the result of the current THD is high ripple current at the input line current with THD_i = 40.6%. In Figure 7(b), the switching frequency 50 kHz is used that produced THD_i of 56.9%. However, the current peak-peak is 1.4 A for both of the switching frequencies with the position of the sine wave is in phase and the voltage peak-peak is 141 V.

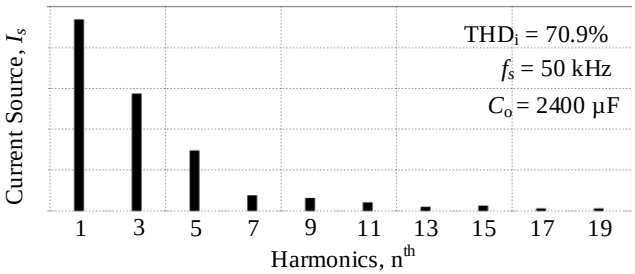


Fig. 6: Frequency spectrum of THD_i

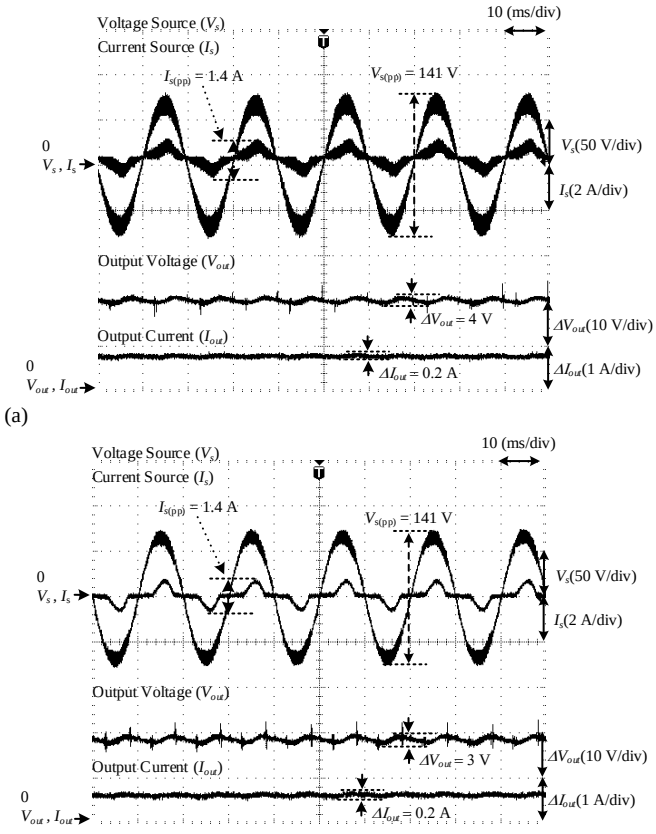


Fig. 7: THD current of switching frequency (a) 10 kHz, (b) 50 kHz

From Figure 7, when the switching frequency is increased, the poor current THD is produced and the output frequency is double from the line frequency for one cycle as shown in equation (15). The output DC is depend on half-wave and full-wave bridge rectifier is shown in Figure 8. However, the output voltage ripple is decreased which will be discussed in the next section.

$$f_L = 2 \cdot f_{out} \tag{14}$$

Figure 9 shows the frequency spectrum with various frequency and output capacitor value. The values of harmonics are collected from the fundamental to 11th harmonics by using power analyser. A 50 kHz and 470 µF has the 3rd and 5th highest harmonics for that results in poor current THD. However, for the 7th and 9th the harmonics component, the current is low compared to the other values.

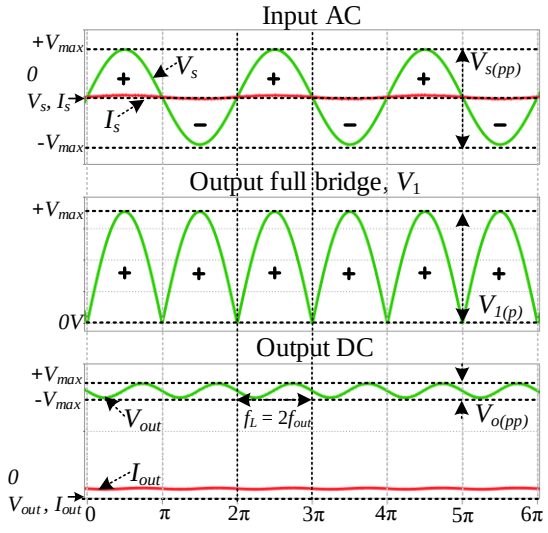


Fig. 8: Frequency line and frequency output DC

It means that to reduce current THD with regard standards IEC 61000-3-2, the highest values of 3rd and 5th should be minimized as much as possible.

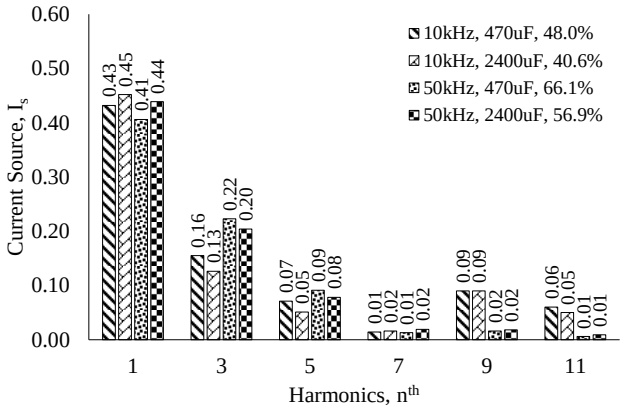


Fig. 9: Frequency spectrum with various frequency and output capacitor

Figure 10 shows the current THD component after optimization which is 2.66%. The lowest current THD for the conventional has some advantages in terms of the structure.

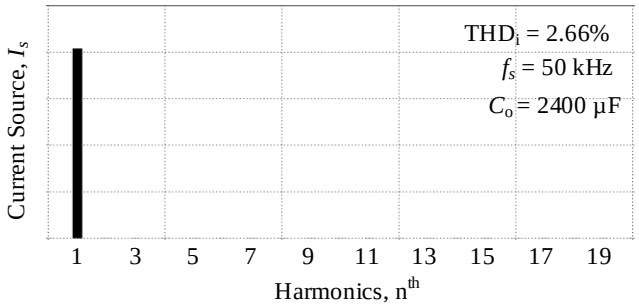


Fig. 10: THD_i component after optimization parameter

3.2. Minimization of output voltage ripple

Figures 11 shows the comparison of the output voltage and ripple current when the value of the output capacitor used are 470 µF and 2400 µF with a fixed switching frequency of 50 kHz. It can be seen that the output voltage ripple is reduced from 9.10 V to 1.16 V when the value of output capacitor is increased. However, the output current ripple also decreases from 0.26 A to 0.05 A when the capacitance is increased. Hence, the output ripple frequency of the structure is two times of the input frequency. In the worst case, the output current during the half period of ripple frequency is generated by the output capacitor.

Figure 11(a) shows the output voltage ripple with the output capacitor of 470 µF. In this case, the output voltage ripple is 9 V and the output current ripple is 0.4 A. It can be seen that the results of experimental is approximately agreed with the simulation results. The spike of the output voltage waveform is depending on the parasitic element parameters and the differences of the output voltage ripple waveforms will cause various effects when different types of capacitors are used. When the output capacitor is 2400 µF, the output voltage ripple is reduced to 3 V and output current ripple becomes 0.2 A. This is because when the capacitance is high, the output voltage ripple is reduced. Thus, the function of the output capacitor is to smooth the voltage as shown in Figure 11(b).

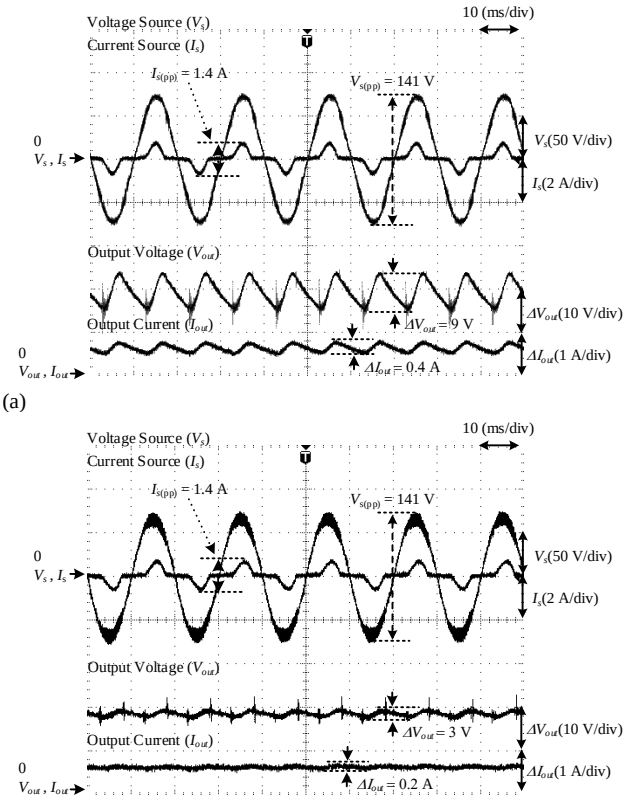


Fig. 11: Output voltage ripple with output capacitor (a) 470 µF, (b) 2400 µF

4. Conclusion

In this paper, a PFC SEPIC converter has been proposed and experimentally verified. The experimental results have shown a good agreement with the designed results. The current THD is 2.66% and less than the previous parameters optimization. Satisfaction of IEC 61000-3-2 requirement have been achieved by balancing the energy compensation of passive elements. Moreover, the output voltage ripple is reduced significantly with the output frequency is two times of the line frequency. Other than that, with higher power factor and efficiency, the structure can be applied to most of the consumer electronic products of 65 W rating in the market. This topology uses the combination of full-bridge rectifier and SEPIC converter structures with single switch (MOSFET). A high power factor can be achieved by applying any PWM switching pattern.

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