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Research paper

Performance of rc low encoding techniques for reducing coupling transitions

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Abstract

RC Network has delay propagation by wire and dynamic power dissipation. Basically it can perform two encoding techniques. They are Firstly it will reduce more dynamic power dissipation and delay propagation of wire simultaneously. Its simulation results of coupling activity and switching activity is more when the input is in Toggle state on 8-bit and for 32-bit data buses It increases. To reduce dynamic power is bus and total propagation delay the encoding techniques is Introduced which reduces coupling Coupling transitions, Dynamic power. Secondly it will also reduce more total power consumption when Width of Bus and Length of Bits Increases Its coupling activity is Reduced Gradually when the Data moves for one state to another State and switching activity is Reduced

***Keywords*: :** *Toggle:Power:Activities:Coupling:Consumption:Delay .*

1. Introduction

In power dissipation has major combination of technology scaling, the mobile battery of electronic products and increase awareness of natural heating.Large attributes of power dissipation in Integrated circuit process is charging and discharging of interconnect capacitance. Cross coupling capacitance between adjacent wires on same metal layer has effect on circuit parameters and power.Coupling capacitance may decrease and switching power can reduce by increase internal wire space as chip level is increased. Transmit the number of changes is more than half of the bus width. Real data is changed with opposite value and control line is set to "high". Else the Real data is transmitted and control line is set to "low".The Real data bus width is changed from 8-bit to 9-bit , from 16-bit to 17-bit , or from 32-bit to 33-bit. There are many techniques to solve the problem statement .The Literature survey focus on the Issues which is Related to Encoding techniques .some techniques are hardcoded and some techniques represents the behavior of data and some techniques focus on comparison of Length of Bus Structure . In this paper we discuss the Encoding techniques with Boolean Logical diagram and Its Impact on Bus Structure

2. Interconnect RC bus model and power expression.

We introduce the terms which are used for description as follows :

d(t): Data on a bus at present and has to sent at time t, (source at time t).

d(t-1): A data previously on bus at a time t-1,(source at time t- 1).

E(t): Encoded value is sent presently on bus lines at time ,(encoded word at t)

E(t-1):previously Encoded value is sent on bus lines at time t-1,(encoded at t -1).

I(t): A bus line for acting bus is changed or not at time t.

I(t-1): A bus line for acting bus is changed or not at time t-1.

P0(t),P1(t),P2(t),P3(t): The 0^{th},1th,2th & 3th input bits are sent presently at time t.

PP0(t),PP1(t),PP2(t),PP3(t): The 0^{th},1th,2th & 3th bits on encoded are sent presently at time t.

The source of capacitance are two types.They are load capacitance (C_L) and coupling capacitance (C_C)

A capacitanceby load indicates wire-to-ground capacitance.

A coupling capacitance is in between wire and adjacent wires.

Dynamic power consumption on coding bus is calculated as

$P_{D,coded} = (\alpha_{CL}+\lambda * \alpha_{CC} * C_C)*V_{DD}^2*f$

$P_{D,coded} =(\alpha_{CL}+\lambda * \alpha_{CC})*V_{DD}^2*f$

Where C_L is load capacitance ,C_c is coupling capacitance,V_{DD} is supply voltage ,f

is clock frequency and λ is capacitance ratio.

The un-coded dynamic power consumption is defined as

$P_{D, un\text{-}coded}= (1+\lambda) * C_L*V_{DD}^2*f$

Capacitance ratio is defined as coupling capacitance to load capacitance $\lambda = C_C / C_L$

The Total Power in the Bus Model is Given By $P= C.V^2_{DD}.f$

In the above power can be minimized by using capacitance in which The Rate of low of data and charging, discharing can be make to control the power by using

encoding techniques

2.1 Block Diagram of Basic encoder

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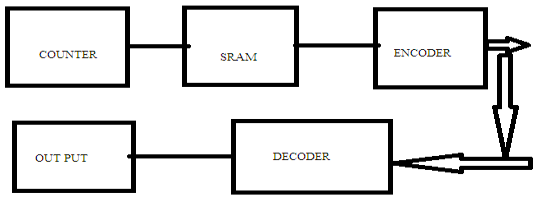


Fig.1: Basic block diagram.

The function if counter is to count the number of Boolean values that are coming from the interacting circuit SRAM is a Temporary memory device it stores the data as per the requirement and it assigns the data to Encoder.SRAM will have Adders Lines,unable pin,Disable pin,Reset pin,clock,wrt pin,rd pin.Depending up on the design of encoder we can use SRAM and we can configure the pins of the internal view of the circuit.Encoder Encodes the incoming stream of data .The are eight level of AND-OR network.The simple Two level AND-OR network is shown below.The internal view of Eight level is same as to that of Two level network

Internal View of Encoder Two Level Encoder

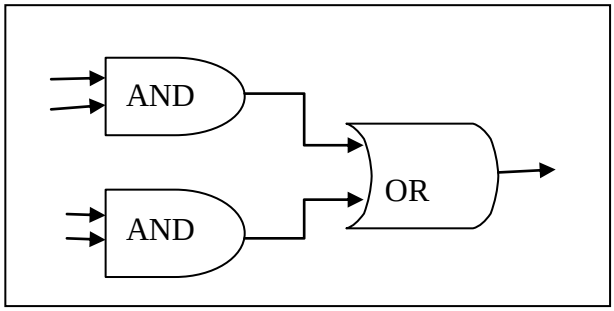


Fig..2 two level and gate

3. Algorithum

1.Let d(t) = d0(t)…….d7(t) be the data present on the Bus at time (t)
2.d(t-1) = d0(t-1)……..d7(t-1) be the data present on the bus at time(t-1)
3.count the change of bits from t to t-1 that is coupling count count.
4.compare the coupling count count value with half of width of bus and quarter width of bus.
5.If the Bits are changing continuously that is in toggle state then the change of capacitor is high there is chance of consuming more power couping transition is high so encode the bits with inverter.
6.I(t)= inverted particular [position of bit
I(t) = I0(t)……..I7(t) at time (t)
I(t-1) = I0(t-1)…….I7(t-) at time (t-1)
7.If coupling transition is high invert the particular bit either by odd or even or both odd and even and by using particular sequence such as continuous zeros and ones.
8.compare above statement with quarter and half of width of bus.if it is found greater then the encode the data
9.If the coupling transition count is still greater then use sequence shift or block shift to encode the data to reduce the coupling transition
10.The new bits will be P(t) = P0(t) ……p7(t)
11.The encoded bits will be pp(t) = pp0(t)…….pp7(t)

3.1Coupling Transition Reducing Techniques for Delay Network:

In this we can reduce not only power consumption but also propagation delay. We represent two inverting techniques for reducing propagation delay and power consumption.

3.1.1 Encoding Steps:

3.1.1.1Techique 1

Firstly it can divide bus width into several clusters. Each one has 4-bit width and an extra control bit. In 16-bit bus encoder as shown in below

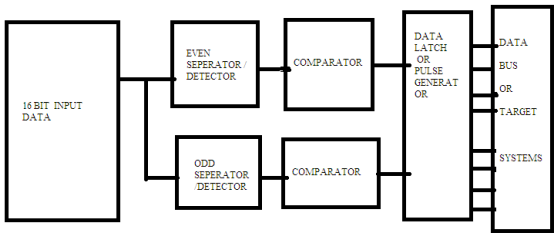


Fig.3: Block diagram to reduce proporgation delay

In the above circuit the 16 bit data is passed into even and odd detector. Even detector takes only even bits and odd detector takes only odd bits.If all even bits are same the comparator calls pulse generator and directly passes the output to the target system.If all the bits of odd detector are the same the comparatoe calls pulse generator to the target system. Instead of moving the data from detector to Target system

3.1.1.2Techique 2

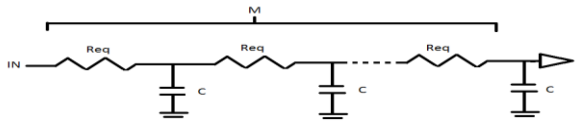


Fig.4 RC Network Interconnected Delay

The interconnected circuit consists of series of Resistance and capacitance in such circuit delay will be maximum.since the data has to move across the resistance and capacitance so the will be very slow and maximum delay will occurs.such problems can be overcome by using Basic Logic circuits where the repetitive values are sent directly into the target system without passing into the Network structures Bulk type RC network is shown Below

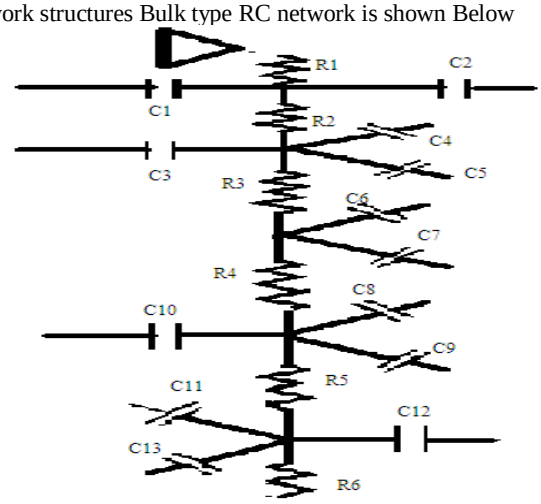


Fig.5 RC nework of roporgation delay

FIG 3. AND FIG 4 are the RC circuits in these circuits there exists a propagation delay these types if circuits depends on the Length of the wire and distance between the capacitor to capacitor In such case we can use the Block diagram of FIG.3 .we can also use Hard coded Logical circuits

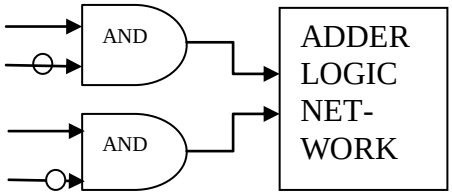


Fig.6 Hard coded Logical circuit

4. Simulation wave forms:

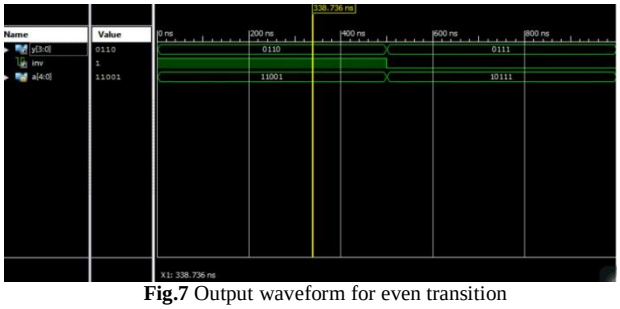


Fig.7 Output waveform for even transition



Fig.8 Output wave form for odd transition

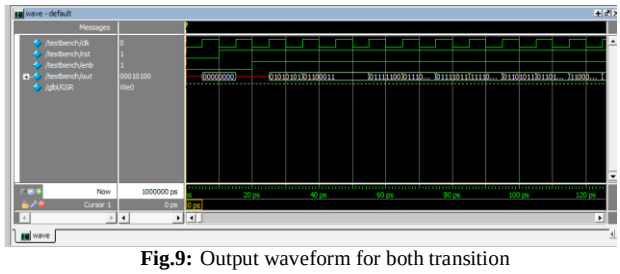


Fig.9: Output waveform for both transition

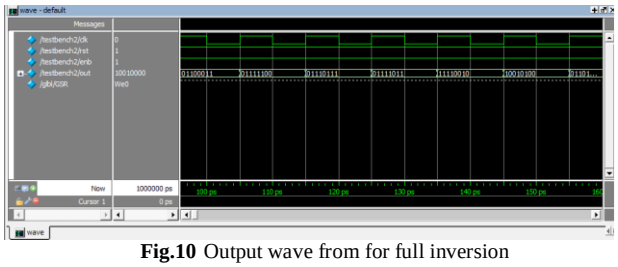


Fig.10 Output wave from for full inversion

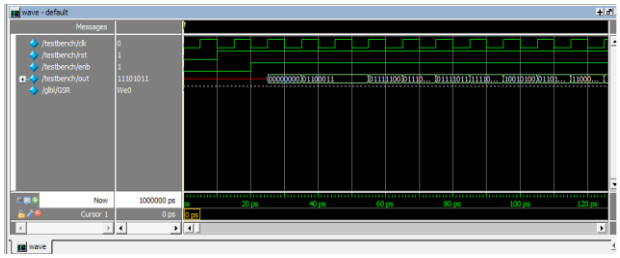


Fig.11: Output wave form for Block transition

Table. 1 comparison table for coupling transition

Methods/ Vectors	Normal method	Bus	Shift	Proposed
16-Bitsdata 500 vectors (set1)	8340	5735	5680	4420
16-Bitdata 500Vectors(set 2)	9720	6788	6200	4840
16-Bitdata 500(set3) Vectors	9340	6959	6559	6130

5. Conclusion

In this Research work we concluded that the performance of RC Encoding technique can be improved by Reducing coupling transitions .As shown in Table 4.1 Different data vectors with different set are simulated and we concluded that coupling transitions can be Reduced by using different Transitions Hence Power consumption is Reduced and power is saved with different encoding Schemes

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