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Research paper



Performance Analysis and Low Power Design of Voltage Level-up Shifters

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Abstract

Voltage level-up shifters are widely used in dual supply applications and it acts as an interface between main core and input-output units. Low power with efficient level-up shifter is designed by reducing the transistor count and the proposed level-up shifters are capable of converting from sub-threshold to above threshold level signal. The strength of pull-down networks and pull-up networks are enhanced by employing a couple of current mirror circuits. The simulation results of the proposed level shifter in 180nm technology yields a power dissipation of 95.79nw, propagation delay of 41.23ns for an input voltage of 0.4V and input frequency of 1MHz, low supply voltage VDDL=0.4V, high supply voltage VDDH=1.8V. Proposed 14T Level shifter in 90nm Technology demonstrates a power dissipation of 54.8nw, propagation delay of 28.8ns for an input voltage of 0.2V and input frequency of 1MHz, VDDL=0.2V, VDDH=1.2V.

Keywords: *Current mirrors, Dual supply voltages, Level-up shifter, Process variation, Sub threshold operation.*

1. Introduction

In VLSI design, the major constraints that are considered for an efficient integrated circuits are performance in terms of power consumption and delay, cost and consistency. With scaling in technology and integration, the power dissipation exponentially decreases whereas delay varies with respect to supply voltage, threshold voltage, load capacitance, aspect ratio (W/L) and thickness of oxide layer. Decreasing the input supply voltage has an adverse effect on performance factor but low power circuits can be achieved [1]- [3]. Dual supply architectures are employed in digital circuits and SOC, where different parts or sub units operates at different speeds and voltages. Dual supply circuits employ two supply voltages namely lower supply voltage (VDDL) and higher supply voltage (VDDH) which are applied to the circuit with non-critical paths and critical paths respectively. The need for level shifter emerges if a low supply voltage drives a high supply voltage, then PMOS may never turn off completely [2], [4]. Voltage level shifters are used to supply correct voltage levels between the digital blocks and it acts as an interfacing module between I/O circuit and core circuits within a dual supply architecture [5].

There are many power minimization techniques such as transistor sizing, voltage scaling, logic optimizations, multi-VDD that are employed to reduce dynamic power dissipation. In broad sense, the total power consumption is due to combination of dynamic and static power dissipations [6]. In order to reduce the power dissipation while converting from a lower voltage in below sub threshold voltage levels into nominal higher voltage levels, 15T and 14T voltage level shifters is designed.

The rest of the brief is permutated as follows. In section II, conventional and some high speed voltage level shifters are analyzed. Section III depicts the design of proposed voltage level shifters. Simulation results of proposed model are projected in section IV. The brief is concluded in section V.

2. Literature Survey

Level shifters based on dual supply architectures can be implemented using different logics namely differential cascade voltage switch logic, contention mitigation logic, current mirrors, wilson current mirrors. First conventional level shifter that was implemented in dual VDD systems used differential cascade voltage switch logic [7]. Conventional level shifter is also called cross-coupled level shifters which is depicted in Fig.1. The working of conventional level shifter can be explained by using two cases such as input signal supplied with higher logic (VDDL) and lower logic (ground or Vss). When input signal is applied with "VIN = VDDL= high", MN1 is ON which pulls the node Q1 down enabling MP2 ON. MN2 is OFF due to an inverting logic of input voltage. Cross coupling structure pulls up the node Q2 up to VDDH turning MP1 OFF. Similarly, when input signal is supplied with "VIN = Vss = Low", reverse operation is performed leading to lower output logic. Contention at nodes Q1 and Q2 occurs due to driven voltages VDDL and VDDH by pull-down network (MN1, MN2) and pull-up network (MP1, MP2) respectively which leads to higher power consumption. Conventional level shifter fails to operate if input voltage applied is below the threshold voltage levels and the potential difference of VDDH and VDDL is High. The strength of weak pull-down network was increased by replacing NMOS with CMOS logic, thereby reducing power consumption and delay when compared to conventional level shifter. The formation of such structure is known as conten-

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tion mitigation level shifter [8]. The contention between two nodes Q1 and Q2 still exists due to driven voltages VDDL and VDDH. So, upgraded version of level shifters such as current mirror level shifters (CMLS), Wilson current mirror level shifters (WCMLS) were developed to reduce overall power consumption and delay by decreasing the strength of pull-up network while the pull-down network is pulling down the output node [9]- [11].

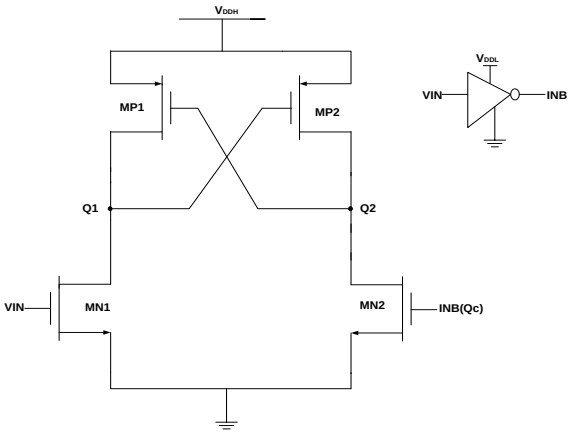


Fig. 1: Conventional Level Shifter

Current mirror level shifters (CMLS) employs current mirror circuits to ensure low power dissipation and its topology is interpreted in Fig.2. It eliminates the contention problem in conventional Level shifter. Current mirror circuits are more economical than resistors and leads to higher voltage gain at low power supply voltages [12]. If the input voltage signal is supplied with higher logic levels, then standby or static current flows through MP1 and MN1. To reduce static power dissipation, an additional PMOS is added to the above structure to form Wilson current mirror level shifter (WCMLS) [9] which is shown in Fig.3. MP3 is a feedback control PMOS because it acts as switch which turns ON only during transition times [14]. When input signal VIN applied is analyzed from low to high transition times, the circuit performs good providing the required level shifting at the output signal and no static current flows through MP1, MP3 and MN1. When the "High" to "Low" transition of the input signal is analyzed, smaller contention problem exists because of its dynamic behavior and MP1 tries to pull up while MN2 tries to pull down the output node. In order to overcome the problem of contention, an auxiliary circuit was proposed in [13] which turns on during "high" to "Low" transition of input signal.

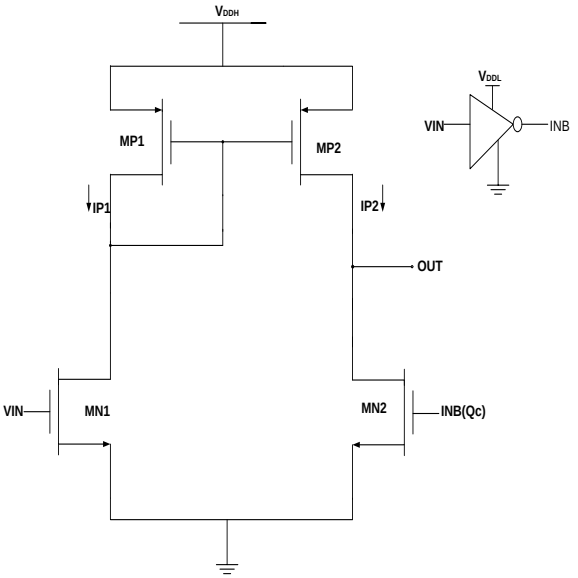


Fig. 2: Current Mirror Level Shifter

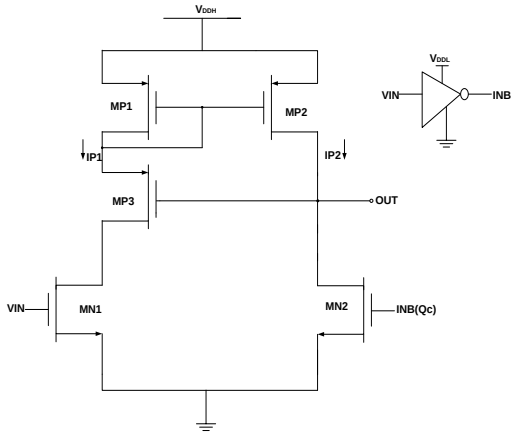


Fig. 3: Wilson Current Mirror Level Shifter [9]

Principle of existing Level Shifter illustrates the dynamic behavior of the structure shown in Fig.4 (a). Smaller conflict occurs between the pull-up networks and pull-down networks during the high to low transition of the input signal when the node A is pulled up by the difference of VDDH and Vth, where Vth is threshold voltage of MP1. Initially, when the input voltage is applied, the output OUT doesn't respond to its input voltage abruptly and hence during low to high transition of input pulse, smaller transition current flows through MN4, MN1 and MP1. MN4 is enabled due to overdrive voltage at MP3 and the current through MP3 is larger than that of MN3. Current mirror circuit replicates the current IP1 from MP1 to MP2 (IP2) which tries to pull the output node up. When the output node is pulled up, MP3 is turned OFF and MN4 is pulled down to ground that leads to no static current flow through the branch of MP1, MN1 and MN4.

Auxiliary circuit in the existing level shifter shown in Fig.4 (b) works during high to low transition of input pulse. It increases the static power lest it improves the performance of the structure by reduced power delay product (PDP). The value of IP1 and IP2 were reduced to improve the performance of the structure with lower power dissipation and higher speed. The motive of the auxiliary circuit is to pull the node QC up to a value greater than VDDL and current flowing through MP7 (IP7) should be small to attain low power and high speed. The structure operates for sub threshold input voltages. When VIN goes from high to low transition, output OUT doesn't corresponds to input pulse immediately and MN6, MN7, MP6 are turned ON leading to the current flow through them. MN5 is turned OFF and the current IP8 is mirrored to MP7 (IP7) which pulls the node QC up enabling MN2 with a voltage larger than VDDL and MP4 is turned OFF. No current flows through MN6, MN7, MP6, when the OUT is pulled down due to OFF state of MN6 which shows the compatibility of auxiliary circuit during high to low transition of input pulse only [13].

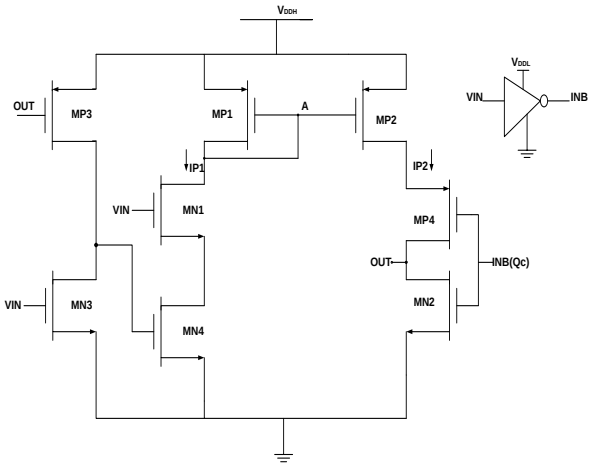


Fig. 4 (a): Principle of Existing Level shifter

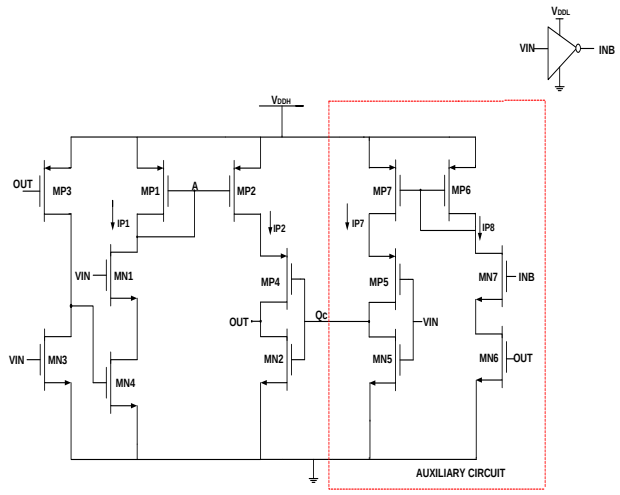


Fig. 4(b): Existing Level Shifter [13]

3. Proposed 15T &14T Level Shifters

Power consumption and transistor count were considered as a point of focus while designing the proposed voltage level up Shifters. As power consumption of any structure depends on number of transistor count and aspect ratio, proposed 15T and 14T level shifters have reduced power dissipation and conciliation in delay. Proposed 15T Level Shifter shown in Fig.5 (a) illustrates the combination of principle of existing structure [13] and a modification in auxiliary circuit. The structure performs a level-up shifting by using the modified auxiliary circuit. The modified auxiliary circuit operates as follows. When VIN changes from High to low transition, MN7, MP5, MN6 are turned ON enabling the flow of current (IP5) through it. The current IP5 is mirrored into IP6. MP6 and MN5 is turned ON and OFF respectively. Negligible amount of current flows through MP6 and MN5 and it provides enough voltage to pull up the node Qc greater than VDDL switching MN2 as ON and MP4 as OFF. Finally, when the output OUT is pulled down, MN6 is turned OFF and no current flows through the branch MP5, MN7 and MN6. The modified auxiliary circuit switches OFF during Low to High transition of input pulse.15T level shifter design acts as level-up shifter and transistor count is reduced in order to reduce switching power dissipation and overall power consumption. The currents IP1, IP2, IP5, and IP6 shown in Fig.7 are two pairs of current mirror currents.

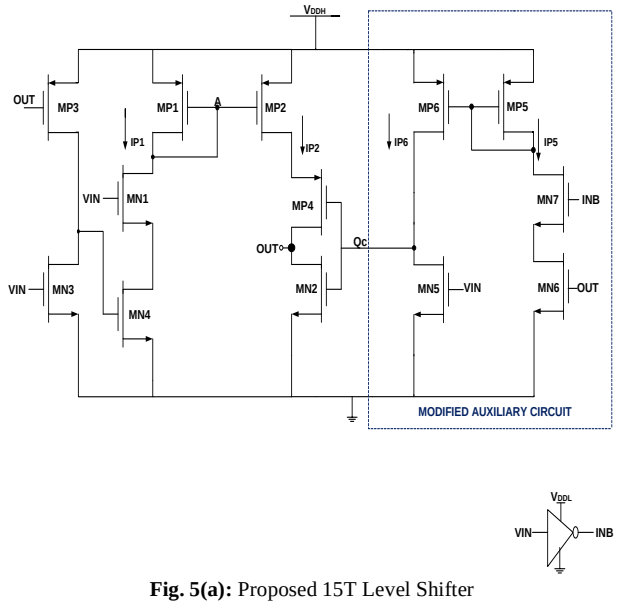


Fig. 5(a): Proposed 15T Level Shifter

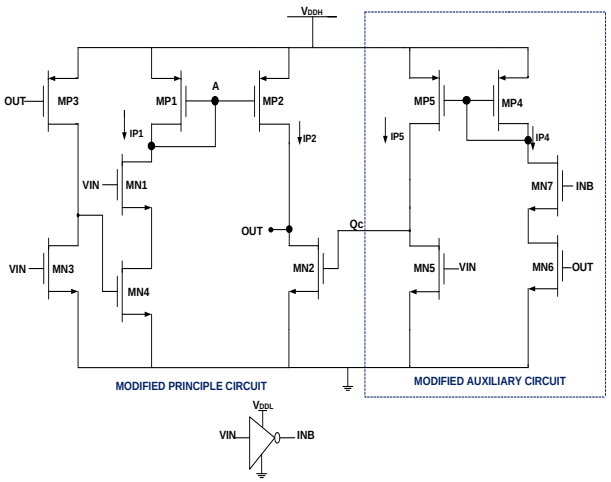


Fig. 5(b): Proposed 14T Level Shifter

Reconstruction of the Fig. 4(b) with a smaller change in principle of existing circuit and auxiliary circuit leads to structure of 14T level shifter as shown in Fig.5 (b). The operation of 14T level shifter has a modified auxiliary circuit which has similar operation as 15T level shifter. As the name auxiliary suggests that similar circuitry has to be maintained in order to have better performance, principle circuit is modified. A couple of current mirrors were used in design of level up shifters. During high to low transition times of input pulse, when MN2 is turned ON due to the node voltage at Qc which is greater than "High" logic. MN5 is turned OFF while MN7 is turned ON and the current in MP4 (IP4) is mirrored into IP5. MP4 drives the higher voltage (VDDH) enabling MN2 as ON and OUT is pulled up to a value of VDDH. Consequently, when the output OUT is pulled down, the modified auxiliary circuit becomes inactive and modified Principle circuit becomes active forcing the structure to perform voltage level shifting operation during Low to high Transitions of input pulse. In Fig.6, Timing results of proposed 14T Level shifter depicts the currents IP4 and IP5 are current mirror currents. This structure focuses on low power consumption and efficient design.

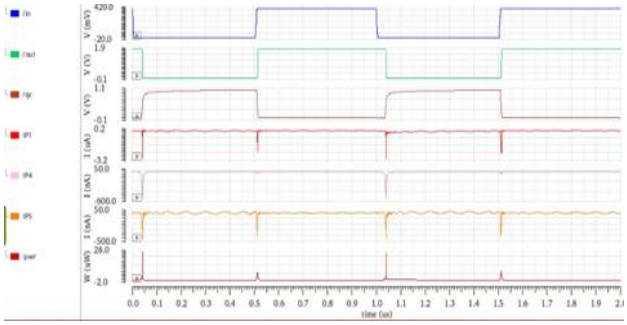


Fig. 6: Simulated waveform of Proposed 14T Level Shifter in 180nm Technology

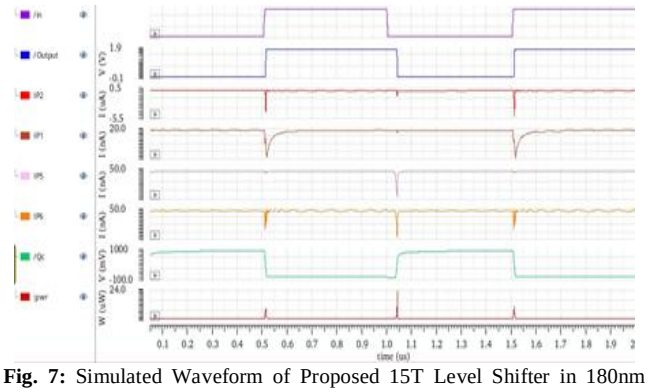


Fig. 7: Simulated Waveform of Proposed 15T Level Shifter in 180nm Technology

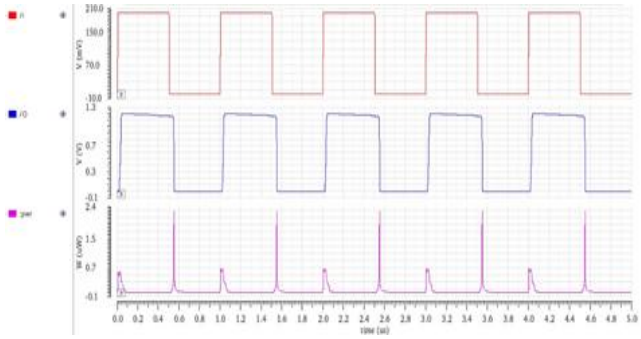
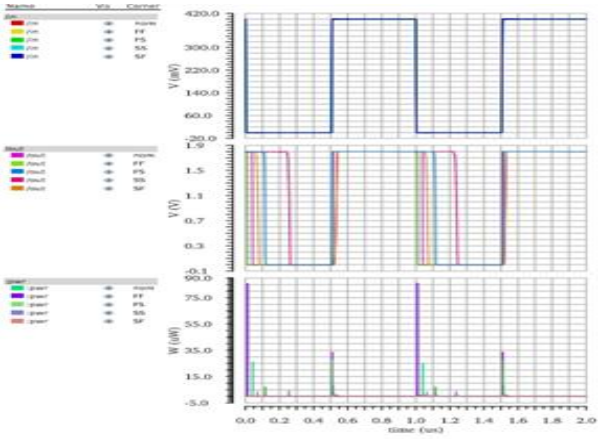
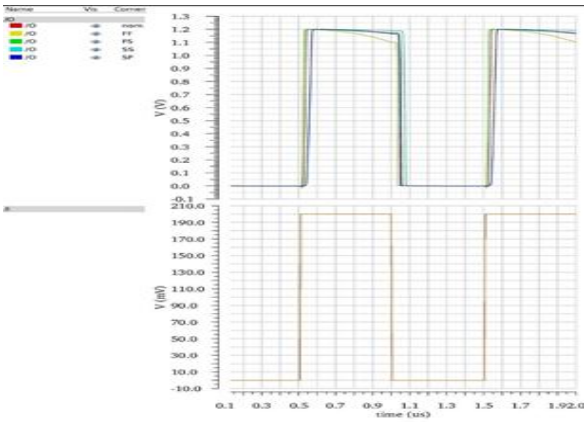


Fig. 8: Simulated waveform of Proposed 14T Level Shifter in 90nm Technology

Timing analysis of proposed 15T Level shifter is shown in Fig.7 which includes the current mirror pairs (IP1, IP2 and IP5, IP6), Power Dissipation and Output waveforms in 180nm Technology. Fig.8 shows the transient analysis of 14T Level Shifter in 90nm Technology which shows a conversion of 0.2V into 1.2V and Power dissipation at VDDL=0.2V and VDDH=1.2V Simulated results of Process corner variations using 180nm and 90nm Technologies are depicted in Fig.9 (a) and (b) respectively which illustrates the output wave at different corners with respect to timing intervals.



(a)



(b)

Fig. 9: Simulated waveform of proposed 14T Level Shifter Depicting Process corner variation in 180 nm and 90nmTechnology

4. Simulation Results

Performance and design of proposed level shifters were simulated in Cadence Virtuoso tool using gpdk180 and gpdk90 libraries. Simulation results of proposed structures are adhering to Process Corner Variations and functionality in terms of power, delay and PDP for VDDL=0.4V, VDDH=1.8V, input Frequency= 1MHz, input pulse (VIN=0.4V to 0V) in 180nm Technology. Proposed 14T Level shifter is designed with an aspect ratio of MP1 chosen in such a way that it must be smaller than MP2. Current mirror ratio of MP1 and MP2 is made large by changing the length of MP1 as 5um whereas lengths of other devices are selected as 0.18um. Strengths of pull up networks and pull down networks were maintained by varying the aspect ratio particularly the length of the devices. Widths of MP2 and MP5 is chosen as 1um and MN7 as 2um to improve the strength of pull-down network. All other transistor width is considered as 0.4um [13]. Substrates of PMOS and NMOS are connected to VDD and Vss respectively while designing the proposed level shifters. Existing level shifter [13] has a certain transistor sizing values which were taken as base in designing the proposed 15T level shifter. Since it is simulated in 180nm technology the common length is taken as 0.18um and common width as 0.4um. Proposed 15T level shifter has similar aspect ratio of [13] except the widths of MN5 as 0.4um and MN7 as 2um in order to maintain the equilibrium between the pull-up and pull-down networks.

Comparative simulation results of level shifters are depicted in Table.1 and Table.2 which shows reduction of power dissipation and slight variations in delay. Table.1 shows that the proposed 15T level shifter has better performance than proposed 14T level shifter and existing level shifter between the ranges of 1MHz to 20MHz input frequencies only. If we compare the overall performance of the structures, 14T Level shifter can be useful in dual supply architectures over a wide range of 1MHz to 500Hz input frequencies for consistency in low Power consumption.

Table 1: Comparative Simulation Results (180 nm Technology, VDDH=1.8V)

Input Frequencies (MHz)	Low Supply Voltage V_{DDL}(V)	Power Consumption (nW)		
		16T Level Shifter [13]	Proposed 15T Level Shifter	Proposed 14T Level Shifter
1	0.4	148.4	95.79	109.1
5	0.38	134.3	92.33	105.2
10	0.41	157.6	97.87	111.1
20	0.44	194	106.4	116.8
50	0.49	286.9	131.2	128.9
100	0.54	385.9	160.1	143
200	0.6	434.7	163.2	146.1
500	0.72	466	174.2	159

Table 2: Simulation Results of Proposed 15T and 14T Level Shifter (180 nm Technology, VDDH=1.8V)

Input Frequencies (MHz)	Low Supply Voltage VDDL(V)	Proposed 15T Level Shifter		Proposed 14T Level Shifter	
		Power (uW)	Delay (nsec)	Power (uW)	Delay (nsec)
5	0.38	0.0922	63.66	0.1052	60.08
10	0.41	0.0978	33.41	0.1111	31.8
20	0.44	0.1064	18.56	0.1168	17.77
50	0.49	0.1312	8.319	0.1289	8.044
100	0.54	0.1601	4.64	0.1430	4.523
200	0.6	0.1632	3.047	0.1461	2.99
500	0.72	0.1742	1.344	0.1590	1.313

Table 3: Comparative Analysis of Level Shifters without any change in aspect ratio. (180nm Technology- Low Supply Voltage VDDL=0.4V, High Supply Voltage VDDH=1.8V)

Parameters	16T Level Shifter[13]	Proposed 15T Level Shifter	Proposed 14T Level Shifter
Power Consumption(nW)	283.6	285.6	255.2
Delay (nsec)	47.77	46.57	25.25
Power Delay Product PDP (nW.nsec)	13547.57	13300.392	6443.8
Static Power Dissipation (nW)	0.126	0.126	0.1536

Comparative analysis of proposed level shifters with existing level shifter without changing the w/l ratio in Table.3 shows minimum Power delay Product as number of transistor count decreases and little variation in static power dissipation.Table.4 depicts the performance of proposed Level shifters when aspect ratio is changed to attain the desirable low power dissipation when input voltage VIN=0.4Vto 0V. Lower power consumption is found in proposed 15T Level shifter and delay is slightly higher than proposed 14T Level shifter. Table.5 depicts the performance of the proposed level shifters in 90nm technology with input frequency of 1MHz and VIN=0.2V. Better performance is observed in 14T level shifter with lesser power delay product.

Table 4: Performance of Different Level Shifters in 180nm Technology with Low supply voltage VDDL=0.4V, High supply voltage VDDH=1.8V, fin =1MHz

Name of the Level Shifters	Average Power (nW)	Delay (nsec)	PDP (nW.nsec)
Principle of Existing Level Shifter [13]	185.4	70.58	13085.532
16T Level Shifter [13]	148.4	30.5	4526.2
Proposed 15T Level Shifter	95.79	41.93	4016.47
Proposed 14T Level Shifter	109.1	39.08	4263.63

Table 5: Comparative Analysis of Level Shifters (90nm Technology- Low Supply Voltage VDDL=0.2V, High Supply Voltage VDDH=1.2V CL=0.5Ff)

Parameters	16T Level Shifter[13]	Proposed 15T Level Shifter	Proposed 14T Level Shifter
Power Consumption (nW)	63.07	60.56	54.84
Delay (nsec)	30.1	29	28.1
Power Delay Product PDP (nW.nsec)	1898.407	1756.24	1541

In proposed structures, process variations are simulated in ADEXL window of Virtuoso Tool. Different process corners such as FF, FS, SF, SS and typical are simulated with respect to Power Dissipation, Delay and VDDL parameters. Process corner variation results are generally required during fabrication of IC or chip design to test its robustness. Fig.10 (a) and Fig.10 (b) illustrates the variations of different corners with delay and power dissipation with respect to different voltages of VDDL in proposed 14T level shifter in 180nm technology and it is found that minimum delay and low power consumption is at even corners FF and SS respectively.

Process corner variation in proposed 15T level shifter shown in Fig. 11(a) and Fig. 11(b) illustrates the variation of delay and power dissipation with respect to different voltages of VDDL. In 90nm technology, variation of power dissipation with respect to different voltages of VDDL at different corners is shown in Fig.12 which projects that low power dissipation is found at SS Corner. Table.6 depicts the variations of different process corners with power and delay in proposed structures and it is observed that low power consumption is found at SS corners (Slow NMOS, Slow PMOS) and lesser delay at FF corner (Fast NMOS, Fast PMOS).

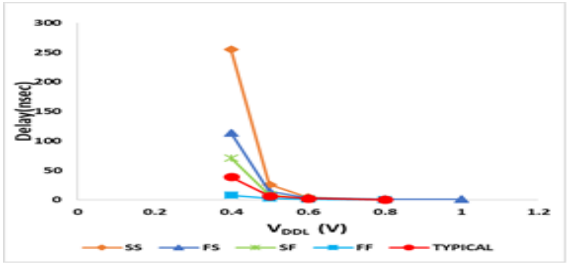


Fig. 10(a): Process Corner Variations with respect to Delay and VDDL (Proposed 14T Level Shifter using 180 nm Technology)

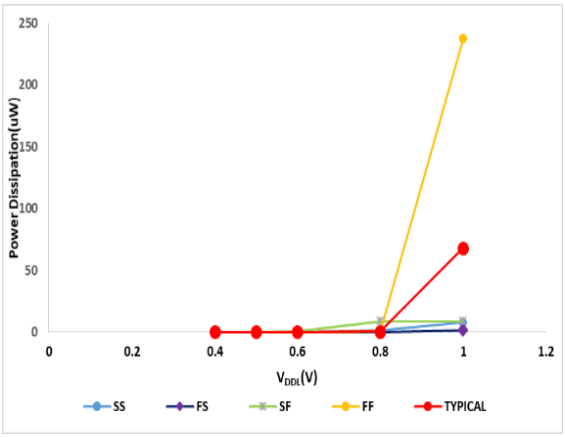


Fig. 10((b): Process Corner Variations with respect to Power Dissipation and VDDL (Proposed 14T Level Shifter using 180 nm Technology)

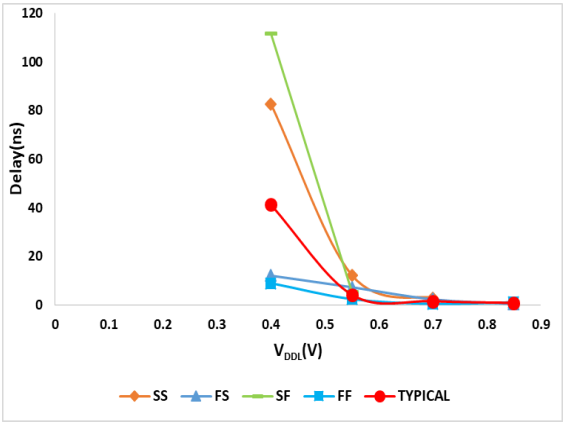


Fig. 11 (a): Process Corner Variations with respect to Delay and VDDL (Proposed 15T Level Shifter using 180 nm Technology)

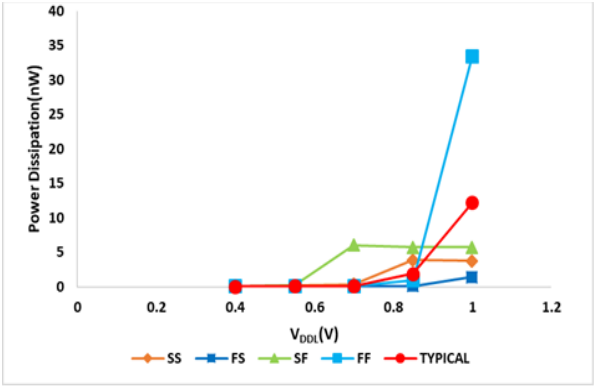


Fig. 11(b): Process Corner Variations with respect to Power Dissipation and VDDL (Proposed 15T Level Shifter using 180 nm Technology)

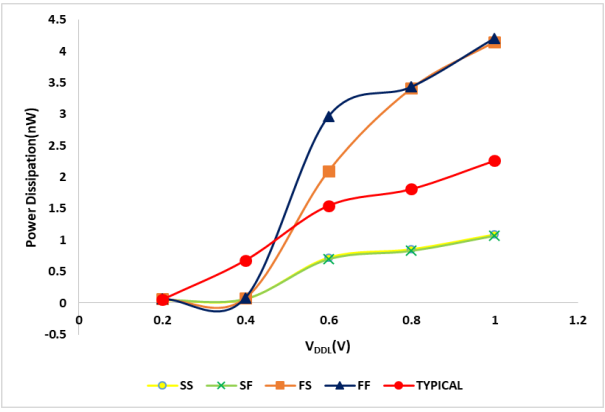


Fig. 12: Process Corner Variations with respect to VDDL and Power Dissipation. (Proposed 14T Level Shifter using 90 nm Technology)

Table 6: Process Corner Variations with respect to Power and Delay in Proposed Level Shifters in 180 nm Technology @ VDDL=0.4V

Corners	Proposed 15T Level Shifter		Proposed 14T Level Shifter	
	Power (nW)	Delay (nsec)	Power (nW)	Delay (nsec)
Typical	95.79	41.23	109.1	39.08
SF	91.07	111.7	99.71	71.23
FS	105.6	120.9	133.3	113.9
SS	82.72	285.0	83.33	255.3
FF	122.4	9.016	170.8	8.701

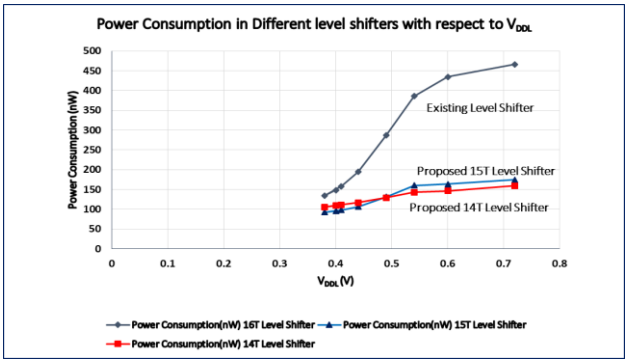


Fig. 13: Comparative Analysis of power consumption with respect to VDDL

The comparison graphs of power consumption with respect to variation of lower supply voltage and input frequencies shown in Fig.13 and 14 depicts that as the values of VDDL and input frequencies increases, Low power consumption is found in 14T Level shifter. Fig.15 shows the comparative analysis of different level shifters to project performance in terms of power dissipation and delay. Fig.16 shows the process corner variations with respect to power dissipation and delay in proposed 15T and 14T level shifters. Proposed structure performance is verified by Process corner variations.

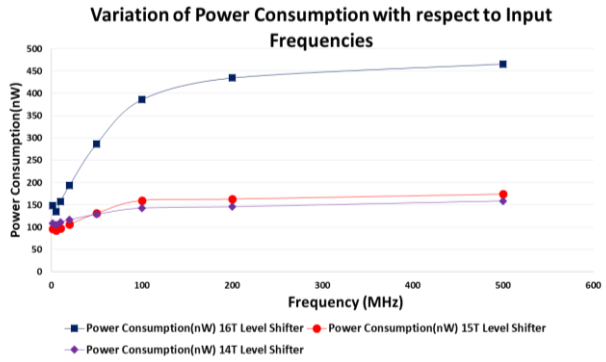


Fig. 14: Comparative Analysis of Power Consumption with respect to input Frequencies

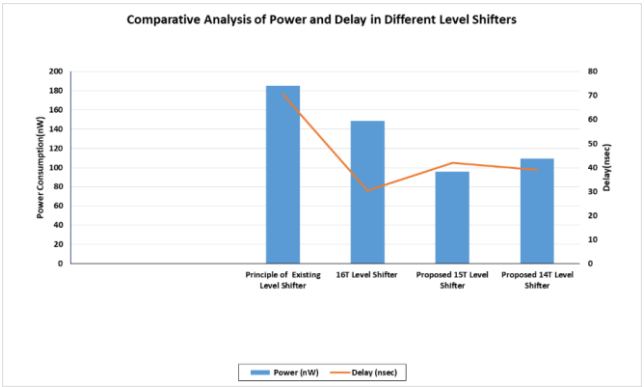


Fig. 15: Comparative Analysis of Power consumption and delay in different Level Shifters in 180nm Technology

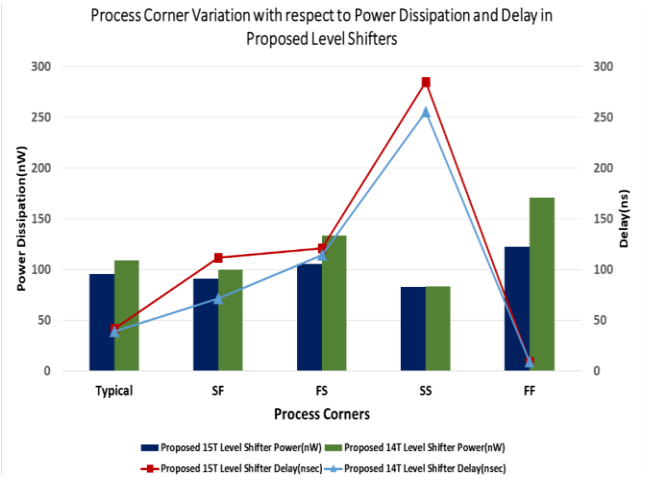


Fig. 16: Variations of Process Corners with respect to Power Dissipation and Delay in Proposed 15T and 14T Level shifters in 180nm Technology

5. Conclusion

Proposed level-up shifters are power efficient and transistor count is reduced to perform the functionality of level shifting. 15T and 14T level shifters are capable of changing sub-threshold voltages to above threshold voltages. Power consumption of proposed 15T level-up shifter and 14T level-up shifter is 54% and 36% respectively less compared to existing level shifter. Power delay product of 15T and14T level-up shifter is 12.7% and 6% respectively less compared to existing 16T level shifter. New configurations of voltage level up shifters shows a significant low power dissipation and little conciliation in delay.

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