*International Journal of Engineering & Technology*, 7(4.16) (2018) 102-105

International Journal of Engineering & Technology

*Website: www.sciencepubco.com/index.php/IJET*

***Research paper***

# Last-Mile Post-Route Power Optimization in Integrated Circuit Conception

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**Abstract**

Power optimization become essential in all the integrated circuit conception phases. During the physical implementation, the requirement is to implement all low power strategies that comes with design from the RTL and logic synthesis. Recently many new techniques for more power reduction were introduced during the physical implementation stage. One of these techniques is post-route power optimization which is performed at the final stage of an integrated circuit conception before the manufacturing. This paper proposes using a model of post-route power optimization technique for a large scope of designs type. Results on complex test-cases shows an important power reduction up to 18% of the total consumed power.

***Keywords***: *Dynamic power, Integrated Circuit conception, leakage power, low power, power optimization, total power.*

## 1. Introduction

The evolution of nanotechnologies allowed to increase the performances and the functionalities of the integrated circuits (ICs) by using advanced technology nodes that offer high integration of transistors in a small area [1]. The ICs are used in a very large number of applications: Mobile, Automotive, Networking, Medical and Internet of thing (IoT) [2]. There are multiple effects in the power optimization such as the increase in device density, the rising clock frequency, the increasing battery life, and reduce the packaging cost. A higher consumed energy involves greater dissipated heat, which requires more efficient cooling system [3]. The ever-increasing complexity of IC has made their power consumption an issue. Thus, it is necessary to take them into account starting from the architecture and through all circuit conception phases [3], [4].

Leakage and dynamic power optimization are known to be runtime expensive. Using the place and route turn-around time shrinking to less than a day, very few design teams are willing to accept waiting several days to get the blocks optimized for power.

To keep having a close control on the power consumption, it is necessary to act at each level of the design implementation. There are several different approaches that can be used to reduce power. The most used low power methods are; supply voltage reduction, clock gating, multiple VT library cells, multi-voltage design, power switching and dynamic voltage and frequency scaling [3]. All of these technologies could be performed during circuit design and/or logic synthesis phases. During the physical implementation, we need to ensure that all the power reduction strategies are well conserved with a back-end annotation [3]. Therefore, more power saving is still needed in modern system-on-chips (SoCs). Although, designers tend to search for new methods to lower the design power. This research focus on the last stage before manufacturing the IC: the physical implementation also called Place and Route (P&R).

At physical design stage, power optimization can target both leakage power and dynamic power, on the two components of the design: components and interconnection. [5] Gives some technics to reduce power on cells elements, [6] focus more on the technology ways to decrease total consumed power in the design, and [7] presents a low power technique that reduce the power on clocks' tree elements and interconnect.

This paper work mainly on the last implementation stage and propose a post-route power optimization flow based on the basic Nitro-SoC leakage and dynamic optimization commands. The objective is to give to the final users a simple flow model that help finding the best receipt for additional power optimization before the IC manufacturing.

To prove the benefit on a real test case, Mentor Graphics' physical design EDA tool Nitro-SoC™ was used on several test-cases made with the advanced technology nodes 28nm, 16nm, and 10nm. The experiment shows an important total power improvement compared to the initial database.

## 2. Materials and Methods

### 2.1. Power Consumption in VLSI Conception

The consumption of an IC at the transistor level can be broken down into two terms: "static consumption" due mainly to parasitic currents, and "dynamic consumption" resulting from the switching activity of circuits [8].

The previous study on power consumption related to the hardware aspect of electronic systems in CMOS technology leads us to the expression:

$$P_{total} = P_{dyn} + P_{leak} \quad (1)$$

The Static Power "$P_{leak}$" consumption is the transistor leakage current that flows whenever power applied on the device, independent of the clock frequency or switching activity. While the dynamic power "$P_{dyn}$" consumption happens during the switching of transistors depends mostly of the clock frequency and the total capacitance of the interconnection. It consists of switching power and internal, distributed on cells and interconnections as follows:

For the cells, the dynamic power model is as follows:

$$P_{dyn} = P_{int} + P_{switch} \quad (2)$$

$$P_{int} = \frac{1}{2}(E_{rise} + E_{fall})TR \quad (3)$$

With: Erise / Efall: Rise and fall energy
TR: Toggle rate, is the number of toggles per time-unit

$$P_{switch} = \frac{1}{2} C V^2 TR \quad (4)$$

With: C is the total wire capacitance
V is the power supply voltage. For the interconnection, the dynamic power model is as follows:

$$P_{dyn} = \frac{1}{2} C V^2 TR \quad (5)$$

## 2.2 Power Optimization Flow Proposal

### 2.2.1 Flow Diagram

The EDA tool Nitro-SoC™ [9]-[11] that performs both leakage and dynamic power optimization was used for this research. Power optimization could be performed either as an integrated stage within the physical implementation full flow or as a separate step after post-route optimization step.
Fig. 1 shows a typical flow diagram for IC conception from System specification until final chip manufacturing, with a scope on the physical implementation stage [12;13;14]. The proposed flow is performed to work after the final "Timing Closure" step, called also "post-route opt" step.
Fig. 2 presents the proposed flow. This flow aims to target different design style with high to low complexity. Also, the flow offers diverse flavors depend on the designer requirement. For example, if the designer needs to spend small time and get a reasonable power reduction or if could wait longer and get further power reduction.
This flow is made to be plugged at the end of post-route optimization, it includes leakage opt, total power opt, legalization, eco route and final timing recovery. Primary metrics are leakage, dynamic and total power and secondary metrics are the timing total negative and hold slacks (TNS, THS). The default of this flow has been tuned for optimum dynamic power reduction on high-activity blocks. This flow helps to optimize the leakage and dynamic power without degrading other metrics, such as timing and routing.

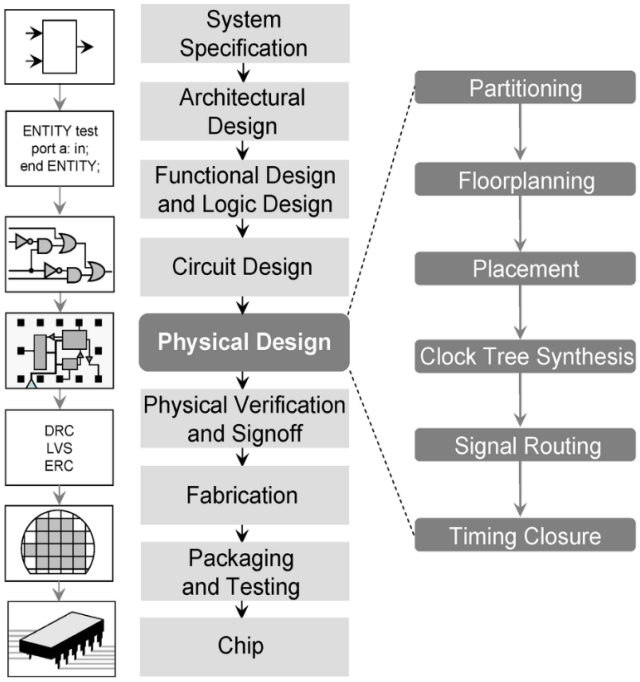


**Fig.1:** Physical design steps within the digital design flow.

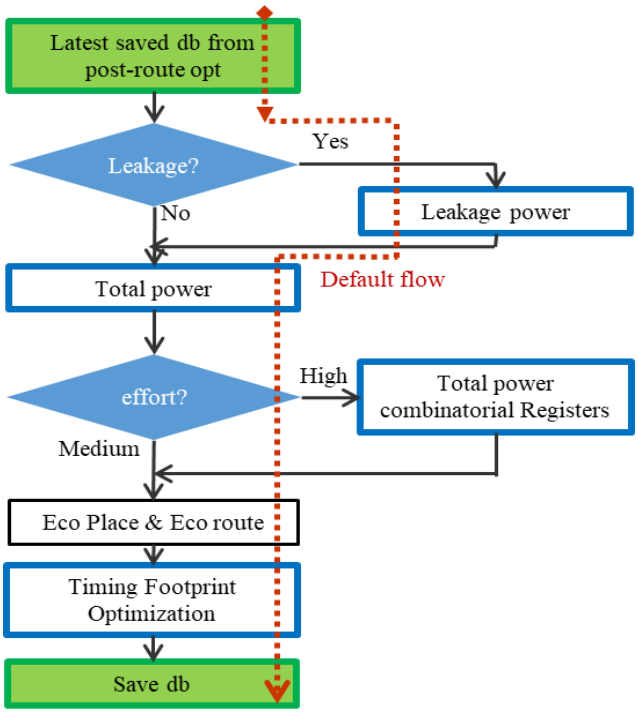


**Fig.2:** Last-mile power optimization flow model.

This research explores how Nitro-SoC achieves 5% to 10% power reduction over the best competition flow with post route optimization, while maintaining an overnight runtime.

### 2.2.2. Flow Description for Best Power Optimization Receipts

When running the optimizer with 'dynamic' objective for a specific target, if the total power increases the optimization will be rejected. On the contrary, when optimizing the leakage, there is no check on the impact on total power. Therefore, the correct sequence is to optimize leakage first then the dynamic power.
Besides, during leakage and dynamic power, to avoid new violations to be created, a costing is done on setup, hold, and max-transition violations. Therefore, it is theoretically possible that the

total negative slack (TNS) degrades by up to 10% during leakage and dynamic power optimization. In case of TNS degradation, it is recommended to run an incremental TNS optimization after leakage and dynamic optimization.
For the 'high' effort, it is advised to run two dynamic power optimizations. Indeed, the cells are visited from endpoint back to start-points during dynamic power opt. When going backward on a path, it can happen that deleting a buffer chain increases the slew at the receiver in a way that the selected lib_cell is no longer the best for dynamic power. One way to get the best solution for the receiver is to revisit the target. This is why the second dynamic power opt helps. A rule of thumb is that the 1st dynamic power opt accounts for 90% of the power reduction, and the 2nd accounts for the remaining 10%.
Finally, the dynamic power optimization is done on data paths, but the user may need to also optimize the registers. The issue with optimizing registers for leakage or dynamic power is to prevent registers moves due to cells overlaps, as it could create large displacements and therefore unwanted timing jumps. The recommendation is to run a separate dynamic power optimization with "white_space" mode (transform only accepted if there is open space in front of target register) and with the property "is_fixed_origin" set at true on registers (to force the optimizer to maintain the cell origin). This way, cells can be sized at their existing location, without creating any cell overlap. This minimizes the impact on clock delay, thus on timing.
In summary, two recipes are provided above: a simple receipt when registers are fixed, then a 2nd receipt when optimizing also registers.

## 3. Results and discussions

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The proposed solution uses the basic Nitro-SoC™ post-route power optimization command within a flow that minimizes total power, by identifying the right trade-off between leakage and dynamic power reduction. Downsizing cells obviously plays a big role for power reduction, but several other efficient techniques complement the sizing and allow further power reduction.
Beyond power optimization, the proposed flow model for post-route power optimization also includes setup, hold and maximum transition optimization, as well as route repair. The usage of both power optimization and timing/route recovery delivers a new post-route database with significantly less power with neutral timing and DRC. (By DRC, we are referring to violations of maximum input slew, maximum load capacitance, and placement/routing design rule checks-DRCs.) The TNS, total hold slack (THS) and DRC count remain the same or better after the power optimization flow.
Table 1 presents results on a 5.87 million instance design including 1.4 million registers. This design is used as test-case for the solution development and validations. The power flow effort was at high with leakage. This design demonstrated that up to 9% power reduction was achieved with neutral timing degradation.

**Table 1:** Results on design#1

| Design #1 | Dynamic (mW) | Leakage (mW) | TNS (ns) | THS (ns) |
|---|---|---|---|---|
| Before Power Opt | 2628.8 | 546.8 | -1198.2 | -3744.0 |
| After Power Opt | 2460.4 | 416.0 | -1040.9 | -1514.1 |

After block design, the power optimization flow model was used on a SoC top design; it has 1.5 million instances, 223 million registers, and 7475 macros. The power distribution is presented in Fig. 3.

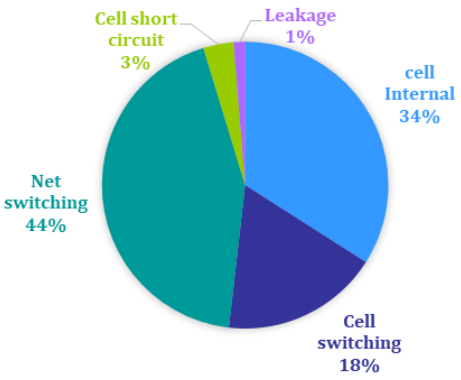


**Fig. 3:** Design #2 Power distribution between all power components

For this SoC top design, 6.52% total power reduction was achieved by applying the best power opt flow receipt. Table 2 shows all detailed power values in addition to the effect on timing and the route closure.

**Table 2:** Results on design#2

| Design#2 | Dynamic (mW) | Leakage (mW) | TNS (ns) | THS (ns) | DRC |
|---|---|---|---|---|---|
| Before Power Opt | 2628.8 | 546.8 | -1198.2 | -3744.0 | 376 |
| After Power Opt | 2460.4 | 416.0 | -1040.9 | -1514.1 | 367 |

Table 3 presents various results of the post route power reduction on several designs with different initial power and timing. By optimizing initial post-route databases, we were able to reduce the power by a further 8.3% on average.
All power optimizations were running for an overnight encompasses the actual power optimization and the timing and routing recovery.

**Table 3:** Summary of the quality of results on several designs

| Designs | | Dynamic (mW) | Leakage (mW) | TNS (ns) | THS (ns) | Power Gain |
|---|---|---|---|---|---|---|
| #3 | Init | 125.44 | 212.59 | -44.12 | -33.14 | **6%** |
| | After | 125.18 | 192.66 | -36.56 | -19.00 | |
| #4 | Init | 82.4 | 0.6 | -900 | -53 | **7.8%** |
| | After | 76.5 | 0.5 | -100 | -53 | |
| #5 | Init | 67.84 | 0.24 | -15 | -48 | **10.5%** |
| | After | 61.38 | 0.23 | -0.636 | -39 | |
| #6 | Init | 283.6 | 3.212 | -2048 | -1.29 | **6%** |
| | After | 266.68 | 3.00 | -2200 | -1.04 | |
| #7 | Init | 376.57 | 1.038 | -284.15 | -23.39 | **2.7%** |
| | After | 366.6 | 0.95 | -359.6 | -19 | |
| #8 | Init | 30.93 | 182.42 | -829.59 | -5.737 | **9%** |
| | After | 29.98 | 163.44 | -744.46 | -6.868 | |
| #9 | Init | 509.27 | 84.22 | -243.2 | -5.714 | **18%** |
| | After | 436.4 | 50.05 | -140.52 | -0.879 | |
| #10 | Init | 129.51 | 0.59 | -6793.6 | -10.46 | **7.5%** |
| | After | 125.71 | 0.52 | -1426.7 | -7.48 | |

"Init" represent value before power opt.
"After" represent value after power opt.
"Power Gain" is the percentage of the result (("Init total power" – "After total power") / "Init total power")

## 4. Conclusion

This paper introduced the post-route power optimization flow, which enables designers to significantly reduce their design leakage and dynamic power with neutral timing and DRC. After using common power minimization techniques such as RTL-level power reduction, multi-bit registers, and automated clock gating, it is still possible to further reduce the total power by 5% to 10% just by optimization of the post-route design. The experiment demonstrates that such results can be achieved in multiple designs.

In summary, the new proposed power optimizer flow model is for design teams to have less consumed power by an IC. Therefore, increasing the battery life time, reducing the size and energy of the devices, reducing the cost of packaging, or implementing more features in the chip with same package can be obtained at the cost of only an overnight last-mile post-route power optimization step at the end of the existing place and route flow.

## Acknowledgement

This research was supported by Mentor Graphics Corporation. We thank Dr. Hazem El Tahawy (Mentor Graphics, MENA Region Managing Director) for initiating and supporting this work.

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