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Research paper

Asymmetric Cascaded Inverter for Photovoltaic Applications Based on Carrier Redistribution Modulation Strategies

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Abstract

Asymmetric Cascaded Multilevel inverter (ACMLI) for photovoltaic (PV) generating system is presented in this paper. The proposed asymmetrical arrangements of seven-level cascaded inverters have been compared with advanced modulation strategies, in order to find an optimum arrangement with lower harmonic distortion and optimized output voltage quality and which makes use of minimum number of switches to get more levels. It also reduces the complexity, number of sources, cost and losses. Modulating control techniques can be modified in two ways, namely Modified Carrier (MC) and Modified Reference (MR). This paper proposes modifies space vector based pulse width modulation (PWM) using various U-type Carrier Redistribution Methods (CRM) which utilize the control freedom degree (CFD) of vertical offsets among carriers and also compared with existing sinusoidal PWM technique for single-phase seven level ACMLI using MATLAB/Simulink.

Keywords: *Asymmetric cascaded inverter; Boost converter;THD;PV Model; PWM Techniques*

1. Introduction

Electrical energy is the highly consumed energy in the global energy system. The generation of electrical energy by conventional energy sources is not able to meet the growing load demand. Therefore, the interest on alternative energy sources is being increased. The available renewable energy sources (RES) are solar, fuel cell and wind. Solar energy is most readily available nonpolluting and maintenance free source of energy. PV systems are used to make best use of solar energy by maximizing the output by adjusting the panel in such a direction so as to receive the maximum solar irradiance or by electrically tracking the maximum power under changing condition of temperature and insolation. Variation of Irradiance and Temperature will vary the overall performance of PV cell [1].

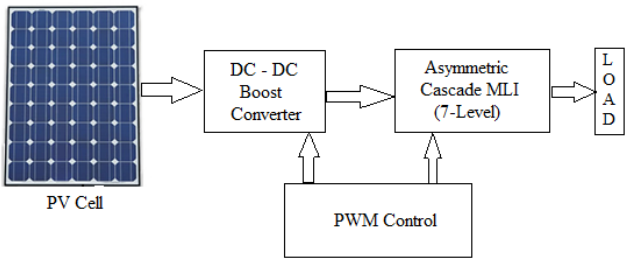

Fig. 1(a): Block diagram of PV fed ACMLI

Recently, several Multilevel Inverter (MLI) topologies have been reported in the literature for PV systems [3]. The drawbacks of existing MLIs, uses more number of switches and DC sources by increasing the number of levels. But this paper presents an ACMLI using two unequal DC sources to generate seven-level output [2]. The block diagram and configuration of proposed single-phase seven level ACMLI fed PV cell is shown in Fig. 1(a) and 1(b) respectively. The proposed ACMLI can have the enhance performance by implementing PWM techniques. This paper also proposes three PWM methods based on various U-type CRMs using modified space vector reference and also compares with the existing sinusoidal reference for ACMLI to generate seven level output [4].

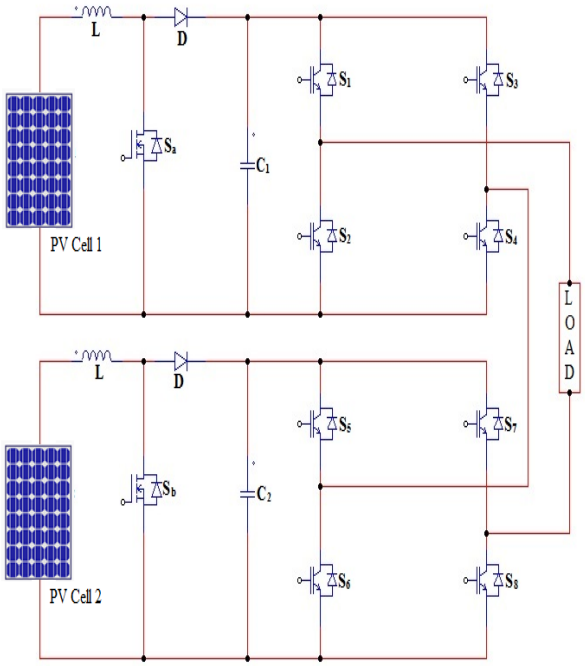

Fig. 1(b): Configuration of PV fed single – phase 7 level ACMLI

2. Solar Simple PV Model

The electrical equivalent circuit of a solar cell is shown in Fig.2, which is having a diode in parallel with the [6]. The output of the current source is directly proportional to the light falling on the cell. The diode type determines the V-I characteristics of the solar cell.

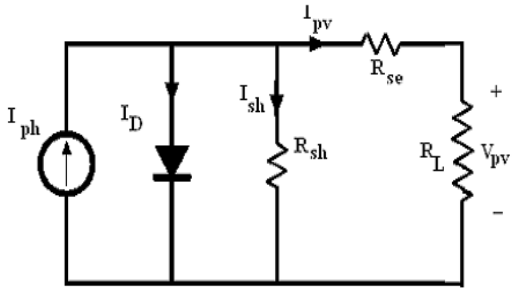

Fig. 2: Electrical Equivalent Circuit of Solar Cell

$$I_{PV} = I_L - I_D = I_L - I_o\left[\exp\left(\frac{V_{PV}+I_{PV}R_S}{\propto}\right)-1\right] \quad (1)$$

Where,

$$I_L = \frac{G}{G_{ref}}\left[I_{ref} + \mu_{Isc}(T_c - T_{cref})\right] \quad (2)$$

$$I_L = I_{oref}\left[\frac{T_{cref}+273}{T_c+273}\right]^3 exp\left(\frac{qe_{gap}}{N_s \propto_{ref}}\left[1-\frac{T_{cref}+273}{T_c+273}\right]\right) \quad (3)$$

V_{pv} and I_{pv} : Cell output voltage and current; Io= Cell saturation current at T_r; T_{ref} = 273° K reference temperature; I_L= Light generated current; T_c = Cell Temperature; e_{gap} = Band gap of the material; q = Charge of an electron; R_s = Series Resistance; μ_{Isc} = Short-circuit current temperature coefficient; α = Timing completion factor of thermal voltage.

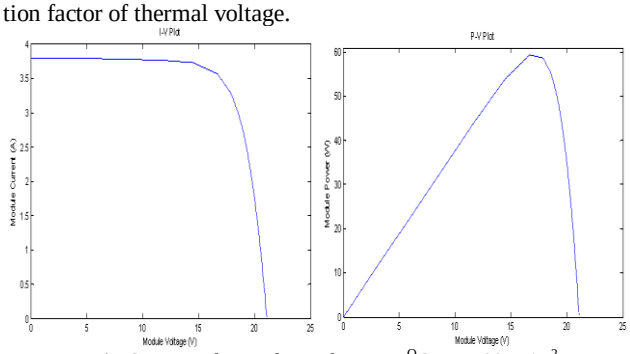

Fig. 3: I-V and P-V plot with T = 25 °C, I = 400 W/m²

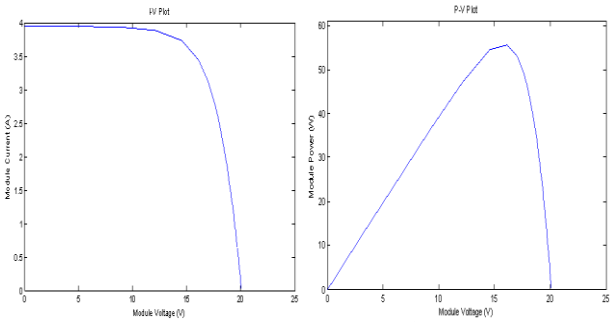

Fig. 4: I-V and P-V plot with T = 100 °C, I = 400 W/m²

I-V and P-V output characteristic curve of PV-module for 400 W/m² irradiation with a 25°C and 100°Ccell temperatures respectively as shown in Fig. 3.and Fig. 4. Similarly, Fig.4 and Fig. 5 characteristic curve of PV-module for 100°Ccell temperature with 400 W/m² and 800 W/m² irradiations respectively [6]. The output of the PV is integrated with the Boost Converter (BC) as it produces low-voltage output.

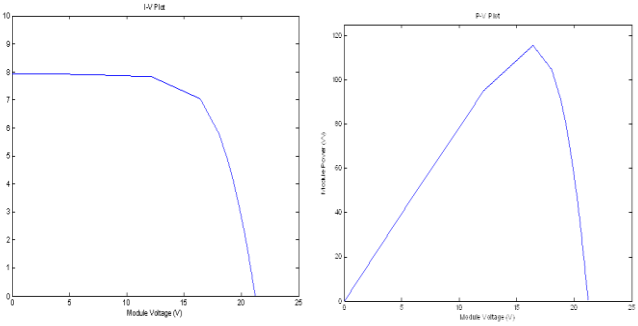

Fig. 5: I-V and P-V plot with T = 100 °C, I = 800 W/m²

3. DC-DC Boost Converter

The PV cell insists for boost operation of voltage using DC-DC converter. BC boost the input voltage which results in greater output voltage based on its duty ratio. BC using a power MOSFET is shown in Fig.6 [8].

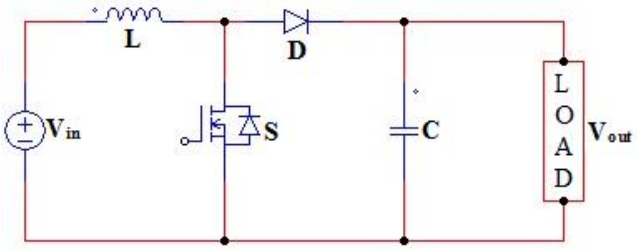

Fig.6: DC – DC Boost Converter

The BC operates in two modes, Mode 1 and Mode 2. Mode 1 begins when power MOSFET 'S' is switched ON at time t=0. The input current rises and flows through inductor 'L' and 'S'. Mode 2 begins when power MOSFET 'S' is switched OFF at time t=t_1. The input current flows through 'L', 'C', diode 'D' and load.
The outputs of BCs are 50V and 100V respectively which are fed to asymmetrical multilevel inverter. Voltage obtained from PV module is 21.73V, thus using two boost converters voltage boosted up to the required level. The relation between output voltage and duty cycle (D) of a pulse applied to power MOSFET 'S' is given by,

$$V_{out} = \frac{V_{in}}{1-D} \quad (4)$$

Required outputs from BCs are 50V and 100V thus using above equation duty cycle is obtained as 0.58 and 0.79 respectively. The output wave forms of boost converter are shown in Fig. 7 & 8.

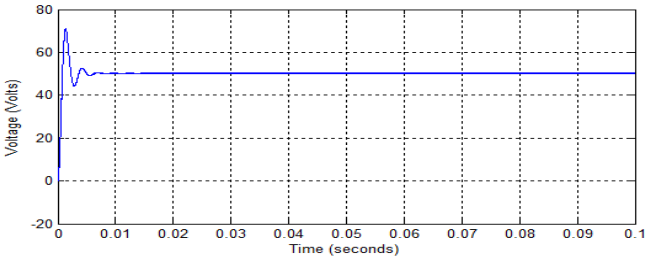

Fig. 7: Output voltage of the BC1 with a D = 0.58

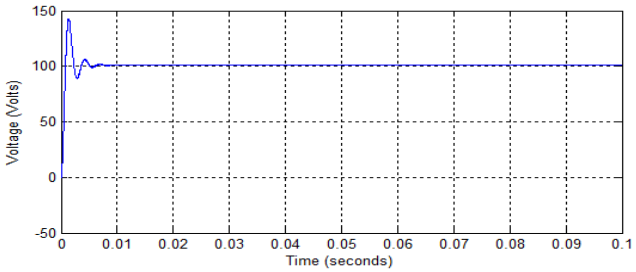

Fig. 8: Output voltage of the BC2 with a D = 0.79

4. Asymmetric Cascaded Multilevel Inverter (ACMLI)

From the literature, it is observed that for high voltage applications, more number of DC sources are required by increasing the number of voltage levels, therefore this could lead to unbalance voltages among the DC sources [1, 2]. In order to reduce the number of DC sources for the existing MLIs, this paper focused on an asymmetric MLI. The proposed ACMLI consists of only two DC sources and eight power switches to generate seven level output which is shown in Fig.9. It consists of two blocks namely, block 1 and block 2. Block 1 of ACMLI generates the output levels - V_{dc}, 0, + V_{dc}. Similarly, block 2 generates the - $0.5V_{dc}$, 0, $0.5V_{dc}$. Therefore, the total output voltages of the ACMLI have the values of -1.5 V_{dc}, -V_{dc}, -0.5 V_{dc}, 0, 0.5 V_{dc}, V_{dc} and 1.5 V_{dc}.

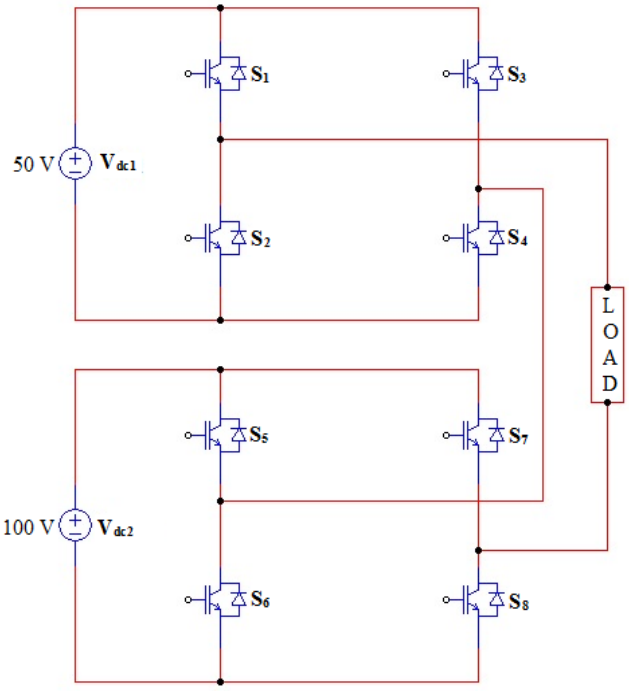

Fig. 9: Single-phase seven level ACMLI

The overall output voltage of a n-level conventional MLI is given by

$$V_o = V_{dc1} + V_{dc2} \ldots\ldots + V_{dcn} \quad (5)$$

The number of output phase voltage levels 'N_{level}' for a conventional MLI is given by

$$N_{level} = 2n + 1 \quad (6)$$

The maximum output voltage (Vmax) for n-level cascaded MLI is

$$V_{max} = n\, V_{dc} \quad (7)$$

The number of output phase voltage levels 'N_{level}' for a proposed ACMLI is given by

$$N_{level} = 2(\sum_{i=1}^{n} n) + 1 = n^2 + n + 1 \quad (8)$$

The maximum output voltage (Vmax) for n-level proposed ACMLI is given by

$$V_{max} = V_{dc}(1 + 2 \ldots\ldots + n) = V_{dc} \sum_{i=1}^{n} i = V_{dc} \frac{n(n+1)}{2} \quad (9)$$

Comparing (6) to (9), it can be seen that proposed ACMLI can generate more voltage levels and high output voltage when compared with n-level cascaded MLI with the same number of dc sources.

Table 1 gives the component count for symmetric and ACMLIs. Form the table 1; it is clear that the proposed ACMLI requires less number of switches and less number of DC sources by increasing the number of levels.

Table 1: Comparison of cascaded multilevel inverters

	Symmetrical MLI	ACMLI
Number of DC sources	n	n
Number of switches	4n	2^{n+1}
Number of voltage levels	2 n + 1	$2^{n+1} - 1$
Maximum output voltage	n	$2^n - 1$

Table 2: Input DC levels combinations and their absence/presence in proposed ACMLI

Number of DC sources	Source description	Voltage levels	Number of combinations of DC input voltage levels	Number of possibilities offered by the ACMLI
1	V_{dc}	0 ± V_{dc}	3	3
2	V_{dc1}, V_{dc2}	0 ± V_{dc1} ± V_{dc2} ± (V_{dc1} - ± V_{dc2}) ± (V_{dc1} + ± V_{dc2})	9	7

Table 2. Gives the number of combinations of DC input voltage levels and their absence/presence in proposed ACMLI. It can be seen that there are some voltage levels which are skipped that is, no switching combination exists.

5. Modulation Control Techniques for MLI

Modulation control techniques can generally be classified into Modified Reference (MR) and Modified Carrier (MC) [5].

5.1. Modified Reference (MR)

MR signals can be classified into Sinusoidal and Modified Space Vector PWM references. These references are broadly studied and compared with the performance parameters for ACMLI to generate seven levels [7].

5.1.1 SPWM

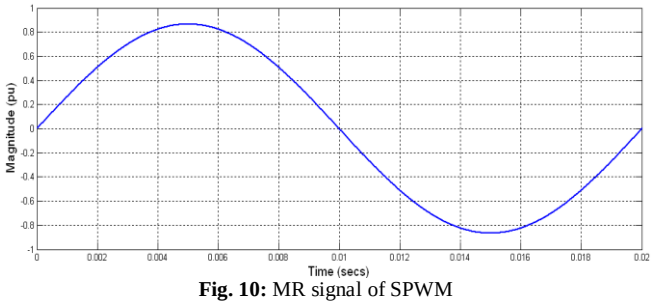

Fig. 10: MR signal of SPWM

SPWM is the most widely accepted PWM technique, where a U-type wave is compared with a sinewave reference known as the MC, shown in Fig. 10.

5.1.2 MSVPWM

To achieve maximum amplitude of the fundamental phase voltage, a common mode voltage, '$V_{offset1}$' is added to the sinusoidal MR signal, where the magnitude of $V_{offset1}$ is given by

$$V_{offset1} = \frac{-(V_L+V_H)}{2} \quad (10)$$

Where, V_L is the minimum magnitude and V_H is the maximum magnitude of the three sampled reference phase voltages. Fig. 11 shows the MR signal of modified space vector [9].

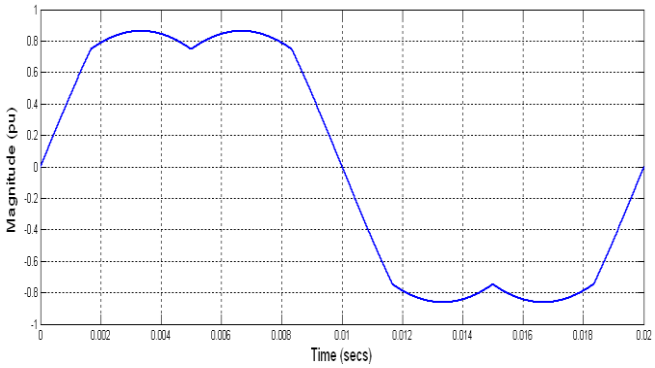

Fig. 11: MR signal of SVPWM

5.2 MC PWM Techniques

This paper also presents multi-level CRM based on U-type [5], [7]. It can be a useful solution to generate the pulses for the ACMLI topology.

5.2.1 Alterative Phase Opposition Disposition (APOD)

For an m-level phase waveform, APOD requires (m – 1) carrier waveforms which are to be displaced from each other by 180^0 phase alternately as shown in Fig. 12 and Fig.13 for various MR based signals.

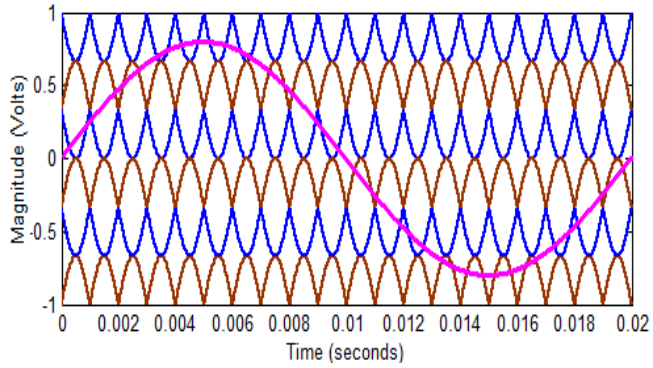

Fig.12: SPWM scheme by U-type carrier for a seven-level inverter using APOD

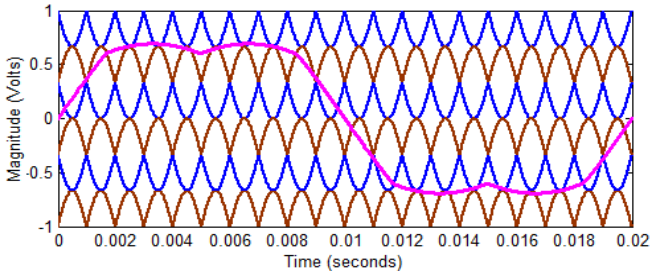

Fig.13: MSVPWM scheme by U-type carrier for a seven-level inverter using APOD

5.2.2 Phase Opposition Disposition (POD)

For an m-level phase waveform, POD requires (m – 1) carrier waveforms which are to be displaced by 180^0 phase shift between the above and below zero respectively as shown in Fig. 14 and Fig.15 for various MR based signals.

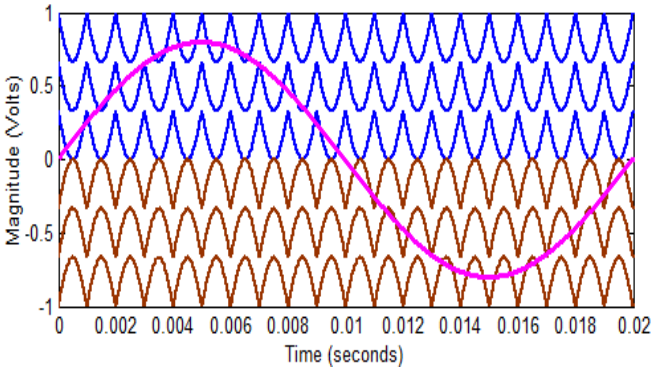

Fig.14: SPWM scheme by U-type carrier for a seven-level inverter using POD

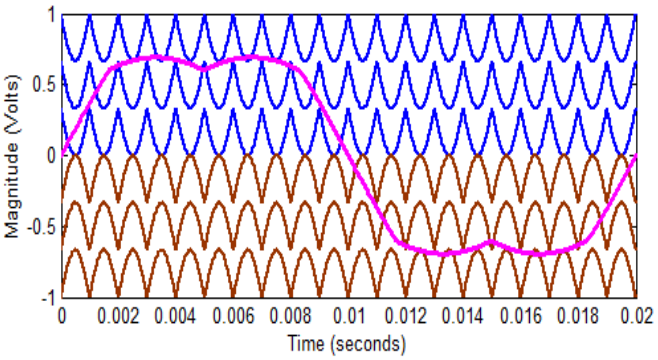

Fig.15: MSVPWM scheme by U-type carrier for a seven-level inverter using POD

5.2.3 Phase Disposition (PD)

For an m-level phase waveform, PD requires (m – 1) carrier waveforms which are in the same phase as shown in Fig. 16 and Fig.17 for various MR based signals.

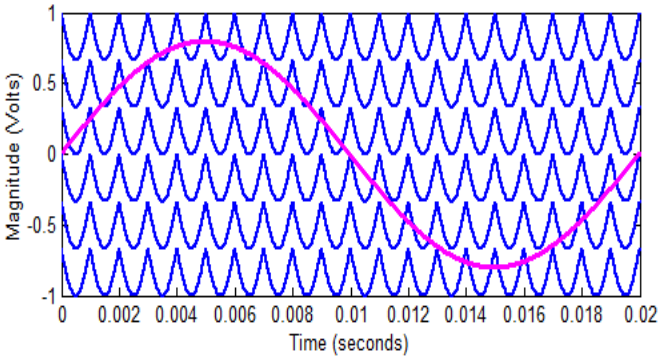

Fig.16: SPWM scheme by U-type carrier for a seven-level inverter using PD

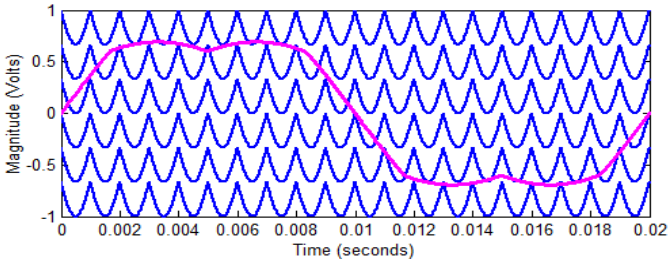

Fig.17: MSVPWM scheme by U-type carrier for a seven-level inverter using PD

6. Simulation Results

The circuit simulation was carried out to verify the operating principles of the proposed single – phase ACMLI for seven level using MR based signals with U-type carriers. In this simulation, input voltage sources are taken as V_{dc1} =50 V and V_{dc2} = 100 V and frequencies of carrier and reference waveforms are taken as 5 kHz and 50 Hz, respectively.

6.1 Seven Level ACMLI for 1–ϕ:

6.1.1 SPWM

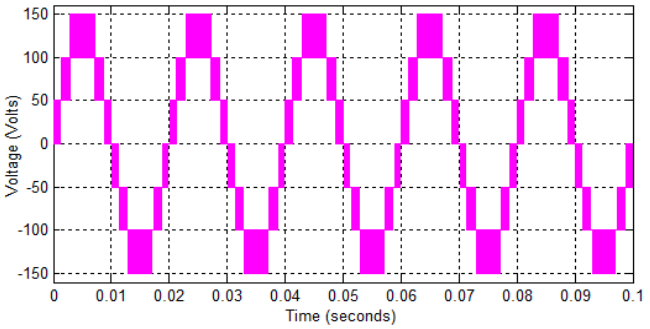

Fig.18: ACMLI Output voltage for 1–ϕ seven level using SPWM for m_a = 0.8

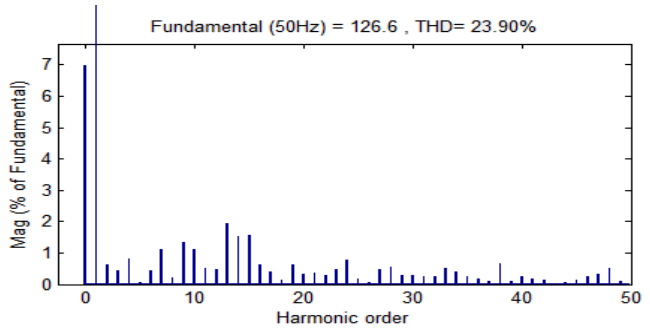

Fig.19: ACMLI Harmonic spectrum for 1–ϕ seven level using APOD for m_a = 0.8

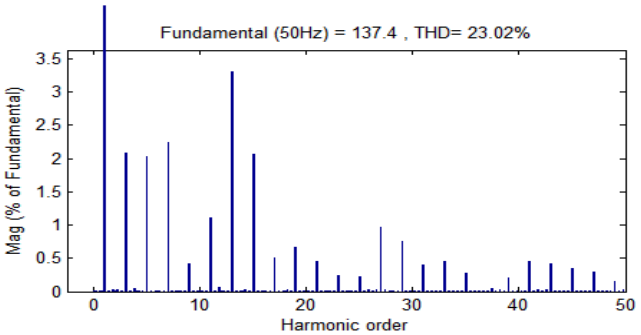

Fig.20: ACMLI Harmonic spectrum for 1–ϕ seven level using POD for m_a = 0.8

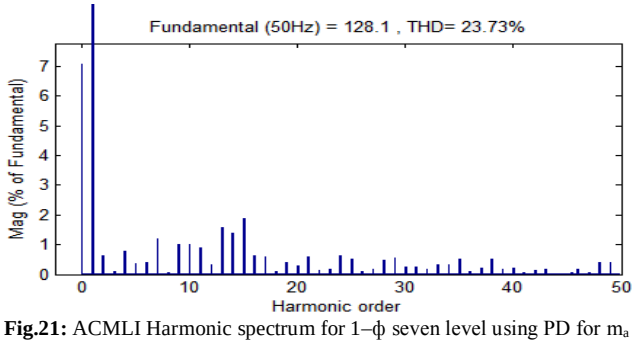

Fig.21: ACMLI Harmonic spectrum for 1–ϕ seven level using PD for m_a = 0.8

6.1.2 Modified SVPWM

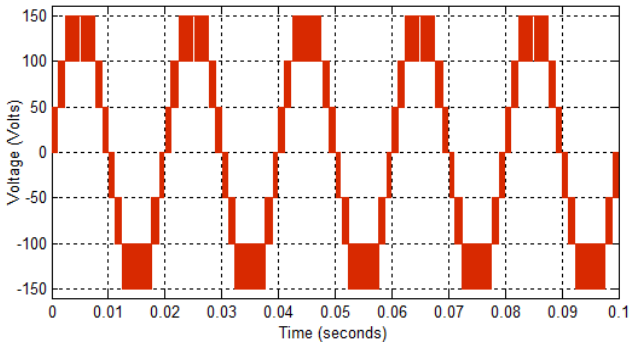

Fig.22: ACMLI Output voltage for 1–ϕ seven level using SPWM for m_a = 0.8

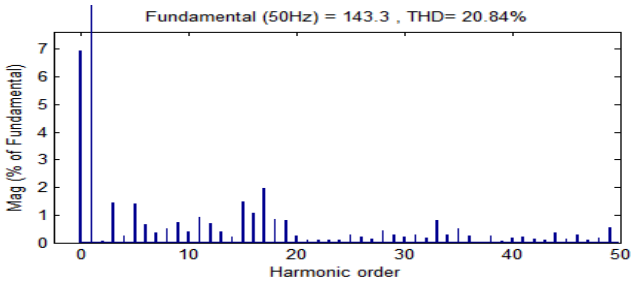

Fig.23: ACMLI Harmonic spectrum for 1–ϕ seven level using APOD for m_a = 0.8

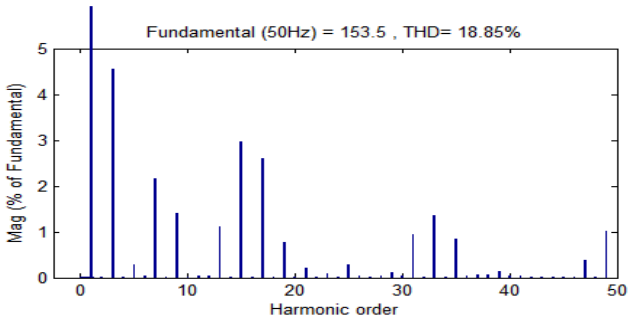

Fig.24: ACMLI Harmonic spectrum for 1–ϕ seven level using POD for m_a = 0.8

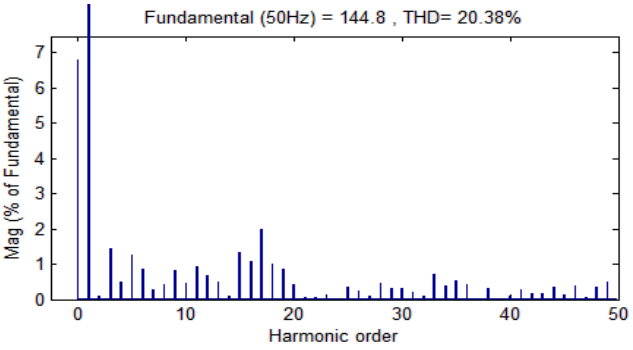

Fig.25: ACMLI Harmonic spectrum for 1–ϕ seven level using PD for m_a = 0.8

The simulated output voltages of the ACMLI for 1–ϕ seven level using various MR based reference signals i.e., SPWM and Modified SVPWM based on U-type carriers its corresponding FFT analysis are shown in above figures for 0.8 modulation index (m_a). These waveforms confirm the principle of operation of 7-level Asymmetric Cascade H-Bridge inverter using SPWM and modified SVPWM fed resistive load.

7. Comparison of Results

Table 3:% THD of ACMLI for 1–ϕ seven level using MR based PWM techniques with U-type carriers

Modulation Index (m_a)	**SPWM**			**Modified SVPWM**		
	APOD	**POD**	**PD**	**APOD**	**POD**	**PD**
0.85	23.90	23.02	23.73	20.84	18.85	20.38
0.8	25.01	24.19	24.77	22.53	20.89	22.26
0.75	25.87	25.34	25.69	23.72	22.68	23.54
0.7	27.39	26.02	27.02	24.89	24.04	24.62

Table 4: Fundamental Output Voltage (Vrms) for various MR based PWM Techniques for 1–ϕ seven level ACMLI

Modulation Index (m_a)	SPWM			Modified SVPWM		
	APOD	POD	PD	APOD	POD	PD
0.85	126.6	137.4	128.1	143.3	153.5	144.8
0.8	119.7	130	121	135.7	146.6	137.1
0.75	112.1	122.1	113.8	128.3	139.2	129.7
0.7	103.3	112.9	105.2	120.1	130.06	121.7

The ACMLI is simulated for various MR based PWM techniques based on U-type carriers for different modulation indices. Table 1 and Table 2 shows the simulation results with various modulation indices of various MR based PWM techniques for 1–ϕ seven level ACMLI. From Table.2 it is observed that the RMS value is found to increase with the increase in the modulation index in steps of 0.5 and corresponding THD is decreases which are tabulated in Table.1. It is concluded that MR based modified SVPWM with U-type POD carrier has given better THD and RMS output voltage when compared with sinusoidal reference.

8. Conclusion

This paper presented a single phase seven level ACMLI for PV application. The proposed seven level ACMLI has several advantages for the use of a standalone PV system. Finally the proposed multilevel inverter topology is providing separate DC supply for each module, which is a good option for PV solar power generation system. It is easy to build and it has more redundancy than any other topologies. Presented topology has high efficiency. If the inverter is used in rural areas for PV systems then the proposed ACMLI will be a good alternative to grid supply in rural industries.

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