

Scalar based Common Mode Voltage Reduction PWM Techniques for Dual Inverter Fed Open End Winding Five-Phase Induction Motor Drives

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Abstract

This paper presents a simplified approach for common mode voltage (CMV) reduction for the dual inverter fed open end winding five-phase induction motor drives. This paper presents the simplified PWM techniques for three-level and four-level topologies of open end winding five-phase induction motor drive. In this method reference voltage signals are synthesized by injecting the zero sequence signals. Through these proposed methods, a reduction of 66.6% in three-level topology and 40% in four-level topology is observed in peak to peak voltage of common mode voltage when compared to conventional space vector PWM technique. Number of levels in common mode voltage is reduced from 5 levels to 2 levels in three-level topology and 6 levels to 3 levels in four-level topology when compared to a conventional space vector PWM technique. Simulation studies are performed to validate the proposed simplified methods.

Keywords: common mode voltage, open end winding, Multi-phase machines, scalar PWM, dual inverter operation.

1. Introduction

Multi-phase machines have gaining more importance since they have better improvements in terms of reliability; torque density; torque pulsations; power handling capability per phase; noise characteristics reduced stator copper losses; and overall efficiency compared to a standard three-phase machine drives. Recent industrial applications of multi-phase machines have been found in literatures which include electric vehicles propulsion [2], ship propulsion [3], low torque pulsation applications [4] and series connected motor drives with single inverter supply [5-6]. Multi-level inverters generate common mode voltage (CMV) at high frequency. Effects of these voltages have major disadvantages which are described as below:

1. It affects machine bearings and insulation
2. It causes electromagnetic interferences and damages the electronic devices such as digital controllers and sensing devices etc
3. Reduces bearing life.
4. Mechanical failure of the motor.

Mario J. Durán, Joel Prieto has proposed Space vector PWM (SVPWM) techniques for a two-level inverter fed five phase induction motor. Some of the research publications[1-2] proposed open ended stator with two inverters feeding on both sides of the five-phase induction motor drives. In this study different PWM techniques have been proposed ; the space vector PWM technique with eliminating zero vectors has reduced the CMV by 40% and avoiding both zero and medium vectors has reduced the CMV by 80% in [3]. And a model predictive control (MPC) methods for CMV reduction has also presented in [4]. CMV elimination using

a common DC source has been presented in [5] and also addressed zero sequence current that flow in inverters. Phase shifted SVPWM for a two-level inverter fed five phase induction motor was proposed in [6] which reduces the normalized RMS value of CMV by about 55%, 100%, 59% at full modulation depth to about 80%, 100%, 100% at zero modulation depth for the five-phase, symmetrical, and asymmetrical six-phase inverters, respectively. A generalized minimum CMV using two different leg distributions: double-sided and central distribution switching strategy for a two-level N-phase VSI is proposed in [7]. A carrier based SVPWM scheme by selecting and identifying the decagons of vectors which produces zero CMV is proposed in [7]. Even though this scheme completely eliminates the CMV but harmonics are more in output phase voltages and currents; quite complicated and time consuming. Carrier based PWM schemes for CMV elimination for a basic two-level inverter fed five-phase motor is proposed in [8], which adopted applying opposite carriers to some specified phase. The CMV reduction using phase shifted carriers is discussed in [9]. CMV reduction in over modulation regions using SVPWM techniques has been discussed in [10]. Dual matrix converter feeding a open end five phase induction motor and its CMV reduction using SVPWM is discussed in [11-12]

2. Three-Level and Four-Level Topology of Dual Inverter Circuit Configuration of Five-Phase Induction Motor

In this configuration the open ended stator of five-phase induction motor is connected with two inverters with equal and unequal DC voltages forms a three-level and four-level topologies of dual

inverter fed open end winding (OEW) five-phase induction motor drives. Inverter I and inverter II are supplied with DC link voltage of Vdc1 and Vdc2. Inverter I and inverter ii when supplied with equal dc voltage of Vdc/2 a three-level topology. Where as if Inverter I is supplied with 2Vdc/3 and Inverter II with Vdc/3 forms a four-level topology is obtained. Here $V_{a0}, V_{b0}, V_{c0}, V_{d0}, V_{e0}$ are the pole voltages of Inverter I and $V_{a'o'}, V_{b'o'}, V_{c'o'}, V_{d'o'}, V_{e'o'}$ are the pole voltages of Inverter II. $V_{aa'}, V_{bb'}, V_{cc'}, V_{dd'}, V_{ee'}$ are the effective phase voltages and $V_{ab}, V_{bc}, V_{cd}, V_{de}, V_{ea}$ are the line voltages. N1 and N2 indicates the neutrals of inverter I and II. The common mode voltage (CMV) is the potential V_{00} which can be evaluated as

$$V_{CMV} = \frac{(v_{ao}-v_{a'o'})+(v_{bo}-v_{b'o'})+(v_{co}-v_{c'o'})+(v_{do}-v_{d'o'})+(v_{eo}-v_{e'o'})}{5} \quad (1)$$

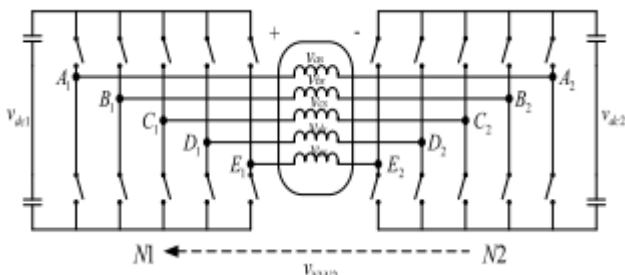


Fig1: Dual inverter topology of a five-phase open-end winding motor drives

Table I below shows four-level pole voltage by utilizing the switching patterns of Inverter I and inverter-II.

Table I: Effective Pole Voltage Calculation

ON STATE SWITCHES IN INVERTER I	POLE VOLTAGE OF INVERTER-I	ON STATE SWITCHES IN INVERTER-II	POLE VOLTAGE OF INVERTER-II	EFFECTIVE POLE VOLTAGE
S ₁₂ OR S ₁₄ OR S ₁₆ OR S ₁₈ OR S ₁₀	0	S ₂₁ OR S ₂₃ OR S ₂₅ OR S ₂₇ OR S ₂₉	+V _{dc} /3	-V _{dc} /3
S ₁₂ OR S ₁₄ OR S ₁₆ OR S ₁₈ OR S ₁₀	0	S ₂₂ OR S ₂₄ OR S ₂₆ OR S ₂₈ OR S ₂₀	0	0
S ₁₁ OR S ₁₃ OR S ₁₅ OR S ₁₇ OR S ₁₉	+2V _{dc} /3	S ₂₁ OR S ₂₃ OR S ₂₅ OR S ₂₇ OR S ₂₉	+V _{dc} /3	+V _{dc} /3
S ₁₁ OR S ₁₃ OR S ₁₅ OR S ₁₇ OR S ₁₉	+2V _{dc} /3	S ₂₂ OR S ₂₄ OR S ₂₆ OR S ₂₈ OR S ₂₀	0	+2V _{dc} /3

Scalar based PWM techniques are quite simple in implementation since it reduces complexity involved in conventional space vector approach. The proposed method has the freedom of selecting the zero sequence signals. In general the five reference signals can be obtained using the equation 1.

$$V_{in} = V_m \cos(\omega t - \frac{2\pi i}{5}) \quad \text{Where } i=a,b,c,d,e \quad (2)$$

The zero sequence signals can be evaluated as $V_{zs} = \frac{V_{dc}}{2} * (2a_0 - 1) - a_0 V_{max} + (a_0 - 1) V_{min}$
 $V_{max} = \text{Max}(V_{in}) \text{ and } V_{min} = \text{Min}(V_{in})$

$$V_{in}^* = V_{in} + V_{zs} \quad (3)$$

The Five reference signals are added with zero sequence signal Vzs to obtain to modified reference signals. These modulating

signals obtained are compared with high frequency carrier signals and the intersection points thus obtain defines the gating pulses for the two inverters. The constant a0 varies between 0 and 1, produces different continuous and discontinuous modulating signals. For a0 =0.5 continuous modulating signals can be obtained. Three carriers are chosen with magnitudes 0 to 1/3; 1/3 to 2/3; 2/3 to 1 to obtain the four-level dual inverter topology. Three different carrier triangular signals can be generated by using XOR logical gates as shown in Fig 4.

The generated gating signals of Inverter I and II are shown in Fig 3 for conventional continuous modulating signal. For explanation purpose the pattern is differentiated into 4 different regions. Continuous modulating signals in region 1, modulating signal interacts with three carrier triangles (0 to 1/3; 1/3 to 2/3 and 2/3 to 1). Carrier signal Vt3 then Inverter I is clamped to -ve DC-bus which means upper switches of Inverter I are in OFF state and Inverter II are in ON state. In region 2, modulating signal magnitudes are greater than the carrier triangular signals Vt1 or Vt2 but less than Vt3 then lower switches of inverter 1 is in ON state and inverter 2 are in OFF state. A quite opposite phenomenon takes for the regions 3 and 4 as in 1 and 2 respectively.

3. Scalar based Common Mode Voltage Reduction Pwm Algorithm:

The proposed PWM algorithms are based on generation of commanded reference signals and these signals are compared with reference signals to determine the slope and location. These commanded reference signals can be generated by using (2). The proposed four level topology can able to generate 4-level calculated effective phase voltages the entire region is divided into three regions (R1, R2 and R3) and hence three sets of level shifting triangular signals are required. Whereas for symmetrical topology (Equal DC Link Voltage for the two inverters) only two regions (Region R1 with Duty cycle <0.5 and Region R2 with duty cycle ≥0.5) are enough. These regions are divided based on the duty cycle of the reference signal as in Table II.

$$V_{it} = V \max \cos(\omega t - \frac{2(r-1)\pi}{5}) \quad (4)$$

Where i=a,b,c,d,e and r=1,2,3,4,5.

Table II: Triangular Pattern Region Identification for three-Level and Four-Level topologies

FOUR-LEVEL TOPOLOGY		THREE-LEVEL TOPOLOGY	
REGION	DUTY CYCLE OF THE REFERENCE SIGNALS	REGION	DUTY CYCLE OF THE REFERENCE SIGNALS
R1	0 TO 1/3	R1	0 TO 1/2
R2	1/3 TO 2/3	R2	1/2 TO 1
R3	2/3 TO 1	-----NO THIRD REGION -----	

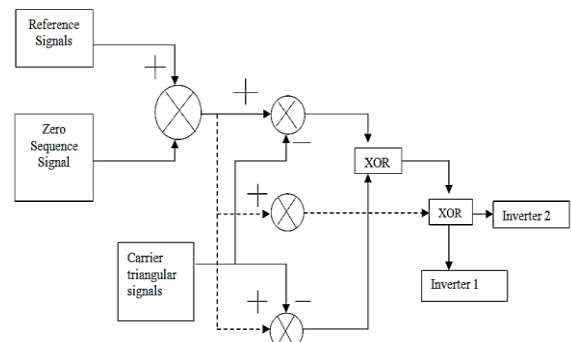


Fig 2: Block diagram showing gate pulse generation for four levels OEW drive.

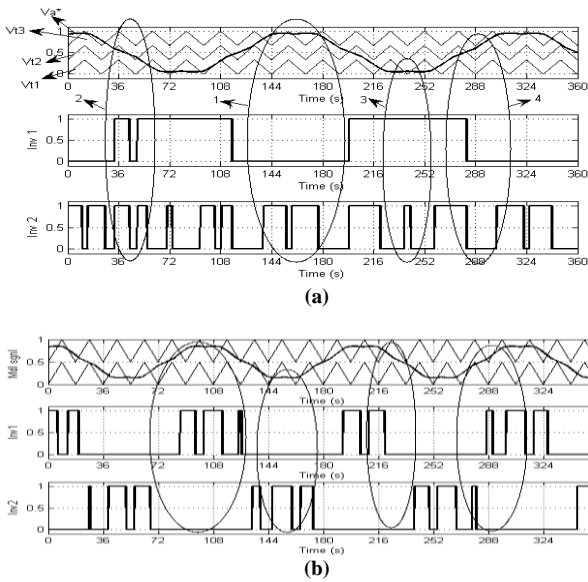


Fig 3: Pulse patterns of Inverter I and Inverter II for conventional continuous PWM technique for $m=0.65$ a) four-level topology b) three-level topology of dual inverter fed five-phase induction motor.

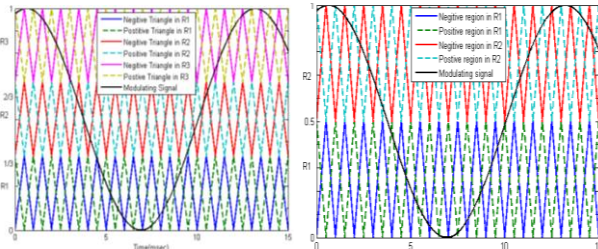


Fig 4: Triangular pattern identification for a) Four-level in three different regions (R1, R2 and R3) b) Three-level in two different regions (R1 and R2)

Fig 4 indicates the triangular pattern identification in three different regions as evaluated in Table II. For proper visualization purpose the switching frequency is selected as 100 Hz in Fig. 6. In each region one positive triangle and one negative triangle signal are presented which cuts the reference signal as per the slope of commanded reference signal in (4). The slope where $r=1,2,3,4,5$ can be cut with the Triangular selection according to the Table III. If the slope is positive i.e. $+VIT$ then positive triangle is selected for comparison of the modulating signal in the three regions (R1, R2 and R3). If the slope is negative i.e. $-VIT$ then a Negative triangle is selected for comparison. The point of interaction with the total of 6 triangle signals generates control signals for the gate terminals of inverter I and II. Different PWM techniques can be implemented for common mode reduction by identifying different reference signals, zero sequence signals and triangular signals. Four PWM (PWM1, PWM2, PWM3 and NSCPWM) techniques have been selected for CMV reduction are tabulated in Table IV. And comparison is made among these four techniques and the best method is proposed.

Table III: Triangle selection using slope of the commanded modulating signal.

REGION	TRIANGLE SELECTION
$0 < \theta \leq 2\pi/5$	+VIT
$2\pi/5 < \theta \leq 3\pi/5$	+VIT
$3\pi/5 < \theta \leq 4\pi/5$	+VIT
$4\pi/5 < \theta \leq \pi$	+VIT
$\pi < \theta \leq 6\pi/5$	-VIT
$6\pi/5 < \theta \leq 7\pi/5$	-VIT
$7\pi/5 < \theta \leq 8\pi/5$	-VIT
$8\pi/5 < \theta \leq 9\pi/5$	-VIT
$9\pi/5 < \theta \leq 2\pi$	-VIT

Table IV: proposed PWM algorithm

PWM TECHNIQUE	REFERENCE SIGNAL AND ZERO SEQUENCE SIGNAL	A0 VALUE	Commanded Reference Signals
PWM1	$V_{it} = V \max \cos\left(\omega t - \frac{2(r-1)\pi}{5}\right)$ WHERE I=A,B,C,D,E AND R=1,2,3,4,5.	1/2	$V_{it} = V \max \cos\left(\omega t - \frac{2(r-1)\pi}{5}\right)$ WHERE I=A,B,C,D,E AND R=1,2,3,4,5.
PWM2	$V_{zs} = \frac{V_{dc}}{2} * (2a_0 - 1) - a_0 V_{max} + (a_0 - 1) V_{min}$	1/2	$V_{it} = V \max \cos\left(\omega t - \frac{2(r-1)\pi}{5} + 2\pi/5\right)$ WHERE I=A,B,C,D,E AND R=1,2,3,4,5.
PWM3		1/2	$V_{it} = V \max \cos\left(\omega t - \frac{2(r-1)\pi}{5} - 2\pi/5\right)$ WHERE I=A,B,C,D,E AND R=1,2,3,4,5.
PWM4		$V_{MIN} + V_{MAX} < 0 \text{ THEN } a_0 = 0$ $V_{MIN} + V_{MAX} \geq 0 \text{ THEN } a_0 = 1$	$V_{it} = V \max \cos\left(\omega t - \frac{2(r-1)\pi}{5}\right)$ WHERE I=A,B,C,D,E AND R=1,2,3,4,5.

In PWM1, PWM2 and PWM3 the modulating signal is continuous and zero states are not employed and hence the CMV generated with zero state vectors will be eliminated. Only the active vectors that both inverters map will generate the CMV. This in turn reduces the CMV. In each cycle modulating signals of PWM4 are clamped to either +ve DC or -ve DC. During this duration the pole voltages of inverter I and II are either +Vdc or -Vdc. During this instant only one inverter switches will operate and CMV generated will less and hence a reduction of CMV is observed.

4. Results and Discussion

The proposed PWM algorithms are compared for the four-level, three-level dual inverter topologies of five phase induction motor drives using MATLAB/SIMULINK based simulations. The parameters of the five-phase induction motor are tabulated in Table V.

Table V: Five-phase Motor parameters

STATOR INDUCTANCE LLS	476MH
ROTOR INDUCTANCE LLR	170MH

ROTOR RESISTANCE RR	0.17 Ω
STATOR RESISTANCE RS	0.22 Ω
MUTUAL INDUCTANCE M	151 mH
POLE P	4
SWITCHING FREQUENCY FS	1KHz
INPUT DC VOLTAGE	540V
RATED MOTOR CURRENT	3.4 AMPS
RATED SPEED	1450RPM

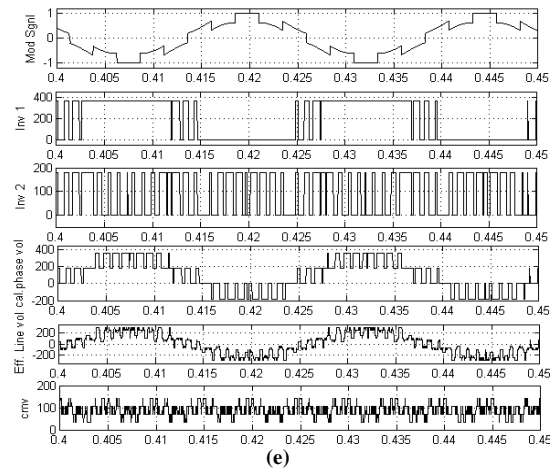
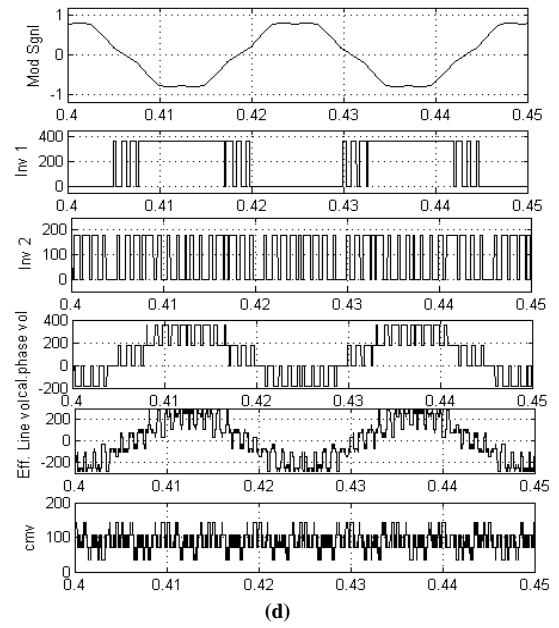
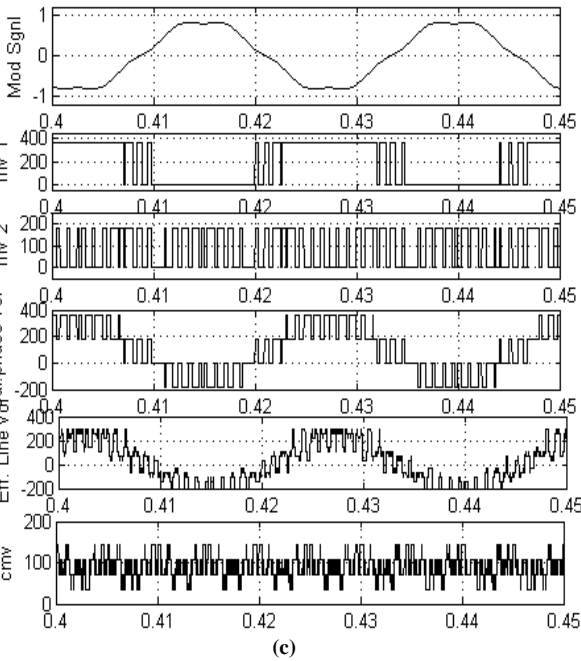
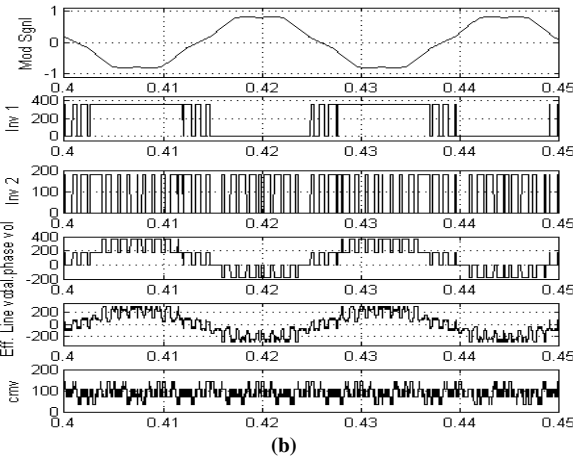
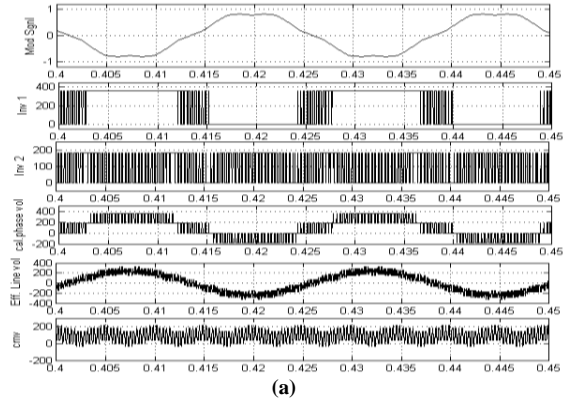
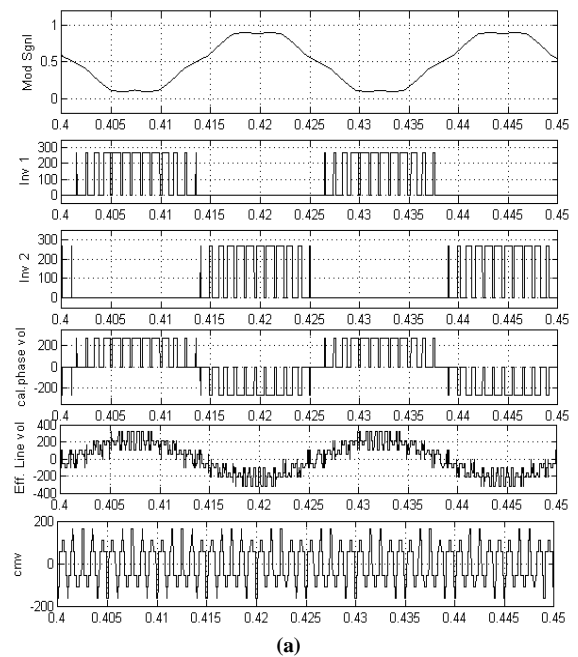
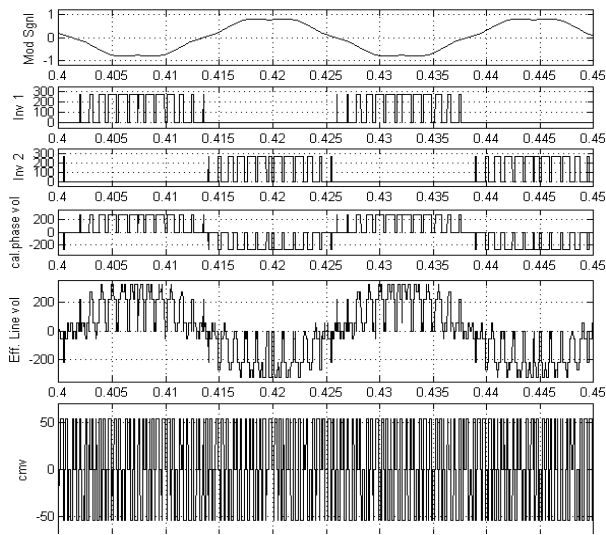
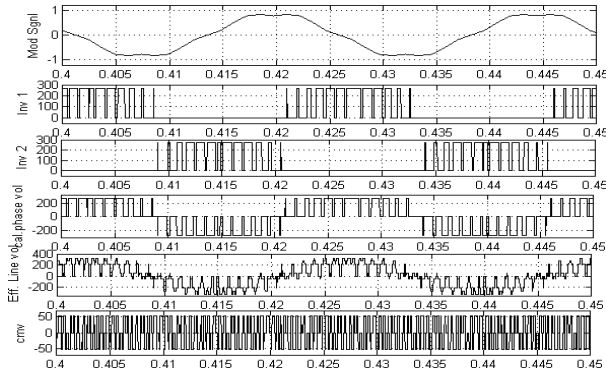


Fig 5 : Output plots for conventional SVPWM and proposed PWM techniques (PWM1,PWM2,PWM3, PWM4) for the four-level topology of the dual inverter fed five-phase induction motor drives.

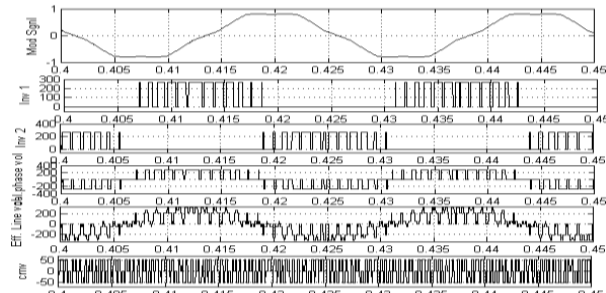




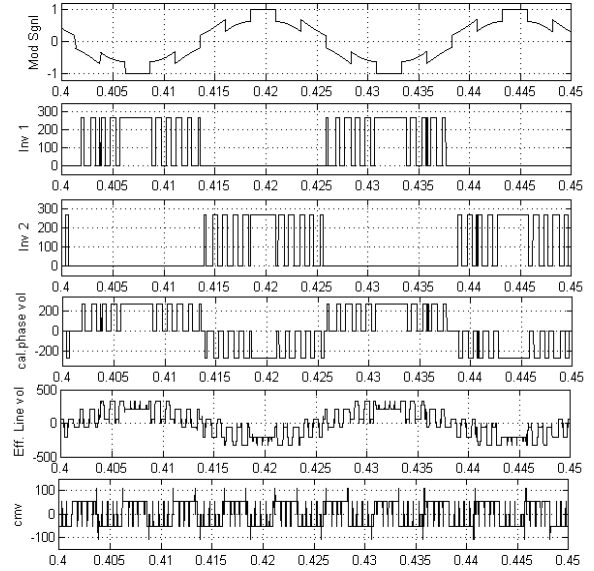
(b)



(c)



(d)



(e)

Fig 6: Output plots for conventional SVPWM and proposed PWM techniques (PWM1, PWM2, PWM3, PWM4) for the three-level topology of the dual inverter fed five-phase induction motor drives.

The five-phase induction motor is controlled by maintain the five-phase induction motor is controlled by maintaining v/f ratio constant. The plots of modulating signal; pulse patterns of inverter I and II; calculated phase voltage; effective phase voltage and CMV are plotted for conventional and proposed PWM techniques for three-level and four –level topologies with modulation index of 0.85 in Fig 5 and 6. It is observed from the results that the modulating signals of conversional, proposed PWM1, PWM2 and PWM3 are continuous and PWM4 is discontinuous. Table VI shows the number of levels and peak to peak CMV for the three-level and four-level topologies of dual inverter fed five-phase induction motor drives.

The results reveals that for the three-level topology the proposed PWM techniques can reduce the CMV from (162V) to (54V) with only 2 levels (+Vdc/10,-Vdc/10) in output CMV compared to 5 Levels (+3Vdc/10,+2Vdc/10,0,-2Vdc/10,-3Vdc/10). This indicates that in three-level topology a reduction of 66.6% reduction in CMV is observed. Similarly for four-level topology the proposed PWM technique can reduce the peak to peak CMV of +Vdc/15 to +5Vdc/15 in conventional PWM to proposed PWM peak to peak CMV of +4Vdc/15 to +Vdc/15.

MODULATION INDEX	PEAK-PEAK CMV AND NUMBER OF LEVELS							
	3-LEVEL PWM1,PWM2,PWM3 AND PWM4		3-LEVEL SVPWM		4-LEVEL PWM1,PWM2, PWM3 AND PWM4		4-LEVEL SVPWM	
0.1	$\pm 5V_{dc} / 10$		$\pm 3V_{dc} / 10$	4	$+ 3V_{dc} / 15$ TO $+ 2V_{dc} / 15$	2	0 TO $+ 5V_{dc} / 15$	5
0.2	$\pm 5V_{dc} / 10$		$\pm 3V_{dc} / 10$	4	$+ 3V_{dc} / 15$ TO $+ 2V_{dc} / 15$	2	0 TO $+ 5V_{dc} / 15$	5
0.3	$\pm 4V_{dc} / 10$		$\pm 3V_{dc} / 10$	5	$+ 3V_{dc} / 15$ TO $+ 2V_{dc} / 15$	2	0 TO $+ 5V_{dc} / 15$	5
0.4	$\pm 3V_{dc} / 10$		$\pm 3V_{dc} / 10$	7	$+ 4V_{dc} / 15$ TO $+ V_{dc} / 15$	2	0 TO $+ 6V_{dc} / 15$	5
0.5	$\pm 3V_{dc} / 10$		$\pm 3V_{dc} / 10$	6	$+ 4V_{dc} / 15$ TO $+ V_{dc} / 15$	4	$-V_{dc} / 15$ TO $+ 6V_{dc} / 15$	6
0.6	$\pm 3V_{dc} / 10$		$\pm 3V_{dc} / 10$	6	$+ 4V_{dc} / 15$ TO $+ V_{dc} / 15$	4	$-V_{dc} / 15$ TO $+ 6V_{dc} / 15$	6
0.7	$\pm 2V_{dc} / 10$		$\pm 3V_{dc} / 10$	6	$+ 4V_{dc} / 15$ TO	4	$-V_{dc} / 15$	6

					$+V_{dc}/15$		$TO + 6V_{dc}/15$	
0.8	$\pm V_{dc}/10$	2	$\pm 3V_{dc}/10$	5	$+4V_{dc}/15$ TO $+V_{dc}/15$	4	$-V_{dc}/15$ TO $+6V_{dc}/15$	6
0.9	$\pm V_{dc}/10$	2	$\pm 3V_{dc}/10$	5	$+3V_{dc}/15$ TO $+V_{dc}/15$	3	0 TO $+5V_{dc}/15$	6
1.0	$\pm V_{dc}/10$	2	$\pm 3V_{dc}/10$	5	$+3V_{dc}/15$ TO $+V_{dc}/15$	3	0 TO $+5V_{dc}/15$	6

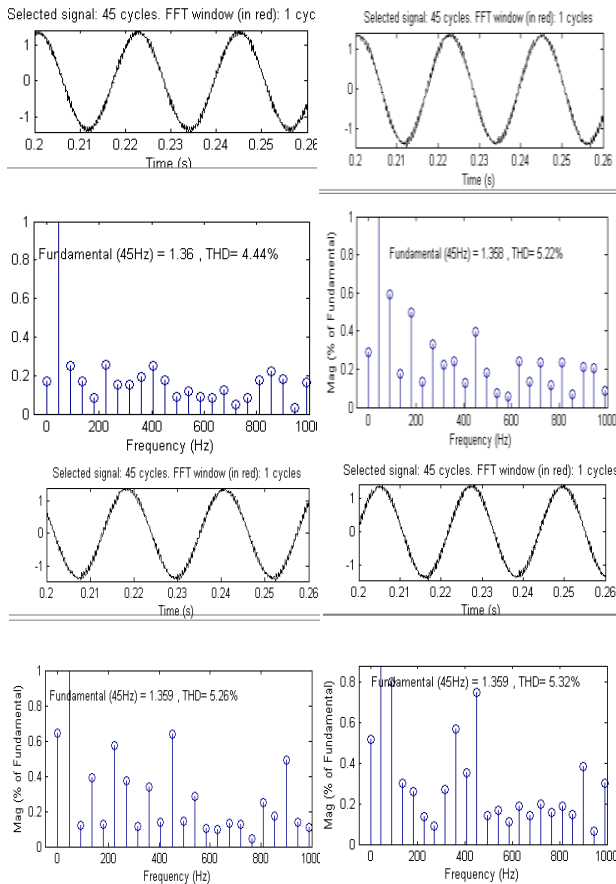


Fig 7: Phase a current waveform and its Harmonic spectrum for three-level topology for svpwm and proposed PWM techniques at MI=0.85

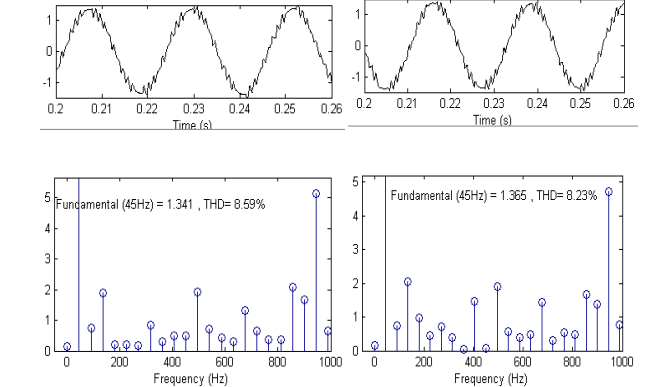
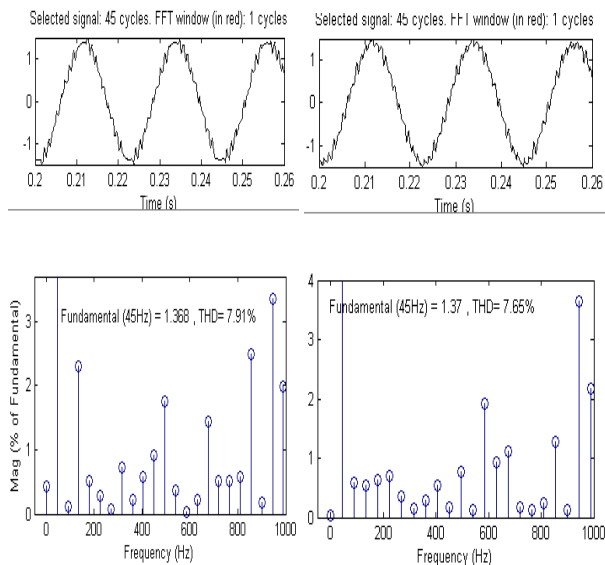


Fig 8: Phase a current waveform and its Harmonic spectrum for four-level topology for svpwm and proposed PWM techniques at MI=0.85

The FFT analysis of phase a currents in table V indicates almost similar values for proposed PWM techniques. On comparison the conventional SVPWM scheme has lesser harmonics. This indicates that the proposed PWM technique is efficient in reducing the peak to peak values and number of levels in CMV for both three-level and four-level topologies but induces some harmonics in phase currents.

Table VII: FFT analysis of stator current

PWM TECHNIQUE	FOUR-LEVEL TOPOLOGY	THREE-LEVEL TOPOLOGY
SVPWM	4.44%	7.91%
PWM1	5.22%	7.65%
PWM2	5.26%	8.59%
PWM3	5.27%	8.23%
PWM4	5.32%	8.35%

5. Conclusion

A simplified method for common mode voltage reduction for dual inverter fed open end winding five phase machine with two different topologies (three-level and four-level) has been proposed. These schemes greatly reduced the complexity involved in classical space vector approach. The proposed PWM scheme depends upon determination of the slope and location method which is very simple in implementation. The proposed reduced the peak to peak CMV from to i.e. 66.6% reduction in three-level topology and in four-level topology the peak to peak CMV from (0 to $+5V_{dc}/15$) to ($+3V_{dc}/15$ to $+V_{dc}/15$) i.e 40% reduction. And also the proposed PWM schemes reduced the number of levels in CMV and lesser ripples in phase currents also reduced, which improves the drive performance. FFT analysis of the stator currents for the conventional svpwm and the proposed PWM are quite similar for both three-level and four-level topologies.

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