International Journal of Engineering & Technology, 7 (4) (2018) 3294-3298

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET
doi: 10.14419/ijet.v7i4.16596
Research paper

Model predictive control based stacked asymmetric multilevel inverter driver

Dr. Raaed F. Hassan [1] *, Dr. Naseer M. Yasin [2]

[1] *Department of Control and Automation Eng. Techniques- Electrical Engineering Technical College - Middle Technical University*
[2] *Department of Electrical Power Eng. Techniques- Electrical Engineering Technical College - Middle Technical University*
**Corresponding author E-mail: drraaed_alanbaki@eetc.mtu.edu.iq*

Abstract

A new structure of a multi-level inverter has been constructed and simulated in this paper to feed a three-phase load. The proposed inverter is a five-level three-phase asymmetric cascade topology. Each phase leg is configured by stacking three-level flying capacitor converter (FCC) and three-level diode clamped converter (DCC). A model predictive current control (MPCC) is employed for generating gating signals that minimize the predefined cost function. These gating signals is applied to the switches of the inverter in the future sample interval. Results from Simulation show the effectiveness of the suggested inverter in achieving the desired results with a significant reduction in the number of flying capacitors and clamping diodes.

Keywords: *Model; Predictive; Stacked, Asymmetric; Multilevel Inverter.*

1. Introduction

Multilevel converters become an essential and crucial part in the modern power systems [1-2]. It has the capability of handling high voltage magnitudes, produce low harmonic distortion, and improving power utility [3-9]. The idea of multilevel inverter is to partition the high voltage level of the dc source into smaller voltage levels. Therefore, power electronic devices of small voltage rating can be utilized in these topologies. In the N-level inverter, the dc bus voltage is evenly divided into small voltage levels, each level equal $V_{dc}/(N-1)$. This configuration will provide a significant reduction of voltage stress on the power semiconductor devices. As the number of levels increase, the step size of the AC voltage will be decreased and approaches a sinusoidal shape, in other words, the harmonic distortion of the output voltage will be decreased. Three main categories of multilevel inverters have been introduced. These are; diode clamped converter (DCC), flying capacitors converter (FCC), and H – bridge converter (HBC) [1], [3], [6], [9] - [12]. These categories have individual limitations as indicated in [9]. Recently, different topologies are developed from the conventional multilevel converters [7], [9], [13] – [17]. In addition to its topology, the behavior of the converter largely depends on the quality of the control algorithm to be considered. Various control algorithms are presented for controlling the converters and drives. The most proposed control algorithm in the literature is Space Vector Pulse Width Modulation (SVPWM) [4] - [7], [9] - [15], [17]. Another popular method for controlling the converters is the hysteresis band current control (HBCC) [1], [2], [8]. These two algorithms are established based on providing appropriate control command to the modulator which is direct the switching states of the converter. However, development of more powerful and fast microcontrollers and computers permits to implement new and more complicated control algorithms. Among these new algorithms is the Model Predictive Current Control (MPCC) [3], [18] – [23]. In this control algorithm a model of the system is employed for prediction of the future performance of the converter current. The prediction is evaluated according to a predefined cost function then the switching state that minimizes the cost function is applied to the converter in the next sampling interval [21] – [23]. MPCC has an advantage over the SVPWM and HBCC algorithms because it generates the gating signal directly without need of the modulator. In this paper a 3-level FCC and a 3-level DCC are stacked to configure the new 5-level inverter topology which is significantly reduces the number of the capacitors and clamping diodes. MPCC is employed for generating the gating signal to the proposed inverter.

2. Conventional multi-level inverter topologies

2.1. Diode clamped converter (DCC)

The three – level diode clamped converter has been proposed firstly by Nabae, Takahashi, and Akagi in 1981 [12]. A single - phase five level diode clamped inverter is shown in Fig.1. A dc source is distributed evenly across four capacitors C_1, C_2, C_3 and C_4 and connected in series with switches (S_1 – S_4) through diodes. For the five – level configuration, the voltage across each switch will be ($V_{dc}/4$) which represents the capacitor voltage. N – level DCC requires (N-1) × (N-2) clamping diodes per phase so it is clear that this inverter topology became bulky as the N increase [12].

2.2. Flying capacitor converter (FCC)

Multilevel flying capacitor converter was introduced 1992 by Meynard and Foch [12]. The configuration of the multilevel flying capacitor inverter is shown in Fig.2. This structure contains a hierarchy shape of DC side capacitors. For N-level topology, FCC needs $(N-1)$ DC link capacitors and $(N-1) \times (N-2)/2$ auxiliary capacitors in each phase when identical voltage rating is realized between auxiliary capacitors and the switches. Flying capaci-

Copyright © 2018 Dr. Raaed F. Hassa, Dr. Naseer M. Yasin. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

tor inverter has phase redundancies, whereas diode clamped inverter has only line to line redundancies [12].

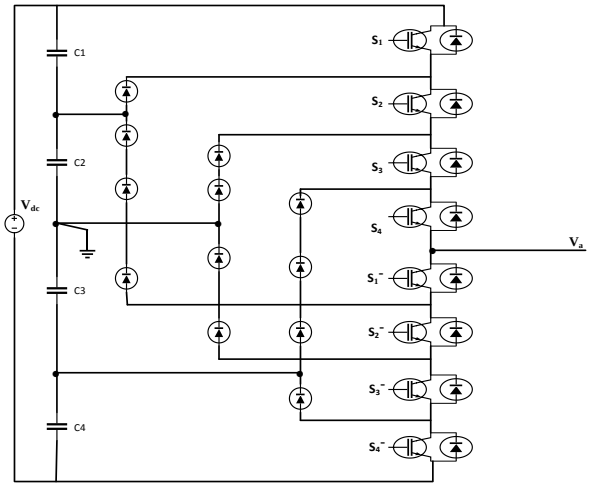


Fig. 1: One Leg 5 - Levels Diode Clamped Inverter.

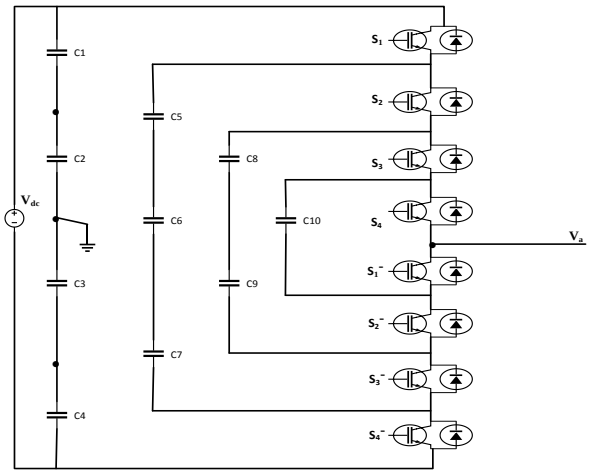


Fig. 2: one leg five – levels Flying Capacitor Inverter.

2.3. Cascaded H-bridge

A one-leg circuit of a 5-level cascaded H-bridge converter is shown in Fig.3 [12]. Each single phase full bridge or H-bridge inverter is connected to a separate DC source (SDCS). The number of cells required for n – level inverter is (n-1/2). In this topology, there is no need for clamping diode or flying capacitors but a separate dc sources are required. Therefore, the applications of this topology are depend on the availability of the isolated dc sources [12].

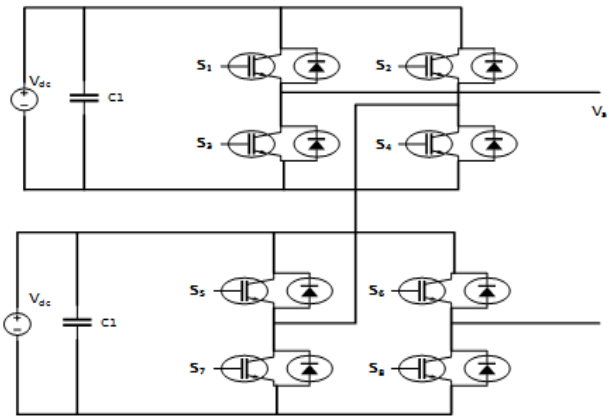


Fig. 3: One Leg 5-Level H-Bridge Inverter.

3. Proposed topology

The circuit diagram of the proposed five-level three phase asymmetric cascade topology is shown in Fig.4. Each phase leg is configured by stacking one three-level flying capacitor converter (FCC) Fig.4(a), and one three-level diode clamped converter (DCC) Fig.4(b).

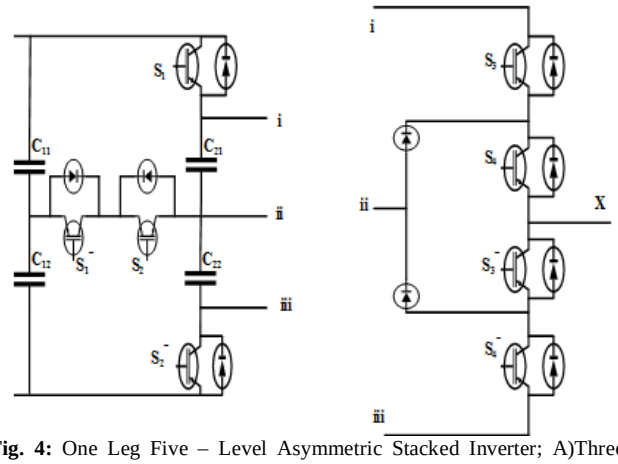


Fig. 4: One Leg Five – Level Asymmetric Stacked Inverter; A)Three-Level FCC B) Three-Level DCC.

In FCC stage, the first cell is configured by S_1, $\bar{S}_1$, and C_{12} when S_2 is closed for long time, while closing S_1^- for long time enforce, S_2, $\bar{S}_2$ and C_{22} to form another cell. When C_{11} and C_{12} are equal in their capacitances, the V_{dc} will be distributed evenly between them (i.e. $V_{dc}/2$ on each). The voltages across the flying capacitors C_{12} and C_{22} will be ($V_{dc}/4$) for each one. The phase voltage is the sum of the voltage produced by the DCC plus the voltage across $\bar{S}_2$. When S_2 is closed (S_2=1, $\bar{S}_2$=0) for long time, S_1 function driving S_1, $\bar{S}_1$ pair producing $v_{\bar{S}_2} = \frac{V_{dc}}{2}\Big|_{S_1=1}$ and $v_{\bar{S}_2} = \frac{V_{dc}}{2}\Big|_{S_1=0}$. Furthermore, when S_1 is opened (S_1=0, $\bar{S}_1$=1) for long time, S_2 function driving S_2, $\bar{S}_2$ pair producing $v_{\bar{S}_2} = \frac{V_{dc}}{4}\Big|_{S_2=1}$ and $v_{\bar{S}_2} = 0|_{S_2=0}$. The states that combines $S_1 = 1$ and $S_2 = 0$ are forbidden, since they close a loop which includes all the capacitors, so their original voltages cannot be sustained. The second stage is the DDC which has two switching functions S_3 and S_4 driving S_3, $\bar{S}_3$ pair and S_4, $\bar{S}_4$ pair respectively. Table 1 summarize the voltages produced by the two stages of the inverter and the resultant arm voltage according to the switching states.

Table 1: Switching States and Voltages of the 5-Level Asymmetric Stacked Inverter

S_1	S_2	S_3	S_4	v_{S_2}	v_{DCC}	v_{xn}
0	0	0	0	0	0	0
0	0	0	1	0	$V_{dc}/4$	$V_{dc}/4$
0	1	0	0	$V_{dc}/4$	0	$V_{dc}/4$
0	1	0	1	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/2$
1	1	0	0	$V_{dc}/2$	0	$V_{dc}/2$
1	1	0	1	$V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
0	1	1	1	$V_{dc}/4$	$V_{dc}/2$	$3V_{dc}/4$
0	0	1	1	0	$V_{dc}/2$	$V_{dc}/2$
1	1	1	1	$V_{dc}/2$	$V_{dc}/2$	V_{dc}

From table 1, it can be noticed that the arm voltage has five levels: 0, $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ and V_{dc}. According to the forbidden states of the FCC, all states 10xx should be avoided. Also the DCC stage has 10 forbidden state, therefore all states xx10 should be avoided. As a result, table II contains 9 states from 16 states and the remaining 7 states are forbidden. Comparing this proposed topology with the 5-level DCC, it can be shown that most of the clamping diodes are eliminated. Also, the number of flying capacitors are reduced when comparing the proposed topology with the 5-level FCC.

4. Converter model

The power circuit diagram of a three phase 5-level asymmetric converter feeding a three phase R-L load is shown in Fig. (5)
Each phase voltage can be calculated as a function of switching states and DC voltage V_{DC} as:

$$V_{an} = (S_{a1} + S_{a2} + S_{a3} + S_{a4})\frac{V_{DC}}{4} \quad (1)$$

$$V_{bn} = (S_{b1} + S_{b2} + S_{b3} + S_{b4})\frac{V_{DC}}{4} \quad (2)$$

$$V_{cn} = (S_{c1} + S_{c2} + S_{c3} + S_{c4})\frac{V_{DC}}{4} \quad (3)$$

The line voltages can be obtained as:

$$V_{ab} = V_a - V_b \quad (4)$$

$$V_{bc} = V_b - V_c \quad (5)$$

$$V_{ca} = V_c - V_a \quad (6)$$

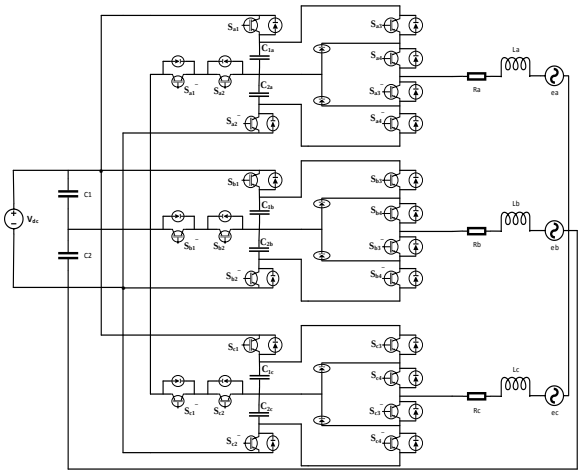


Fig. 5: Three Phase Five Level Structure Inverter.

For a three phase inverter, there are 61 switching states to determine the equivalent voltage space vector according to the following equation:

$$V_s = \frac{2}{3}(V_{an} + aV_{bn} + a^2V_{cn}) \quad (7)$$

Where:

$$a = e^{j\frac{2\pi}{3}}$$

5. Load model

From the definitions of variables shown in figure 8, the output loop equations for each phase are as follows:

$$V_{an} = L\frac{di_a}{dt} + Ri_a + e_a \quad (8)$$

$$V_{bn} = L\frac{di_b}{dt} + Ri_b + e_b \quad (9)$$

$$V_{cn} = L\frac{di_c}{dt} + Ri_c + e_c \quad (10)$$

Substitute equations (8-10) into (7) to get:

$$V_s = \frac{2}{3}\Big[L\frac{d}{dt}\big((i_a + ai_b + a^2i_c)\big) + R\big((i_a + ai_b + a^2i_c)\big) + (e_a + ae_b + a^2e_c)\Big] \quad (11)$$

According to the definition given in equation (7) and the definitions below for the load current and back-emf vectors

$$i_s = \frac{2}{3}(i_a + ai_b + a^2i_c) \quad (12)$$

$$e_s = \frac{2}{3}(e_a + ae_b + a^2e_c) \quad (13)$$

The output vector can be represented by the following differential equation

$$L\frac{di_s}{dt} = V_s - Ri_s - e_s \quad (14)$$

The output vector equation (14) can be discretized using forward Eular approximation

$$\frac{di_s}{dt} = \frac{i_s(k+1) - i_s(k)}{T_s} \quad (15)$$

Then the discrete form of equation (14) is:

$$i_s(k+1) = \Big(1 - \frac{RT_s}{L}\Big)i_s(k) + \frac{T_s}{L}\big(V_s(k) - e_s(k)\big) \quad (16)$$

Also the back-emf $e_s(k)$ can be estimated using equation (14)

$$e_s(k-1) = V_s(k-1) - \frac{L}{T_s}i_s(k) - \ (R + \frac{L}{T_s})i_s(k-1) \quad (17)$$

Balance of the capacitors voltages is an important issue that affects the performance of the inverter. Therefore, the prediction of the capacitor voltage must be contributing in the evaluation of the cost function and it's calculated as follows:

$$i_c = C\frac{dv_c}{dt} \quad (18)$$

$$\frac{dv_c}{dt} = \frac{v_c(k+1) - v_c(k)}{T_s} \quad (19)$$

Using eq.'s (18 and 19) to determine the prediction of the capacitors' voltages:

$$v_{c1}(k+1) = v_{c1}(k) + \frac{1}{C}i_{c1}T_s \quad (20)$$

$$v_{c2}(k+1) = v_{c2}(k) + \frac{1}{C}i_{c2}T_s \quad (21)$$

Where $v_{c1} and\ i_{c1}$ are the capacitor's C_1 voltage and current respectively , and $v_{c2} and\ i_{c2}$ are the capacitor's C_2 voltage and current respectively.

6. Model predictive current control

In driving the power converters, model predictive current control depends on the fact that there is a finite number of possible switching states can be generated by a static power converter. The system models can be used to predict the performance of the controlled variables for each switching state. The future switching state that will be applied to the converter is selected according to the minimization of the pre-defined performance index or cost function. In the current control strategy, the cost function is defined as follows [21]:

$$g_c = \big|i_{\alpha ref}(k+1) - i_{\alpha p}(k+1)\big| + \big|i_{\beta ref}(k+1) - i_{\beta p}(k+1)\big| + |v_{c1}(k+1) - v_{c2}(k+1)| \quad (22)$$

Where
$i_{\alpha ref}$ and $i_{\beta ref}$ are the real and imaginary components of the reference current

$i_{\alpha p}$ and $i_{\beta p}$ are the real and imaginary components of the predicted current

A block diagram of the predictive current control of the three phase five level asymmetric converter is shown in Fig. (6). It can be seen from Fig. (6) that the reference current is assumed to be unchanged, that is:

$$i_{ref}(k+1) = i_{ref}(k)$$

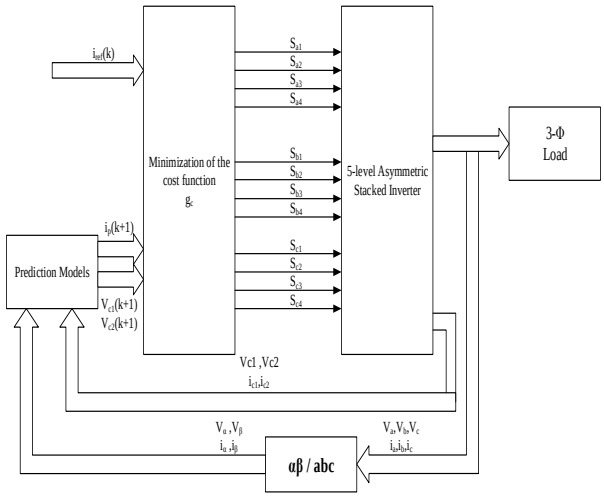


Fig. 6: Systematic Diagram of Predictive Current Control.

7. Simulation results

In order to evaluate the performance of the proposed inverter, simulation has been achieved based on Matlab / Simulink. The power circuit of the inverter is constructed using Simulink, while the MPCC algorithm is implemented using Matlab function block. The results from simulation has been obtained according to the following design parameters:

Input DC Voltage: 600 V.
Input Capacitors C_{11}, C_{12}: 5000 µF.
Capacitors of the FCC: 2500 µF.
Filter impedances: 5 mH.
Filter resistances: 0.45 Ω.
Load impedance: 5 + j0.7.
Sampling Interval: 50 µsec.

The asymmetric stacked inverter produces three – phase 9-level line to line voltages as shown in Fig. (7).

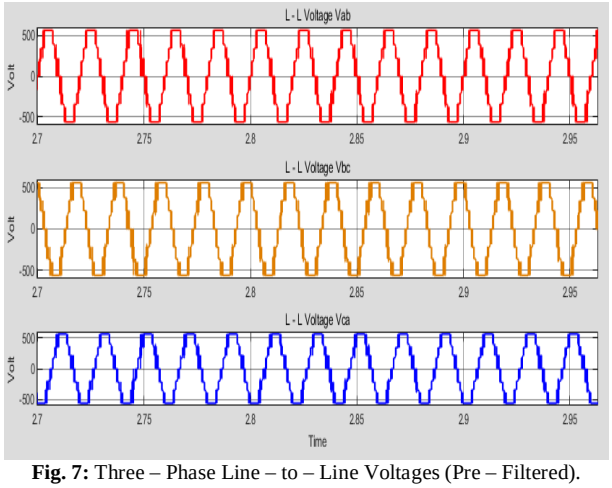


Fig. 7: Three – Phase Line – to – Line Voltages (Pre – Filtered).

Fig. (8) shows the same voltages after processing based on the RL filter.

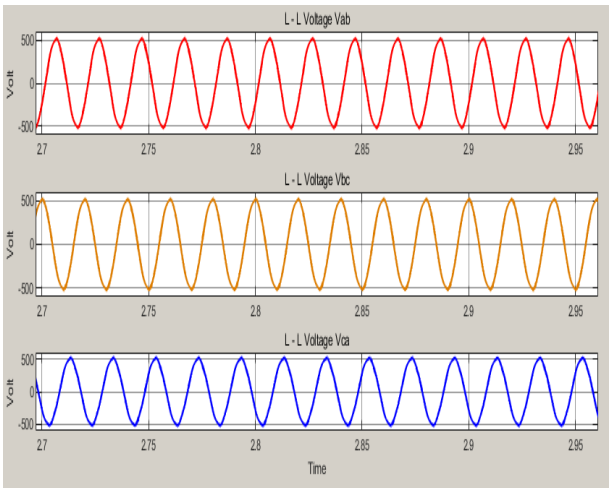


Fig. 8: Three – Phase Line – to – Line Voltages (Post – Filtered).

The load voltage and current per phase are shown in Fig. (9), it can be noticed that they are in phase i.e. unity power factor (p.f= 0.998).

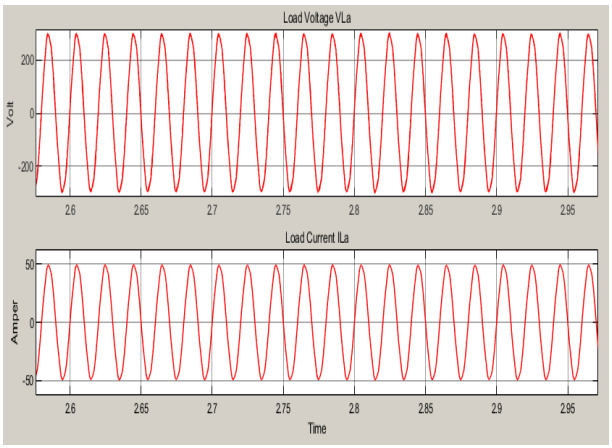


Fig. 9: Single – Phase Load Voltage & Current.

A minimum Total Harmonics Distortion (THD) of the load current is achieved as shown in Fig. (10).

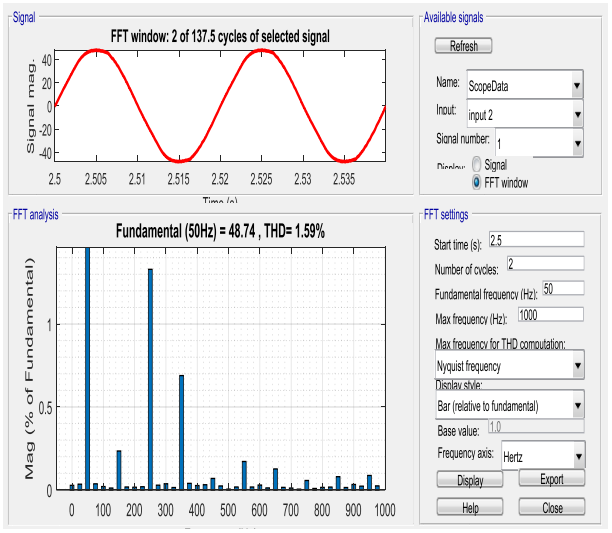


Fig. 10: THD of the Load Current.

Including the prediction of the input capacitors voltages in the cost function leads to balance the voltages across these capacitors as shown in Fig. (11) with acceptable voltage drop in both capacitors (≤ 40 v).

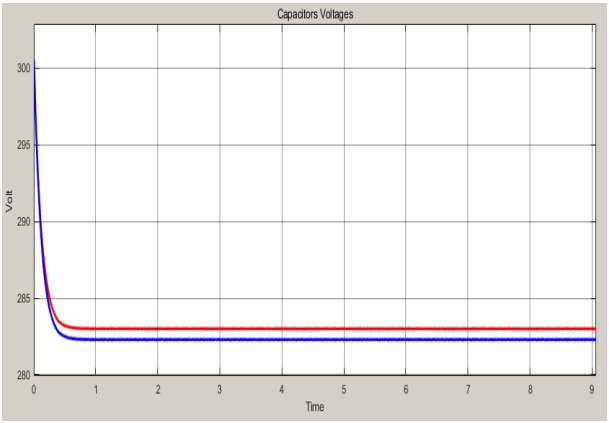


Fig. 11: Input Capacitors Voltages.

The trajectory of the load currents in αβ plane system is shown in Fig. (12) which indicates the minimum distortion in these currents.

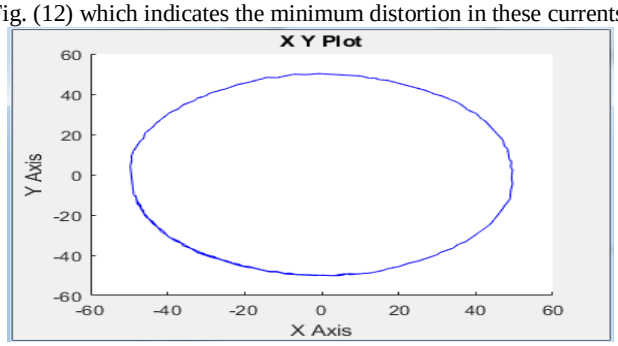


Fig. 12: Locus of the Load Current in [2] – Coordinates Plane.

8. Conclusions

A configuration of a three-phase five-level asymmetric stacked inverter has been submitted. This proposed topology is composed from stacking 3-level FCC and 3-level DCC in series for each phase. It has an advantage of using less components than the other two types (FCC and DCC) which leads to considerable reduction in circuit complexity for performing the same task. Model predictive current control is employed for driving the proposed inverter. The dominant feature of this controller is directly generate the gating signals to the inverter as a result of prediction values that minimize the defined cost function. Generation process of the desired gating signals don't need a modulator like the conventional control algorithms. This facilitates the MPCC to control different variables that affect the inverter model.

References

[1] F. Zare and G. Ledwich, "A Hysteresis Current Control for Single-Phase Multilevel Voltage Source Inverters: PLD Implementation," IEEE TRANSACTIONS ON POWER ELECTRONICS, vol. 17, no. 5, pp. 731-738, 2002. https://doi.org/10.1109/TPEL.2002.802192.

[2] p. c. Loh, G. H. Bode, D. G. Holmes and T. A. Lipo, "A Time-Based Double Band Hysteresis Current Regulation Strategy for Single-Phase Multilevel Inverters," IEEE Transactions on Industry Applications, vol. 39, no. 3, pp. 883 - 892, 2003. https://doi.org/10.1109/TIA.2003.810667.

[3] F. Zare and G. Ledwich, "A New Predictive Current Control Technique for Multilevel Converters," in TENCON 2006 - 2006 IEEE Region 10 Conference, Hong Kong, China, 2006. https://doi.org/10.1109/TENCON.2006.343727.

[4] L. Jih-Sheng, H. Allen, M. Arindam and G. Frank, "Characterization of a Multilevel HV-IGBT Module for Distribution Applications," in IEEE Industry Applications Conference Forty-First IAS Annual Meeting, Tampa, FL, USA, 2006.

[5] P. M. Brendan, G. H. Donald and M. Thierry, "Reduced PWM Harmonic Distortion for Multilevel Inverters Operating Over a Wide Modulation Range," IEEE TRANSACTIONS ON POWER ELECTRONICS, vol. 21, no. 4, pp. 941-949, 2006. https://doi.org/10.1109/TPEL.2006.876864.

[6] B. Stefano, Z. Pericle, W. Alan, T. Luca and C. C. Jon, "Advanced Power Electronic Conversion and Control System for Universal and Flexible Power Management," IEEE TRANSACTIONS ON SMART GRID, vol. 2, no. 2, pp. 231-243, 2011. https://doi.org/10.1109/TSG.2011.2115260.

[7] P. A. Miguel, C. Laura and I. V. María, "Multilevel Current-Source Inverter With FPGA Control," IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, vol. 60, no. 1, pp. 3-10, 2013. https://doi.org/10.1109/TIE.2012.2185014.

[8] G. Shweta and G. Rajesh, "Switching Frequency Derivation for the Cascaded Multilevel Inverter Operating in Current Control Mode Using Multiband Hysteresis Modulation," IEEE TRANSACTIONS ON POWER ELECTRONICS, vol. 29, no. 3, pp. 1480-1489, 2014. https://doi.org/10.1109/TPEL.2013.2262807.

[9] V. N. R, A. R. S, S. Pramanick, K. Gopakumar and L. G. Franquelo, "Novel Symmetric Six-Phase Induction Motor Drive Using Stacked Multilevel Inverters With a Single DC Link and Neutral Point Voltage Balancing," IEEE Transactions on Industrial Electronics, vol. 64, no. 4, pp. 2663 - 2670, 2017. https://doi.org/10.1109/TIE.2016.2637884.

[10] L. Jackson and L. H. Marcelo, "Generalized Synchronous Optimal Pulse Width Modulation for Multilevel Inverters," IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6297 - 6307, 2017. https://doi.org/10.1109/TPEL.2016.2621022.

[11] O. Saeed, R. Z. Mohammad, K. Masih, S. Mahmoud, R. Jose, O. Hashem, L. Pablo and U. S. Andres, "Improvement of Post-Fault Performance of Cascaded H-Bridge Multilevel Inverter," IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, vol. 64, no. 4, pp. 2779 - 2788, 2017. https://doi.org/10.1109/TIE.2016.2632058.

[12] P. Aparna and B. Sanjay, "A comparative analysis of classical three phase multilevel (five level) inverter topologies," in 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 2016.

[13] S. Aparna, E. Ali and S. Yilmaz, "A novel three-phase multilevel diode-clamped inverter topology with reduced device count," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016.

[14] S. Emad, S. Abdolreza, A. G. Sayyed and A. Jafar, "A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters," IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 987 - 996, 2018. https://doi.org/10.1109/TPEL.2017.2675381.

[15] K. Mohammad, T. Amir, A. Jafar and R. Mohammad, "Multi-level inverter with combined T-type and cross-connected modules," IET Power Electronics, vol. 11, no. 8, p. 1407 – 1415, 2018. https://doi.org/10.1049/iet-pel.2017.0378.

[16] B. Ebrahim, "A Cascade Multilevel Converter Topology With Reduced Number of Switches," IEEE TRANSACTIONS ON POWER ELECTRONICS, vol. 23, no. 6, pp. 2657-2664, 2008. https://doi.org/10.1109/TPEL.2008.2005192.

[17] K. D. Madan, C. J. Kartick and S. Akanksha, "Performance evaluation of an asymmetrical reduced switched multi-level inverter for a grid-connected PV system," IET Renewable Power Generation, vol. 12, no. 2, pp. 252 - 263, 2018. https://doi.org/10.1049/iet-rpg.2016.0895.

[18] K. Igim, C. Roh and K. Sangshin, "Model predictive control method for CHB multi-level inverter with reduced calculation complexity and fast dynamics," IET Electric Power Applications, vol. 11, no. 5, pp. 784 - 792, 2017. https://doi.org/10.1049/iet-epa.2016.0330.

[19] M. B. Hazrul and M. Saad, "Digital predictive current control of multi-level four-leg voltage-source inverter under balanced and unbalanced load conditions," IET Electric Power Applications, vol. 11, no. 8, p. 1499 – 1508, 2017. https://doi.org/10.1049/iet-epa.2017.0032.

[20] B. Ahmad, M. Mostafa, S. B. Robert and A.-R. Haitham, "Optimum number of cascaded multilevel inverters for high-voltage applications based on Pareto analysis," in 2017 IEEE Texas Power and Energy Conference (TPEC), College Station, TX, USA, 2017.

[21] J. Rodriguez, P. Cortes, R. Kennel and et.al, "Model predictive control -- a simple and powerful method to control power converters," in 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, China, 2009.

[22] Atif, M. Shaikh and R. Khaliqur, "Finite State Predictive Current and Common Mode Voltage Control of a Seven-phase Voltage Source Inverter," International Journal of Power Electronics and Drive System (IJPEDS), vol. 6, no. 3, pp. 459 - 476, 2015.

[23] H. Goh, A. Aida and S. L. a. e. al., "Predictive Direct Power Control (PDPC) of Grid-connected Dual-active Bridge Multilevel Inverter (DABMI)," International Journal of Power Electronics and Drive System (IJPEDS), vol. 8, no. 4, pp. 1524 - 1533, 2017.