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Research paper



Design and Simulation of Timing Recovery Synchronization for Digital Wireless Receiver Based on SDR Technology

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Abstract

The design and simulation of the digital wireless receiver with talented time recovery synchronization based on software-defined radio (SDR) technology are present in this paper. The fast growth of wireless communication systems with complexity and constraints increasing is placed upon the hardware to utilize the ability of the developed algorithms. New algorithm efforts were provided for more bandwidth capability to utilize the frequency and time recovery and achieve accurate synchronization between transmitter and receiver. In addition, as high bandwidth receiver become integrated into small mobile, high synchronization is required to attain low power consumption and small size components. This work suggests efficient time recovery techniques to neglect much computation and reduce the power consumption in the digital wireless receiver based on SDR technology. The use of systematic SDR design methodology is to develop the system which provides better synchronization and could reconfigure the equipment without replacement. The proposed design allows to introduce high-level simulation including the constraints and has a functional simulation system capable to translate to hardware implementation without any difficulties. The simulation and implementation results show a promising technique to support the current and future generation of wireless mobile receiver.

Keywords: *Synchronization, Timing Recovery, Digital Wireless Receiver, SDR*

1. Introduction

In Early of 1991, the aim to move some of the digital signal processing by means of SDR technology has been proposed by [1]. Nowadays, the SDR technology becomes, in reality, to use for more flexibility and adaptability in most wireless systems as close as possible to the antenna. This technology is permitted to reconfigure the hardware components without the need to change any part of the receiver device [2]. Consequently, the SDR technology provides an adaptable platform occupied with an analog system with data synchronization via DSP techniques to correct the symbol time in the receiver section [3]. The management of symbol time is possible in case of missing the transmitted signal at the receiver in physical layers. Many options have used to matched the filter output samples by means of signal filtering required in case of oversampling or significant cutting in the baseband signal. The Nyquist rate is desirable to be close to the processing signal to have computational efficient DSP [4]. In the sampling clock, the poly phase filter becomes more effective which permits to high flexibility in the receiver by computing the necessary multiplications for matched filtering. At the same time, the interpolation will achieve sufficient sampling [5]. The filter bank in polyphase type proposed by [6] has used in symbol synchronization of the digital receiver under SDR technology with loop control development to optimize the filter design. In their proposal, they insert a numerical control oscillator (NCO) before the matcheded filter to minimize the distortion created by the carrier offset. His design allows simulating track the symbol time and carrier phase in same time. Additionally, the proposed system incorporate coarse frequency and symbol time offset. The synchronization of carrier phase before matched filter could be despoiled by noise interference. Therefore, inserting matched filter before decimator could consume expensive resource in this process. For this case, more investigation of an alternative technique of collective two signals process block with autonomous control loop could be contributed [7, 8]. The major task of a digital communication system is to transmit and receive binary data via a specific channel. Fig. 1 shows the main block diagram of the digital system includes a transmitter, channel, and receiver [9]. The analog data is sampled by using the D/A converter and the source coding is applied in the transmitter part. The generated bitstream is extended associated with error correction by channel encoder in order to decrease the distortion created by the transmission channel. The bit stream is shaped to baseband and modulated which transmits after amplifying by power amplifier via the antenna to the channel. By means of amplitude, frequency and phase modulation, the carrier wave of low noise amplification should be used in the receiver side [10]. In addition to all mentioned process, the symbol synchronization should be used on the receiver side as an important process to accurately recover the received data.

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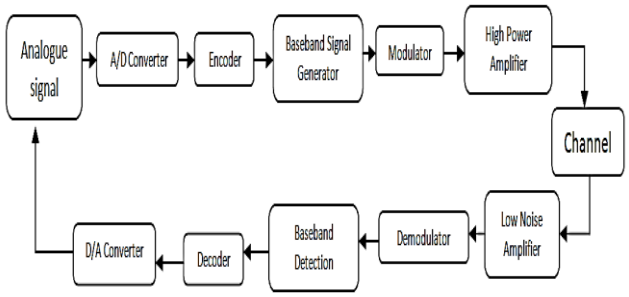


Fig. 1: Digital transceiver System

In the receiver section, the phase, frequency and time recovery synchronization should be performed to receive the proper information [11]. In this work, an efficient technique to time recovery and synchronization has been introduced as illustrated in Fig. 2.

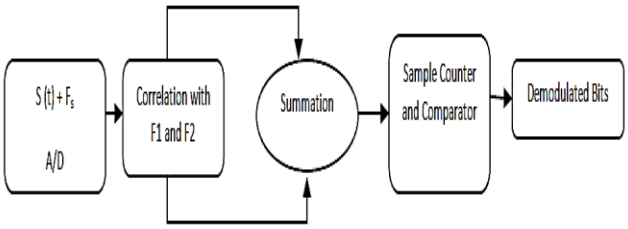


Fig. 2: a synchronization algorithm for digital receivers

2. The principle of Synchronization Theory

Firstly, assume the analog signal S(t) is the amount of symbol filtered by pulse determining filter P(t) which separated by the time unit (T) and suppose the received signal is delayed to S(t) via noise n(t) and could be articulated as follow:

$$r(t) = n(t) + s(t-\tau) \quad (1)$$

To optimize the receiver performance, one could use matched filter output y(t) with impulse response:

$$h(t)=p(-t) \quad (2)$$

The received signal in discrete uniform sampling period Ts is r(nTs) which applied to an interpolator at minimum rate Ti = T/N and the interval of synchronization should be adjusted to Ti interval in order to matched the rate of transmitting data symbol. The new sample of interpolator filter h1(t) with the time is given by [12, 13]:

$$y(kT_i) = \sum_{i=I1}^{I2} r[(m_k - i)T_s]h_I\,[(i+\mu_k)]T_s \quad (3)$$

where
$m_k = kT_i/Tsc$ represents the base point index
$\mu_k = kT_i/T_s - m_k$ represents the unreasonable index of time offset

The decomposition of polyphase sampling techniques of matcheding filtering can be used to determine the interpolation coefficients. Hence, the impulse response of M number in filter bank can be expressed as in [14]:

$$h_m(nT_s) = h\,(nT_s) + \frac{m}{M}T_s) \quad (4)$$

The synchronization objectives are to select the filter bank with index m to fraction portion $\frac{m}{M}T_s$ as close as possible to the time offset μ_k as explained in Fig. 3. A fine solution could be sufficiently provided by choosing more filter bank sequences. As shown, the number of the interpolator in filter bank lies on optimum output.

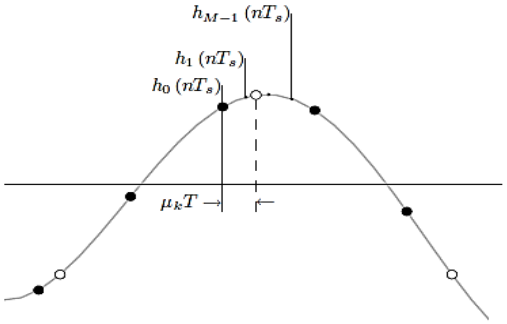


Fig. 3: Relationship between the sample point and interpolated samples

The timing of symbol can be tracked by so-called (tracking loop) which has dual pairs of matcheding filter with derivation matcheding filter which can be produced by a polyphase filter bank. Hence, the output of each symbol interval can result in matched and derivation output respectively which send to time error generator to adjust them. The common techniques used to recover the samples in the receiver part are the coherent algorithms. For correlation purpose, the sample function is used as a reference waveform [15]. The coherent receiver has better performance than non-coherent in term of bandwidth which is lost in the case of not maintained process [16]. The existing communication systems such as mobile is subjected to multipath propagations which affected by rising from different paths of propagation. In difference with the traditional digital modulation scheme, the transmitted symbol has shaped to a finite set of periodic waveforms segmentations [17]. The text message of a sequence of characters for alphanumeric is encoded into a sequence of bits named baseband signal or bitstream. The group of K bits can be combined to produce a new symbol in the system and the size of this symbol referred to M-array. Both K and M values signify the initial selections in the system. Bandpass waveform detection uses a similar concept of baseband detection in matched filter realization with AWGN presence [18].

3. Model Design and Simulation

The design and simulation of a digital receiver are to synchronize the data code time sent by a radio station and decode this message to display the data time. The SIMULINK block set and DSP toolbox system have been used to provide digital receiver design. Fig. 4 shows the complete structure of a receiver model.

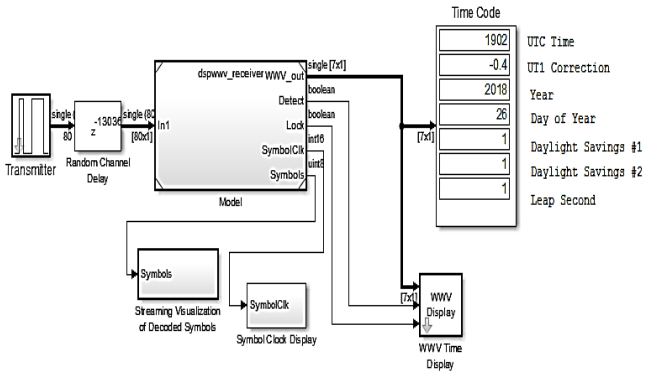


Fig. 4: Digital Receiver model

Fig. 5 illustrates the frame decoder of the transmit trigger. The symbol was displayed as a decoded symbol on the time scope. Fig. 6 shows the decipher time code data displayed by timecode display. The reduction has divided into two parts one for daylight indicator 1 and the other for daylight indicator 2 respectively. The number of samples is pointed to the clock drift between the rising edge of succeeding symbol in the receiver which varies between 90 and 100 sample.

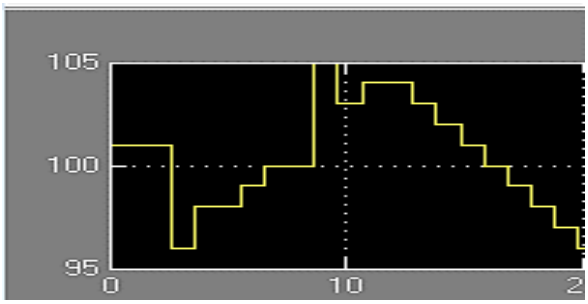


Fig. 5: Input signal

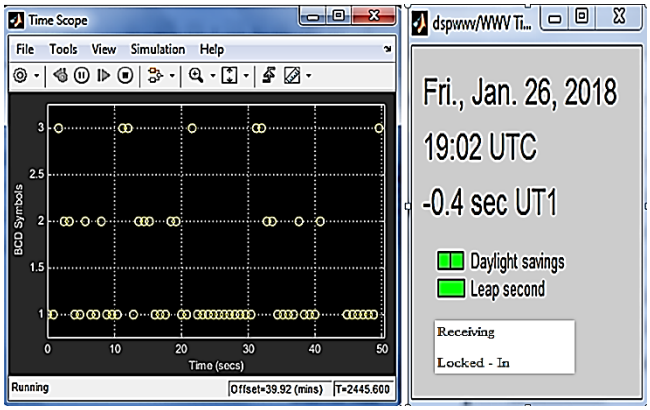


Fig. 6: Decoded time display scope

The model has continuing current time constraints set to the current mode. The updating functions were done each minute and you can change the display time constraints of the transmission systems to be used as defined function specifying all time requirements. The subsystems of the designed model are shown in Figs. 7, 8, 9 and 10 that illustrate the details of each part. For capable buffering of input sample, the buffer sample is inserted to maintain the internal circular isolation. The buffered sample has used a valid output frame computed at what time received Boolean at the port of output. In case of suitable frame predictable in the receiver section, the subsystem of frame synchronization gives Boolean true is buffered as well. To process the suitable frame, the identical Boolean wave acts as a trigger to the subsystem of a receiver. This collection will run the receiver as required and the buffer sample output is running also. This collection is used in synchronization and demodulation as well as for decoding.

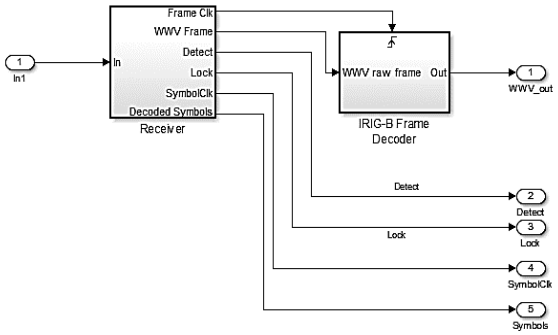


Fig. 7: Decoder and receiver design

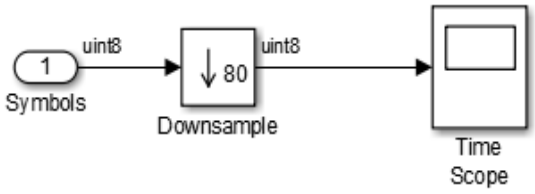


Fig. 8: Visualization of streaming decoded symbol

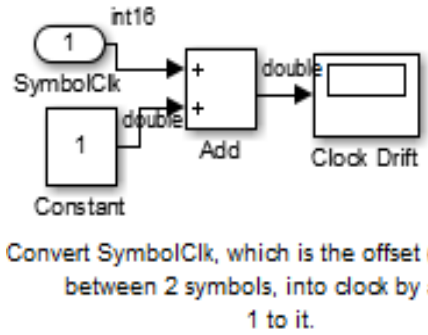


Fig. 9: Symbol clock display

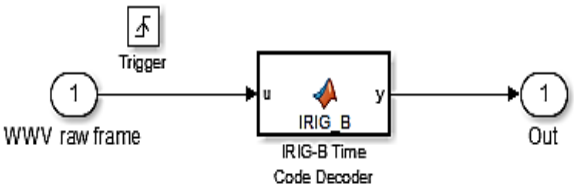


Fig. 10: Frame decoder

The sample synchronization block carries out the symbol synchronization by taking the input as a rising edge of the demodulation signal represented by 100 samples as shown in Fig. 11. The sample block parameters are symbolized by N1, N1est and N window. These parameters represent a number of samples, estimated number of sample and window sample respectively. The N-half window represents the half window length.

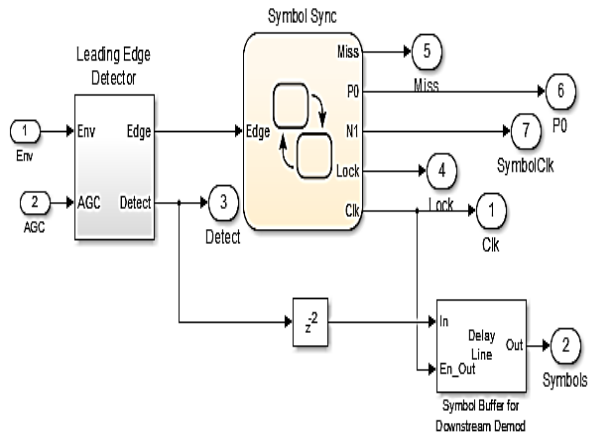


Fig. 11: Timing recovery of the received symbol

The synchronization process starts when the chart succeeds the system claims by assuming the rest symbol is valid or else the chart is still waiting until the succeeding sample occurs again. In case of this chart is not found silence through this interval, the chart is treating new edge such a reference edge. These steps are repeated much time until it is succeeding another silence after getting edge reference. This chart determines and calculates how many silence samples after reference sample to detect another edge in the sequence. In case of establishing next edge within N windows, the chart changes the status to (Lock) position in order to start receiving the symbol again. When the subsequent edge is not established inside the N window, the orientation edge discards, and searches again for reference edge. Lastly, if the chart does not find any symbol in two successive times, in this case, the chart is going to lock state. The chart keeps tracking the sample in window port after finding next edge in the sequence. After the sample has found inside the window, the update process is repeated again and the new sample will be calculated for a new edge. This chart permits to have founded edge within N windows to calculate the missing symbol. However, when this process happened for two consecutive times, the start symbol synchronization is repeated another time. The clock signal can be generated by clock synchronizer if new rising edge received of the demodulation signal. In these methods, the clock has synchronized with any occurrence of new edge without SIMULINK clock running at a fixed rate sometimes. Fig. 12 shows the structure of receiver timing recovery and AGC circuit connections.

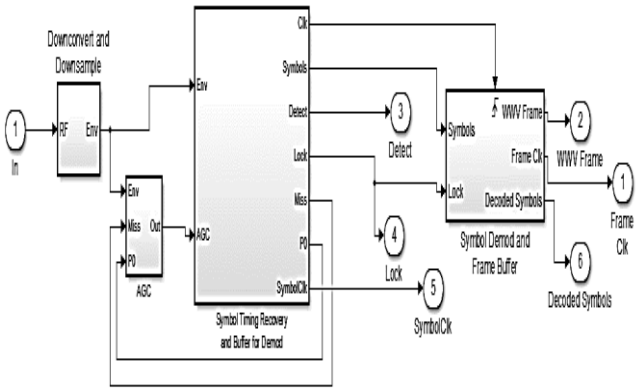


Fig. 12: AGC and timing recovery of the Receiver

This integration of template produces a specific sample to run the symbol in case of finding the edge sample to use in AGC block. Fig. 13 illustrate the AGC receiver structure. The AGC block guesses the amplitude of demodulation signal which used as a standard signal in the next process.

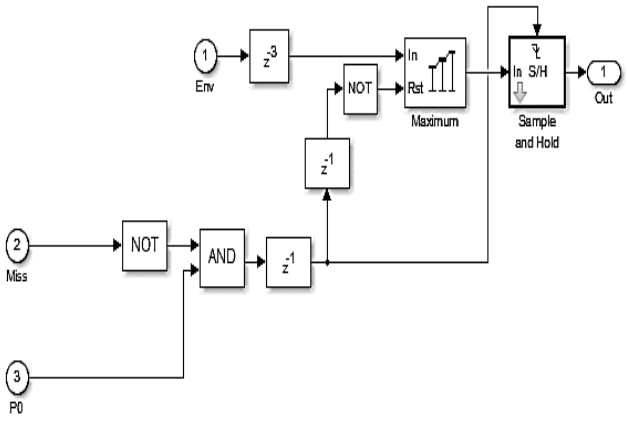


Fig. 13: Receiver AGC design

The frame of buffer and symbol demodulation shown in Fig. 14 have triggered each time when a nonzero clock is received by using the block of vector quantization to achieve the modulation process of the symbol. This process is done by a comparison between the input of buffer and next four candidate symbols to provide the best matcheding. The system of frame synchronization precedes the delay line for consecutive occurrence and missing symbol. Because of this process, the new frame will start and delay line output could be a valid buffer only. In this instance, the subsequent decoder has triggered to generate binary code within a hundred Hertz. The sample rate used in the SIMULINK model is about 8000 sample per second.

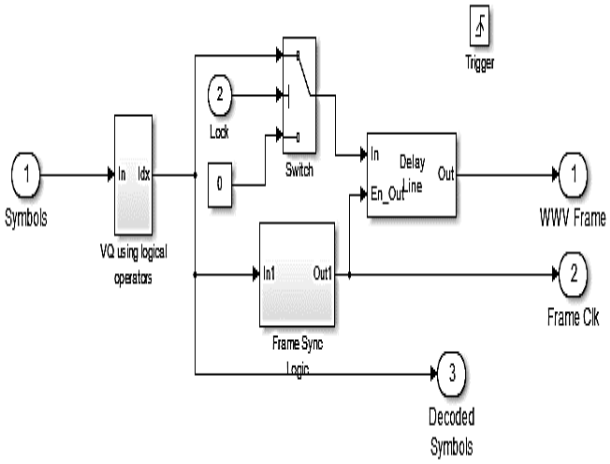


Fig. 14: Frame buffer and symbol demodulation subsystem

The downsampling block is shown in Fig. 15 accepts the input pulse with modulated signal to perform the envelope detection and low pass filtering and down sampling by 80 to the received signal. Hence, every transmit signal has 100 symbols in demodulation process and the block output is serial of variable square pulses in length and interval.

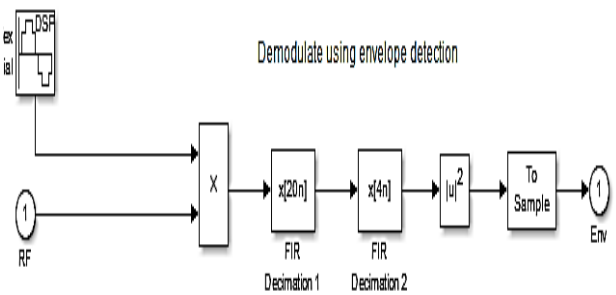


Fig. 15: Down sampling and demodulation process

The timing recovery of the symbol and demodulation buffer are used to provide symbol synchronization from demodulation buffer which has the leading edge detector to quantize the symbol into specific waveform. The detected output signal is right when the values of the demodulation signal are bigger as compared with AGC signal or else goes to a false situation.

4. Implementation Results

The proposed model is based on the design of system generator environments from Mathworks to implement the suggested digital receiver timing recovery as shown in Fig. 16. The SIMULINK block set is incorporated with a system generator in programming structure [19, 20, 21].

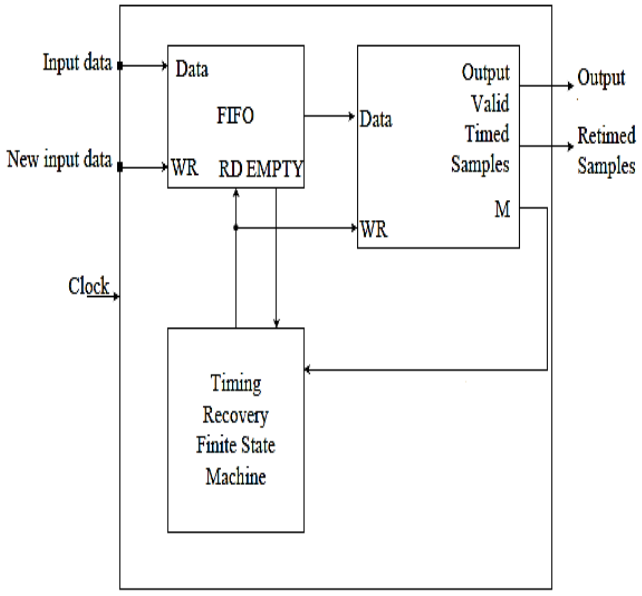


Fig. 16: Timing recovery high-level design implementation

This design allows to the system generator to develop the structure at a suitable level of abstraction from target hardware and allow the user in same time to compute the graphical for simulation and verification with FPGA implementation environments. The system generator is a bit cycle and has a true performance model to FPGA properly. The full timing recovery design has been realized in all the above tools and its environments. The verification of simulation and implementation has been done without any error. The resource utilization of receiver timing recovery illustrated in table 1. This implementation requires one memory BRAM to realize the FIFO implementation with two BRAMs to store filter coefficients. The filter input needs only one identical BRAM to realize the time recovery filter and the real components of the receiver filter is required to form the time error signal. Due to using the one multiplier in this circuit, the error signal is generated for real components.

Table 1: Utilization of receiver timing recovery implementation in FPGA vertex-5

FPGA Version	BRAM	Slices	LUP /FFs	Utilizations
Vertex – 5	2	560	312/ 710	12%

The receiver timing recovery implementation will support a clock frequency of more than 300 MHz in a fast speed of FPGA vertex – 5. The implementation results show the processing interval of 25 clocks to produce the output sample rate. The data are in the modulation with a bit rate of 15.6 Mbps which is allocating more FPGA embedded filter unit to decrease the process timing.

5. Conclusion

In this paper, the synchronization design for digital communication receiver is investigated and developed. The proposed structure has totally browbeaten the correlation of the design in entity function block to synchronize the symbol and decrease the complexity by using a large computation load between many functional block set. The major specifications of this design are the symbol timing with the greatest correlation and the combined signal detection with low cost and high gaining. Additionally, the iterative organization for symbol evaluation compensates for the range and accurateness. The use of a polyphase filter bank in the interpolation process can provide many advantages for reliability and low complexity in receiver operation at the low sample rate. The integration of carrier tracks loop to the receiver system which provides a good solution to transmit mapping in a periodic acquisition of carrier frequency and symbol time is compulsory in this case. The simulation indicates the efficiency of the synchronization process to track many symbols and frequency offsets under different conditions. In addition, the implementation of time recovery scheme using FPGA vertex-5 under SDR platform was tested and the results show an important utilization in term of slices and LUP. Lastly, the proposed model is promising to support the current and future generation of digital wireless receivers.

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