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Research paper

An enhanced sensitivity RF energy harvester system using tunnel FET based rectifier

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Abstract

Radio Frequency (RF) energy harvesting system is a viable solution for powering ultra-low power sensors as long as there is minimal am-bient power that exists around it. However, at very low ambient RF level or under sub-milliwatt (< -20 dBm) level conditions, the RF recti-fier in the harvester system shows very poor performance and probably fails to convert RF signal into DC output voltage. This is due to the sub-threshold voltage limits or weak sensitivity of the rectifying device used in the rectifier. However, to actively operate it in sub-milliwatt level RF input, this research proposes a band-to-band tunneling behavior of Tunnel FET (TFET) device. The steep slope characteristic of TFET contributes in improving the sensitivity, output voltage, and power conversion efficiency (PCE). Keysight Advanced Design System (ADS) software is used to conduct a simulation study on our proposed idea. An LC matching network is also designed using the smith chart tool to achieve maximum sensitivity. The proposed concept achieved a maximum sensitivity of -60 dBm at UHF of 900 MHz and produced an output voltage of 350 mV at -25 dBm. A maximum PCE of 70% at -39 dBm is obtained in the 3 stage voltage multiplier.

Keywords: *RF Energy Harvesting; Tunnel FET (TFET); Sub-Threshold Swing (SS); Sensitivity; Voltage Multiplier.*

1. Introduction

The enormous development and utilization of Radio Frequency Identification (RFID) and Wireless Sensor Network (WSN) systems has given more significance to the RF energy harvesting system for powering its internal circuits. In fact, the RF energy available in the environment is in the range of $\mu W/m^2$ at a particular distance from various sources such as TV stations, Cellular stations, WIFI, etc. but it can be used for powering WSN applications especially to be implemented in the area where it is very tough to change the batteries including under bridges, buildings, chemical plants, aircraft, etc. [1 - 2]. In the last decade, a number of researchers had proposed in their work that the generated power from the RF energy harvesting system is sufficient for powering the sensor nodes [3 - 5]. In that circumstance, it is possible only when a standalone RF source is implemented to transfer the power [6 - 8]. While using the standalone sources, the RF power transmitted through space will deteriorate when it travels a long distance. Under that situation, the RF harvester circuit does not provide the required output voltage, current driving capability, and at times it fails to operate. The failure of the RF harvester under this range can be ignored but not the RF rectifier that is not functioning or with very weak sensitivity. The performance of the RF rectifier is the most vital contribution of the RF harvesting system since the actual conversion of RF to DC is taking place here as shown in the block diagram of Figure 1. Hence, designing a RF rectifier with good sensitivity to work under very low RF input power is very challenging and resulting in a bottleneck for the RF circuit designer.

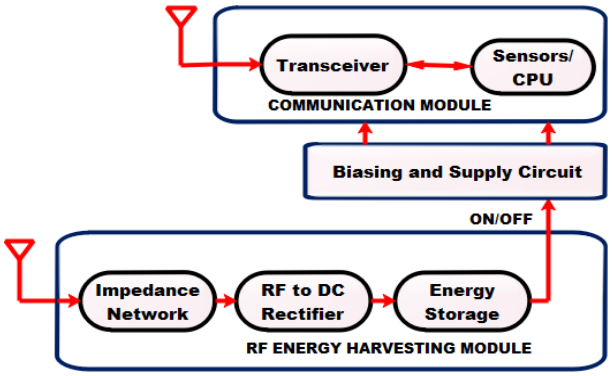


Fig. 1: Block Diagram of RF Powered WSN Which Consists of RF Harvesting Module, Communication Module and Supply Circuit.

The RF rectifier performance is evaluated mainly by two parameters [9] (i.e.) Power Conversion Efficiency and Sensitivity. PCE are the ratio of converted DC power to the RF input power as shown in equation (1). The conversion of RF to DC takes place in the rectifier section. Sensitivity is the minimum RF dBm input power to activate the whole system and it is given by equation (2) as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\text{Output DC Power}}{\text{RF Input Power}} \quad (1)$$

$$\text{Sensitivity (dBm)} = \log_{10}\left(\frac{P}{1mW}\right) \quad (2)$$

However, there are tradeoffs between these two parameters. These parameters are affected by the non-linear behavior, threshold volt-

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age value, forward bias current and off state leakage current of the components used in the circuits. If very low sub-threshold operation of device is chosen then it will lead to high leakage current and achieve very low efficiency. By addressing this bad threshold voltage of operation and having a limited SS value of 60 mV/decade in CMOS devices [10 - 11] at room temperature, this paper proposes the tunnel FET device to increase the sensitivity. Section 2 shows the literature review of research work related to enhancing the efficiency and sensitivity of the RF CMOS rectifier and its limitations. Section 3 of this paper discusses the TFET technology, modeling, and its advantages. Section 4 shows the design of the TFET rectifier based on the RF harvester with a matching network by simulation. The performances of the TFET harvester are discussed with results in Section 5. The conclusions are made in Section 6.

2. Review & challenges of RF CMOS rectifier

Normally, schottky diodes are used for designing the RF rectifier circuits at higher value of RF input (> 10 mW) since it has low on-state resistance and low forward voltage drop of 200-300 mV [12]. It is able to achieve more than 80% PCE because the matching is quite easy and it can deliver the DC power efficiently to the load. However, it requires extra steps to fabricate and make the cost incurred very high. Other drawbacks are the conventional CMOS fabrication technologies are not compatible to produce schottky diodes where high integration levels are desired. After that, the MOS connected diodes were preferred for use in the RF rectifier. However, the efficiency decreases severely due to high threshold voltage operation of CMOS devices. Certain researchers proposed several V_{th}, threshold voltage cancellation techniques to increase the power conversion efficiency [13]. An external bias voltage is added between gate and drain of a transistor which is called as External Voltage Cancellation (EVC) technique which is more efficient compared to the conventional charge pump but PCE is low because each stage requires different bias voltage and the circuit becomes quite complex. Similar to EVC, another technique called the IVC Internal Threshold Voltage Cancellation technique in which a gate bias voltage is generated by using an internal node of the rectifier. The main drawback of this IVC technique is that it requires additional circuitry of transistor, resistor, and capacitor and the circuits become very large in size. Self-Threshold Voltage cancellation technique (SVC) was followed in a number of rectifier circuits in which the gate terminals of MOSFET is cross connected and statically biased to produce the output voltage [14]. The SVC circuit does not require any external circuits but the disadvantage of this technique is sometimes the transistor will remain turned ON once the gate bias voltage is over boosted. Now, most of the RFID circuits commonly use two cross coupled SVC circuits in which the gate bias voltage is dynamically varying in the said to be Dynamic or Differential drive V_{th} Cancellation Technique (DVC). It shows good performance compared to other techniques [15] but it requires more number of switching components. Each Cancellation Techniques has some merits in increasing the PCE but it also includes in increasing the cost of fabrication and the circuit complexity.

3. TFET technology & its advantages

The scaling of MOSFET has been practiced in the semiconductor industries for the past half century to reduce the supply voltage and power consumption, increase the operating frequency, transistor density and speed [16]. But due to the tradeoff between V_{th} threshold voltage and off state leakage current of the transistor, its internal power consumption becomes more dominant and this characteristic is fundamentally controlled by the parameter called the Sub-threshold Swing (SS). In CMOS, it is limited to 60 mV/dec. The industry has pushed the scaling of cmos into its limit and forced to move to a new device which should operate in ultra-low power (requires SS to be less than 60 mV/dec), ultra-low voltage, less leakage of currents and high speed of operation. TFET is one of the promising and efficient device alternate to the MOSFET, especially to work under the conditions of ultra-low power applications [17 - 18]. Compared to MOSFET(N-P-N), the TFET is similar in structure consisting of the P-I-N tunnel diode that is gated as shown in Figure 2. The TFET has asymmetrical source and drain (i.e.) the dopants of the source that are opposite to draining.

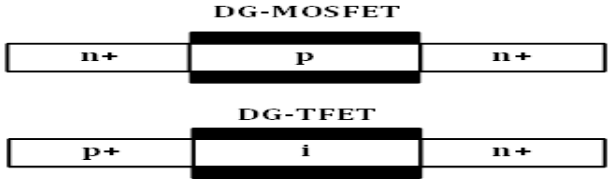


Fig. 2: Structure of MOSFET and Tunnel FET.

However, MOSFET has a symmetric source and drains (i.e) the dopants of source and drains are the same. In MOSFET, when high energy carriers exceed the potential barrier, only then is the carrier injection processed from source to drain due to thermionic emission. These high energy thermionic carriers follow the Fermi Dirac distribution and achieve a SS limitation of 60 mV/dec. The SS of MOSFET is given by equation (3):

$$SS = \frac{d(V_g)}{d(I_d)} = \frac{2.3mkT}{q} \quad (3)$$

$$\text{where } m = 1 + \frac{C_{dep}}{C_{ox}}$$

Where K-Boltzmann constant, T-temperature, C_{dep} is semiconductor depletion capacitance, and C_{ox} is the oxide capacitance. In TFET, conflicting band to band tunneling movement of electrons from source terminal to channel enables a better ON/OFF switching control as shown in Figure 3a. The high energy carriers distributed in the Fermi-Dirac tail are rejected by the bandgap in the source and hence it cannot contribute to the movement process. It is fundamentally the lower temperature of carriers involved in the transportation process through a tunneling window which results in a sub-threshold slope of less than 60 mV/dec. Thus, the SS of TFET curve has a steep slope compared to the MOSFET as shown in Figure 3b. The possibility of tunneling electrons movement from source terminal to channel is given by equation (4) [19]:

$$T(b2b) = \exp\left(\frac{-4\sqrt{2m^* E_g^3}}{3qh\delta}\right) \quad (4)$$

Where m^* and Eg is the relative mass and energy band gap of the material; δ is the tunnel junction electric field; q is the charge of electron; and h is Planck's constant. At ultra-low voltage condition, the choice of low band gap (Eg) and low relative mass materials (e.g., III-V, Ge etc.) are preferred and besides, hetero-band structure improves the tunneling probability and makes the on-drive current increasing. The efficient low power TFET has many advantages (a) Mostly appropriate for low power application because of less leakage current; (b) Can operate on SS of less than 60 mV/dec; (c) Band to Band tunneling process makes the operating speed higher; (d) OFF state current is lower; (e) Smaller Vth threshold voltage roll off; (f) Better ON/OFF current control; and (g) Invulnerable to short channel effects.

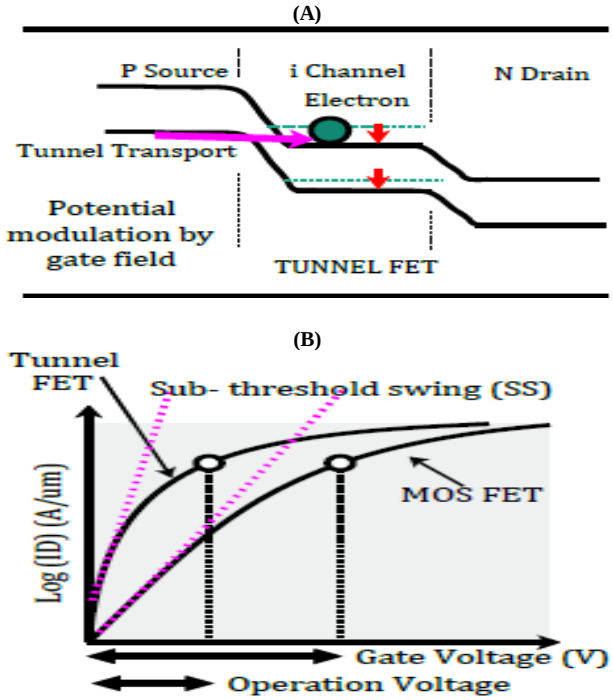


Fig. 3: A) Band- to- Band Tunneling Movement of Electrons in TFET B) Steep Slope Characteristics of TFET Compare to MOSFET.

3.1. TFET modelling and its DC characteristics

Recently, in most of the previous research works, the TFET device available in the form of Verilog A model is used in circuit. Verilog-A is a language used to describe the analog behavior models of analog circuits. It can be implemented in most of SPICE programs with inclusion of progressive features such as arrays, looping, conditional statements, events etc,. It is possible and easy to compile the Verilog-A in to binary which can take the advantages of running the model with efficient and speed. In this paper, GaN/InN hetero-junction N-type universal TFET Verilog-A model is used in our design for the rectifier simulation [21].

The modelling parameters are used to develop this Hetero-junction TFET as mentioned in Table 1.A new Tunnel FET symbol is created and Verilog-A code is entered with these model parameters can be compiled in the ADS software for device simulation. The device width (W) and Length (L) are chosen to be considered as design parameters. After modelling the device, its internal characteristics can be found by DC simulation.

Table 1: Model Parameters of GAN/INN TFET

Model Parameters	N- HTFET
L_g Gate Length	20nm
W Gate Width	17nm
EOT-Equivalent Oxide Thickness	0.43nm
E_G-Semiconductor Band Gap	0.64eV
T_{CH}- Channel thickness	20nm
V_{TH}- Threshold Voltage	0.096V
m_t- Reduced Effective Mass	0.1
LAMDA- Saturation Voltage parameter	0.435V
C_{GS0}- Gate Source Capacitance per unit width	2.3e-10F/m

To obtain the DC characteristics of the modeled TFET device operating in a sub-threshold region, a schematic circuit set up is made in which two supply voltage sources, Vgs and Vds, are connected as shown in Figure 4. By choosing the optimal value of W & L of the TFET device and sweeping the voltages Vgs and Vds, with minimum value from 0.1 to 1V, we can get the TFET DC drain current characteristics as shown in Figure 5a and 5b. From these characteristics, it is clearly observed that TFET has achieved a steep slope characteristic with SS value of 52 mV/dec which indicates the current driving capability is at a more low power of operation.

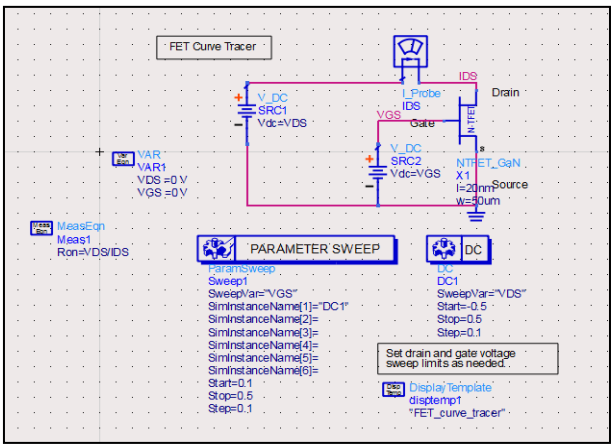


Fig. 4: Schematic Circuit to determine the DC characteristics of GaN/InN TFET

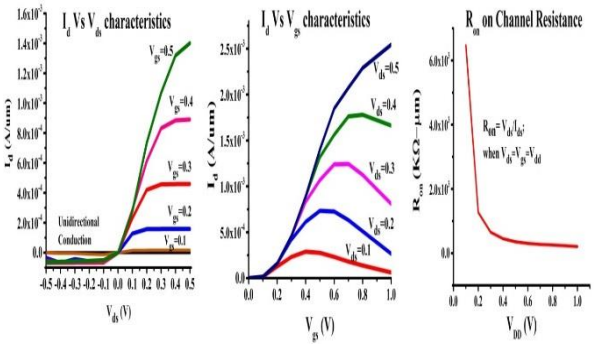


Fig. 5: TFET-DC-Characteristics A) Id Vs Vgs Characteristics B) Id Vs VDS Characteristics C) on-State Channel Resistance.

From these characteristics, it is clearly observed that TFET has achieved a steep slope characteristic with SS value of 52 mV/dec, which indicates the current driving capability is at a more low power of operation. Due to its P-I-N structure as well as asymmetric source and drain, it exhibits almost an unidirectional current conduction with very little reverse leakage current compared to other beyond CMOS devices. It is also operating at a very lower turn-on voltage of 0.096V, which increases the sensitivity of the rectifier or utilizing the low power RF input with negligible reverse leakage losses. By having these characteristics, PCE can be improved especially at low power dBm input. As shown in Figure 5c., the reduced on-channel resistance characteristics of TFET during very low voltage forward bias, will increases the PCE by reducing the resistive power losses.

4. Simulation of TFET based harvester

In this paper, the Keysight ADS tool is used to design and simulate the overall RF harvester circuit. The overall simulation steps and the procedure involved in the design of the proposed TFET based RF harvester is summarized in the form of a flow chart in Figure 6. After an extensive simulation using GaN/InN HTFET device with various rectifier architectures, Dickson topology structure.

Performance is good and it is proposed in this work as shown in Figure 7. To transfer maximum power from RF input source to the rectifier, a matching network (LC) is designed by using smith chart tool available in ADS. The smith chart utility tool for the different stages of TFET based rectifier is shown in Figure8.

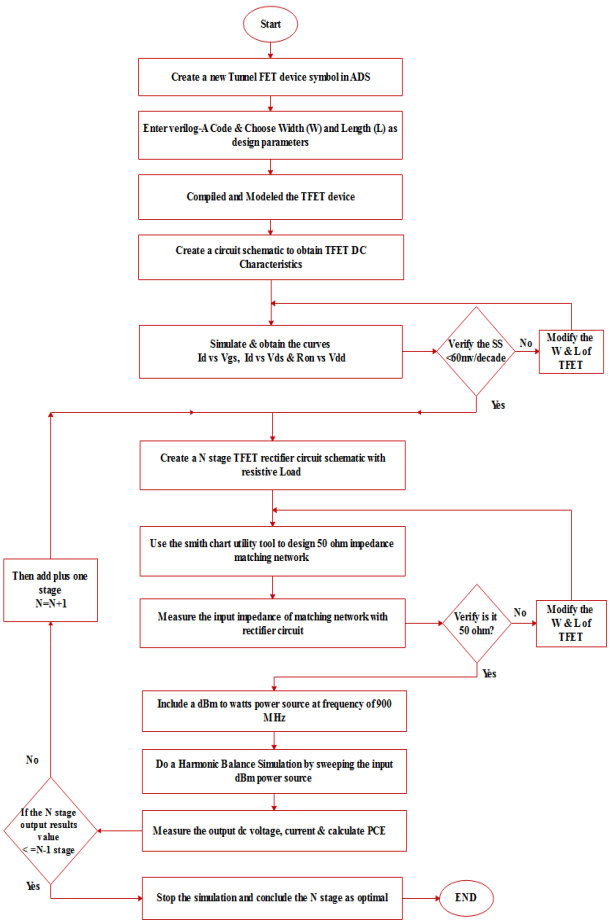


Fig. 6: Flow Chart Describes the Simulation Procedure Involved in the Design of TFET Based RF Harvester.

The designed LC impedance matching networks value are tabulated in Table 2. To determine the LC matching value, initially we have to measure the input impedance of the rectifier stages or voltage multiplier circuit by connecting the 50Ω port impedance on two ports. Then in the smith chart utility where entering the source impedance of 50Ω and load impedance value as the measured input impedance of rectifier stages in it; we can get the value of LC matching network through tuning by setting the frequency at 900 MHz. After designing the matching circuit, it is necessary to ensure that the characteristic impedance of the whole circuit supposed to be around 50 Ω for maximum power to be transferred.

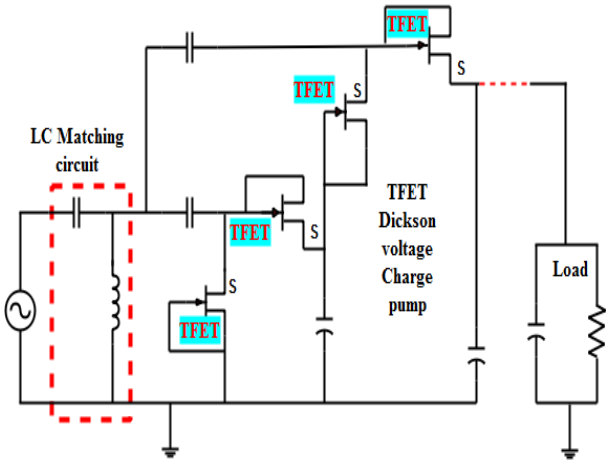


Fig. 7: Circuit Diagram of TFET Based RF Harvester Made of Dickson Charge Pump.

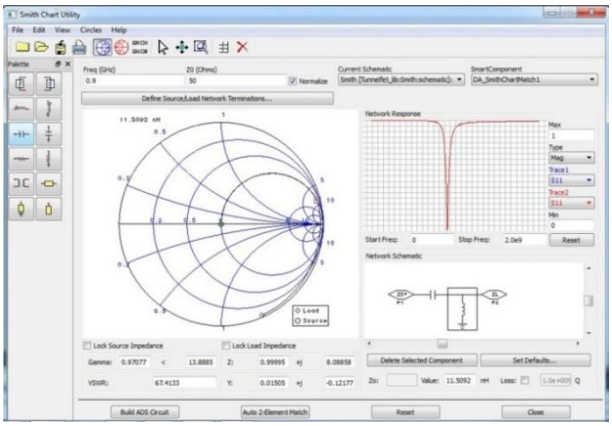


Fig. 8: Smith Chart Utility Tool for Designing the LC Matching Circuit at900 MHZ with Impedance of 50 Ω.

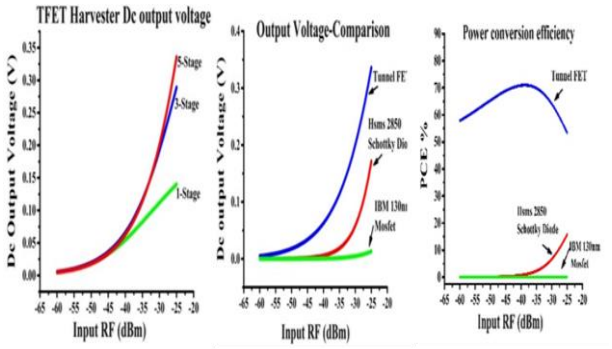


Fig. 9: A) Proposed RF Harvester DC Output Voltage Results Of Various Rectifier Stages B) TFET Performance Compared with Schottky Diode & MOSFET C) Calculated PCE In % Compared with Schottky Diode & MOSFET.

Table 2: Designed LC Impedance Matching Values

Number of stages	Measured Input impedance of TFET rectifier	Designed Impedance matching network	Measured Input Impedance of TFET rectifier with matching network
1stage	5.6-j230	L= 43.46 nH C= 9.95 pF	49.354-j0.092
3 stage	1.841-j77.34	L= 11.56 nH C= 437.25 fF	50.002-j0.001
5 Stage	1.1-j46.5	L= 9.52 nH C= 23.53 pF	49.904-j0.021

5. Results & discussion

Harmonic Balance simulation is a frequency domain analysis technique for simulating non-linear circuits and systems which are applied in our design for getting the output results [22]. Its performances can be studied by adding the stage one by one and analyzed by sweeping the RF input from -20 dBm to -80 dBm with ultra-high frequency of 900 MHz. The performance reveals that TFET output DC voltage is increased until 3 stages as shown in Figure 9a. The output voltage varies in the range of 350 mV to 5 mV while varying the RF input in the 3 stage TFET rectifier harvester. From the simulation, it is observed that output voltage increases from 1 stage to 3 stages but when it comes to 4 or 5 stage rectifiers, the output voltage gets saturated and is, more or less, similar to the 3 stage output due to the higher internal losses of the components. Further increasing the rectifier stages, the DC output voltage will be reduced but not shown in the graph. The higher DC output voltage of 350 mV, 3.3 µA current at -25 dBm in 3 stage, and lower DC voltage of 5 mV, 50 nA current at -60 dBm were obtained. The performance of the proposed TFET RF harvester was compared with Avago HSMS 2850 schottky diode and the IBM 130nm MOSFET harvester with the same topology of connection and stages. The performance of TFET at under low power dBm is superior when compared to other devices as shown in Figure 9b. The TFET achieves a maximum sensitivity of -60

dBm input due to perfect matching but the schottky diode sensitivity is only -45 dBm. The MOSFET rectifier can also extend its sensitivity to be more than -50 dBm, but the performance is very bad by providing a very low DC output voltage due to the high internal component and reverse leakage losses. The HTFET power conversion efficiency is also calculated for all the sweeping input RF levels as shown in Figure 9c.

Table 3: Comparison Table of Previous Research Works

Reference/ Parameter	Wang, J .et.al [23]	Beheshti.et.al [8]	Wang.W.et.al. [9]	Liu .et.al [20]	Cavalheiro.et.al [19]	This work
Cmos Fabrication	0.18 µm CMOS	180nnm CMOS	40nm CMOS	20nm GaSb/InAs HTFET	20nm GaSb/InAs HTFET	20nm GaN/InN HTFET
Device Vth	(EVC)	0.354V	0.45V	0.1, -0.12	Sub 0.25	0.096
Matching Network	LC Matching Network	-	LC Matching Network	-	-	LC Matching Network
Rectifier Topology	2-T Drive	2-T doubler circuit	Full wave Dickson	4-T Differential Drive	4-T Differential Drive	Dickson topology
RF frequency	145 MHZ	900 MHZ	900 MHZ	915 MHz	900 MHZ	900 MHZ
RF input power/ voltage	-18dBm	0.4 µW /0.35 v	0.4 to 0.55 V	-34.5 dBm Vin 0.25 v	-55 dBm to -5 dBm	-60dBm to -20 dBm
Output DC voltage	1 V	2 V	1.34 V	0.41 v @ 2-stage	0.58 V @ -20 dBm	0.35V @-25dBm
PCE	25.87%	10%	44%	85%	68% @ -43 dBm	70% @ -39 dBm
Sensitivity	-22.5 dBm	-	0.39V	-34.5 dBm	-50 dBm	-60 dBm
No. of stages	4	13	7	2	2	3

The proposed one has achieved a maximum PCE of 70% at -39 dBm. Other comparative devices have achieved a poor PCE at low power dBm. From the thorough analysis through simulation, it is observed that TFET performance is superior to other rectifying components especially in low power RF input. However, its performance deteriorates at higher RF dBm input or milli-watt level (> -10 dBm) condition. This is because the band-to-band tunneling concept is not happening. During that situation, the Schottky diode is the best choice, which performs well and provides a higher DC output voltage and current. The comparison of previous research works are shown in Table 3.

6. Conclusion

A band-to-band tunneling behavior of TFET based RF harvester circuit is proposed in this paper to increase the sensitivity of the system. The proposed TFET harvester has given better performance compared to CMOS, especially in ultra-low power and low voltage applications because it has the advantage of steep slope characteristics due to very low turn-on voltage and high ON current drive capability. The proposed harvester with different stages of a rectifier are designed, analyzed, and compared with conventional rectifier components such as HSMS 2850 Schottky diode, and IBM 130 nm MOSFET. In addition, LC impedance matching was designed using the smith chart tool and perfect matching can be ensured by measuring the characteristic impedance of 50Ω. The simulation of proposed RF harvester circuit has achieved a maximum sensitivity of -60 dBm at 900 MHz frequency with a PCE of 57%. The maximum PCE of 70% is obtained at -39 dBm. The higher DC output voltage of 350 mV, 3.3-µA current at -25 dBm is obtained. Finally, from this simulation study, it is highly recommended that TFET is the most preferable in RF energy harvesting circuits at sub mill-watt level RF input to improve the sensitivity for maximum signal utilization and PCE. However, the performance of the TFET becomes very poor at higher value of RF dBm input, due to internal losses involved in which degrades the PCE. It will be a future research scope of work to improve the TFET rectifier performances at a higher value of dBm input (more than milli-watt level) for harvesting. To achieve an energy efficient switching of TFET, still more research work is required to improve its tunneling rate.

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