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Research paper



A low pass filter based integrator in a digital feedback loop AGC for WLAN receivers

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Abstract

This paper describes a Digital feedback loop automatic gain control (AGC) for Wireless Local Area Network (WLAN) receivers. The proposed AGC employs a novel lowpass filter-based integrator for the gain generation, which controls digital multiplier to maintain constant signal dynamic range. The AGC performance is analyzed for 16 and 64 Quadra-ture Amplitude Multiplexing-Orthogonal Frequency Division Multiplexing (QAM-OFDM) modulated signal with differ-ent attenuation factors under Additive White Gaussian Noise (AWGN) channel. The proposed AGC has a dynamic range of 70dB with the gain error less than ±1dB and settling time is 1.2µs. The proposed algorithm is validated on a Field Programmable Gate Array (FPGA) platform.

Keywords: *Automatic Gain Control; Quadrature Amplitude Multiplexing; Wireless Local Area Network; Feedback AGC.*

1. Introduction

The AGC is an essential block in WLAN receivers to maintain the constant dynamic range of the received signal. There are different standards for wireless communications such as 802.11a/b/g standards, which operates over different capacity and range of coverage for wireless access. Most of these communication standards use OFDM modulation to employ high data rates in the multipath channel environment. In WLAN protocol, each received data packet consists of a preamble, header and data segments. The preamble consists of ten short training symbols of 0.8 µs and two long training symbols of 4µs each. During the preamble duration, AGC must amplify or attenuate incoming signal without altering its envelope. WLAN modem employs M-ary QAM-OFDM modulation technique, in which the message is coded in both amplitude and phase of the carrier signal. This short preamble time which arrives in burst communication mode poses a challenge in AGC response.

There have been several research contributions that provide AGC algorithms and discussed the implementation issues. In [1][5][7] a single stage Digital AGC is proposed to control the gain of coarse Programmable Gain Amplifier (PGA) [6] and fine Low Noise Amplifier (LNA) with the help of Digital to Analog Converter for full band cable receiver application. In [2][8][10] a feedback digital AGC algorithm, which controls the update moment of AGC by the feedback of acquisition and tracking state to eliminate the effect of amplitude fluctuation in DSSS receiver, is proposed. In [4-6] presented a new feedback analog AGC algorithm using switched coarse gain steps, followed by an analog open-loop fine gain step to set the gain of VGAs for WLAN receiver. In these papers, a separate AGC for coarse and fine gain adjustments are discussed, which results in hardware complexity and results are provided without considering hardware implementation constraints. In analog AGC, the presence of R-C components in energy estimator will affect loop gain and settling time. Hence analog AGC loop [11-14] will limit the performance of digital burst modes communication protocol-based receivers such as Bluetooth and WLAN applications.

This work focuses on the design and analysis of Digital AGC algorithm for QAM-OFDM modulation technique for 802.11b receivers with operating frequency band 2.4GHz. The proposed architecture has a feedback loop with low pass filter-based integrator for adaptive gain control. The AGC has a dynamic gain range of 70dB with gain steps of 1dB. The algorithm is simulated on MATLAB-SIMULINK by considering M-ary QAM-OFDM signal with attenuation factors of 20dB, 40dB and 60dB under AWGN channel. The algorithm is validated on FPGA platform in fixed point notation for a 16 and 64-QAM signals. The results are evaluated in terms of Error Vector Magnitude (EVM) by considering QAM constellation under different attenuation factors.

The paper organization is as follows. In section 2, the design of Digital AGC for WLAN Receiver is illustrated. In section 3, the design of low pass filter for feedback loop AGC is discussed. In section 4, Simulation Results of Proposed AGC is presented and carried out performance evaluation. In section 5 hardware implementation results for proposed AGC is shown and in section 7, a few conclusions on this paper is illustrated.

2. Design of digital automatic gain control

Presence of the communication channel leads to amplitude variations in a signal at the receivers. Fig.1 illustrates the energy constellation plot of the received QAM samples. The constellation point (3, 3) and (1, 1) is having an energy of 9 and 1 respectively. The energy level 1 and 9 are away from the AGC reference value 5. AGC must perform suitable amplitude correction on these energy levels 1and 9 with respect to AGC reference value, before sending to a demodulator for error-free demodulation of data.

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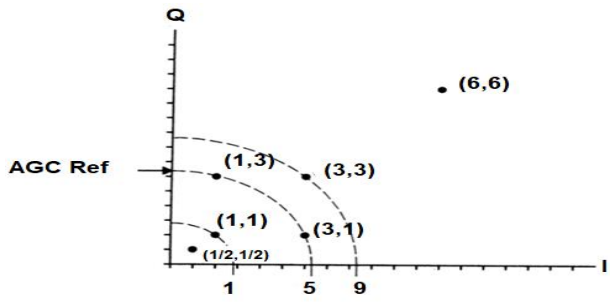


Fig. 1: Signal Energy Constellation Diagram.

In QAM-OFDM signal, digital bits are encoded into amplitude and phase of the carrier signal. AGC at the receiver must keep received signal at a constant level without changing its message envelope. The important block of the Digital AGC is Multiplier, which amplifies the incoming signal based on gain provided by AGC loop. The presence of multiplier will introduce amplitude modulation (AM) effect at the AGC output, which has not been considered by previously mentioned contributions. To minimize this AM effect, a novel Digital feedback AGC algorithm with lowpass filter-based integrator is proposed as shown in Fig. 2.

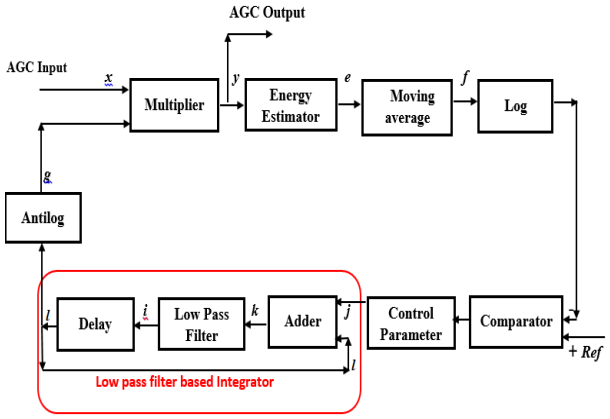


Fig. 2: Proposed Architecture of Proposed Digital AGC for WLAN Architecture.

x[n] is AGC [15] input sample multiplied with its corresponding gain sample g[n] to produce AGC output sample y[n + 1]. Where ncorresponds to received signal sample index. In this work we are considering multiplier as amplifier in digital domain.

$$y[n+1] = x[n] * g[n] \tag{1}$$

Energy e[n] of the AGC output sample is computed as

$$e[n] = (\mathrm{Re}(y[n]))^2 + (\mathrm{Imag}(y[n]))^2 \tag{2}$$

Where Re(y([n])) is in phase component and Imag(y[n])) is Quadrature Phase component of the received QAM sample. To avoid abrupt variations in e[n] we are employing moving average f[n] of energy samples. The Moving averagef[n] of the energy is computed as

$$f[n] = \left(\frac{1}{k}\right) \sum_{s=0}^{k} (e_s[n]) \tag{3}$$

Where k=16, k is the moving average window length of the energy samples. The averaged energy value is compared with AGC Ref=0.5V value and multiplied with control parameter (step size) value $\alpha = 0.1$, α value is AGC gain steps, hence α must be selected by considering settling time of AGC loop and EVM of AGC output constellation. Output of the control parameter is described as

$$j[n] = \alpha * (\mathrm{Ref} - \log(f[n])) \tag{4}$$

The output of the control parameter block j[n] is fed to a novel low pass filter-based integrator to produce AGC gain g[n].

$$k[n] = l[n] + j[n] \tag{5}$$

$$l[n] = k[n] * h[n] \tag{6}$$

$$g[n] = \exp(l[n-1]) \tag{7}$$

g[n] is the delayed version of the lowpass filter output l[n]. h[n] is the impulse response of the low pass filter.

3. Design of digital low pass filter for DAGC

Low pass filter has normalized passband frequency of $F_p = 0.002$ and normalized stopband frequency of $F_s = 0.55$, order of the filter N=1, with passband ripple $\Omega_p = 1$dB and with direct form-1 filter structure. The digital low pass filter is designed and analyzed using Filter Visualization (FV) tool of Simulink. The magnitude response of the digital lowpass filter is as shown in the below Fig. 3 and phase response is shown in Fig. 4. The digital low pass filter is iteration-based design, considering AGC loop settling time and % EVM of the QAM constellation as a highest priority. The tarnsfer function of low pass filter in feedback loop DAGC is given by

$$H = \frac{(0.006136Z^2 + 0.006136Z + 1.362\mathrm{x}10^{-4})}{(Z^2 - 0.9877Z)} \tag{8}$$

The magnitude response and phase response of the low pass filter is defecated in Fig. 3 and Fig. 4 respectively.

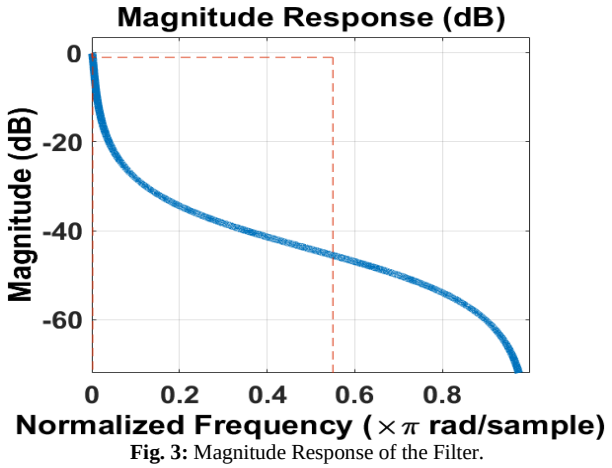


Fig. 3: Magnitude Response of the Filter.

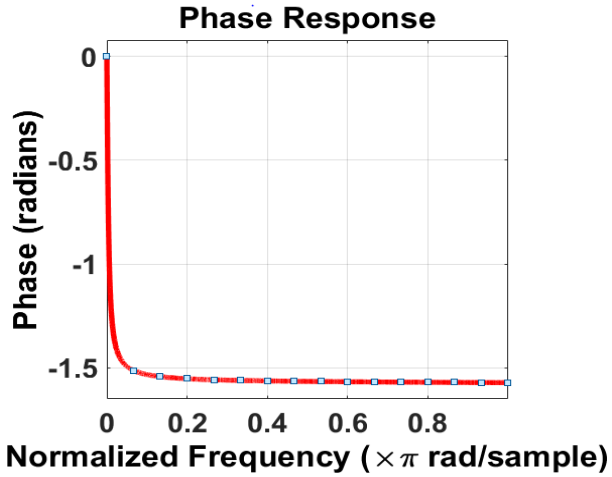


Fig. 4: The Phase Response of a Filter.

4. Analysis of the proposed DAGC

AGC is provided with 16, 64-QAM-OFDM modulated signal with 20 dB, 40 dB and 60 dB attenuation factors to evaluate the performance of the proposed AGC algorithm as shown in Fig. 5. AGC will utilize 200 samples to reach its reference voltage level and corresponding gain is plotted in Fig. 5. The AGC will alter the gain of the digital amplifier based on the incoming signal amplitude to maintain constant output. If the incoming signal amplitude is less than AGC reference value, then AGC will increase the digital amplifier gain to maintain the desired output level.

A 16-QAM-OFDM signal with amplitude with attenuation of 20 dB, 40 dB and 60 dB is applied to AGC with AGC reference value of 0.5V. AGC will compare its input n^{th} sample energy with AGC reference value to generate the corresponding gain, which is then applied to $(n + 1)^{th}$ sample. The settling time of the proposed AGC is 1.2µs. The gain steps are set to 0.5 dB by choosing the control parameter (α) value. The Transient response of the AGC, with corresponding input and gain signals are shown in Fig. 5. In the received samples, 0-300 input samples are of 60 dB attenuation, 300-750 samples are of 40 dB attenuation and 750-1000 samples are of 20 dB attenuation. AGC will generate the gain signal by comparing incoming signal amplitude with its reference value by using sample-based approach. The 60 dB attenuated signal needs amplification gain of 20(13 dB) to settle to its reference value, 40 dB attenuated signal needs the gain of 5(7 dB) and 20 dB attenuated signal needs the gain of 2(3 dB) as shown in Fig. 5.

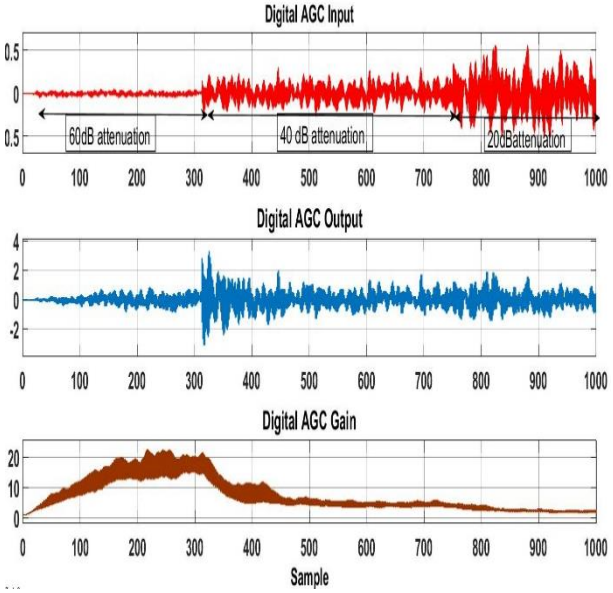


Fig. 5: Transient Response of AGC with 16-QAM-OFDM Signal.

The 64-QAM attenuated signal which is of range 0.08V is fed to AGC, the constellation plot of the signal is shown in Fig. 6. AGC must compensate the attenuations on a received signal and amplify the applied 64-QAM signal. AGC must perform this task without altering the scale of the constellation by restricting an Error Vector Magnitude (EVM) to 10% for error free QAM demodulation as shown in Fig. 7a. The Proposed AGC amplifies the 64-QAM signal by maintaining the 10% EVM compared to conventional Digital AGC as shown in Fig. 7b.

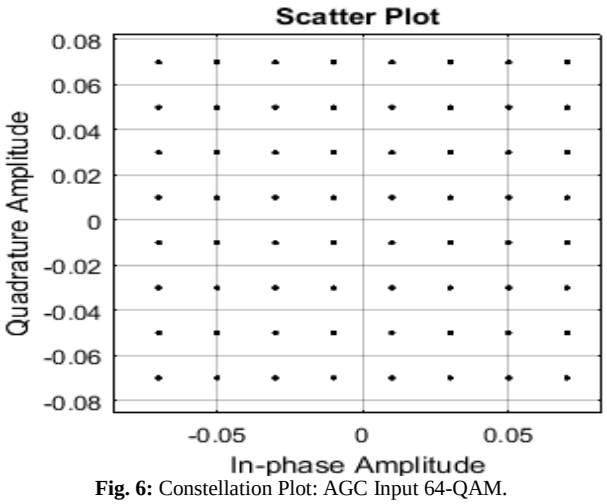


Fig. 6: Constellation Plot: AGC Input 64-QAM.

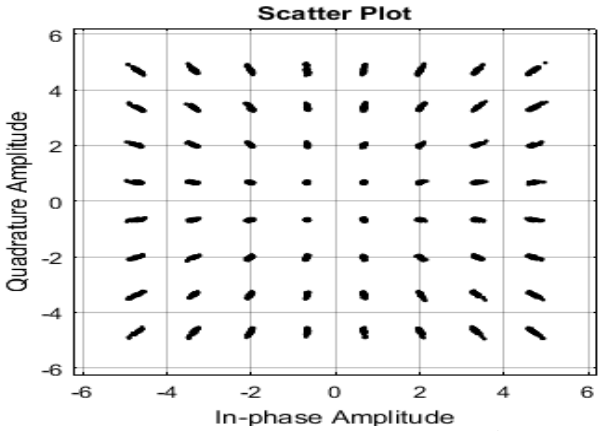


Fig. 7: A) Constellation Plot: Proposed Digital AGC Output for A 64-QAM Signal.

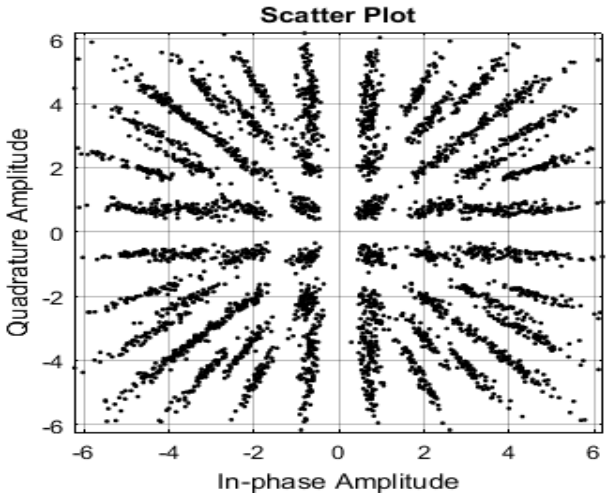


Fig. 7: B) Constellation Plot: Conventional Digital AGC Output for A 64-QAM Signal.

The proposed AGC algorithm is also validated for adaptive modulation technique-based signal by considering, 16-QAM-OFDM and 64-QAM-OFDM signal with an attenuation factor of 60 dB and 40 dB respectively, as shown in Fig. 8. The AGC will maintain output signal at the constant amplitude despite a change in modulation scheme and attenuation factor, hence the proposed AGC is suitable for adaptive modulation-based WLAN receivers.

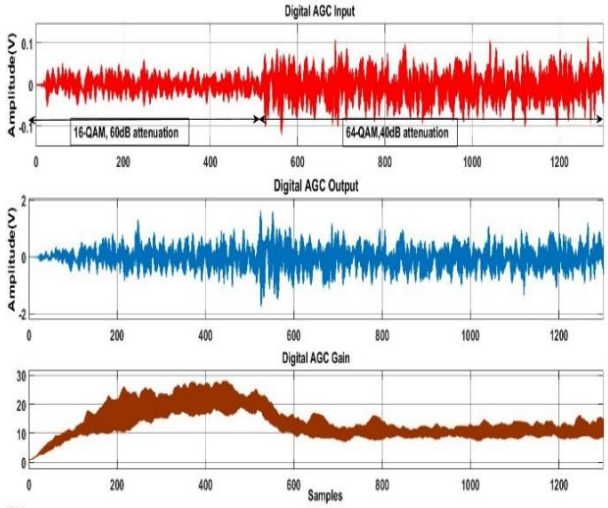


Fig. 8: Transient Response of the AGC for Adaptive Modulation-Based Signal.

5. Experimental results for proposed DAGC

Proposed AGC algorithm results are validated on Kintex-7 FPGA development board. The algorithm is implemented in fixed data point notation on FPGA with the help of a system generator tool. The in-phase(data_real) data v/s quadrature phase(data_iimag) data represented in data v/s data mode. The 40 dB attenuated 16-QAM signal take the range from -40000 to +40000 in fixed point notation as shown in constellation plot at Fig. 9. The constellation diagram in Fig. 9 indicates the state transition from one symbol point to another symbol point. The AGC has to follow these transition between the data symbol point while changing the gain of the incoming signal by maintaining the scale of the constellation. The AGC output constellation plot is shown in Fig.10, whose scale has changed to -70000 to + 70000 after the amplification of the QAM signal.

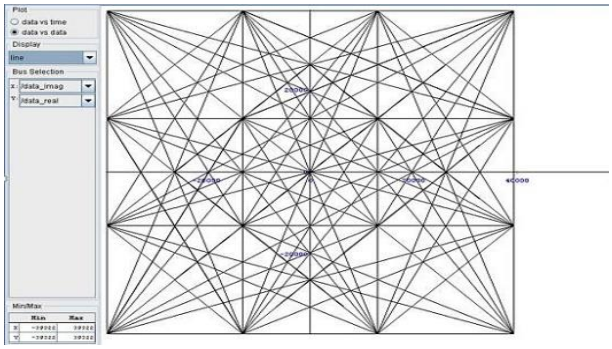


Fig. 9: AGC Input 16-QAM Constellation on Hardware in Chipscope Bus Plot.

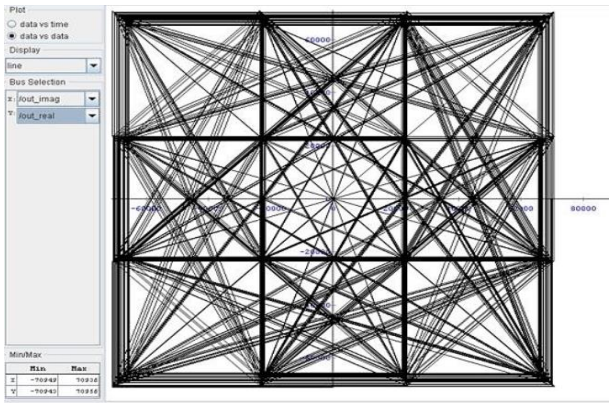


Fig. 10: AGC Output 16-QAM Constellation on Hardware in Chip Scope Bus Plot.

AGC input signal with two attenuation factors is shown below Fig.11, in data v/s time format and its corresponding AGC output is shown in Fig. 12. The proposed AGC algorithm is validated for signal under the presence of AWGN channel with different Signal to Noise (SNR). The attenuated signal constellation of 16-QAM with 20 dB SNR will fall between the scale of 7500 as shown in Fig. 13. AGC will calculate and increase the strength of the QAM constellation signal, which takes the scale of 50000 as shown in Fig. 14.

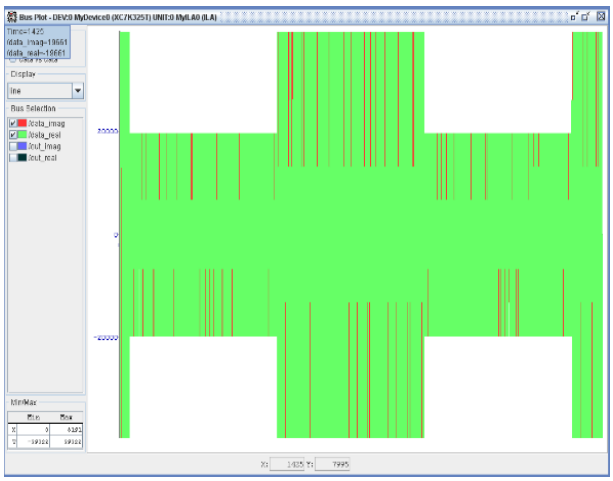


Fig. 11: AGC Input Signal on Hardware in Chip Scope Bus Plot in Data V/S Time Mode.

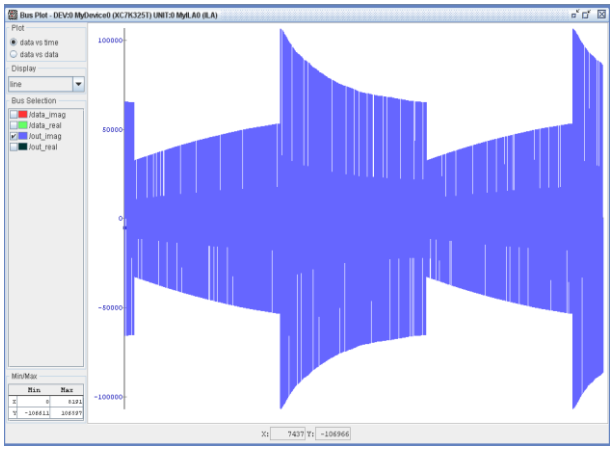


Fig. 12: AGC Output Signal on Hardware in Chip Scope Bus Plot in Data v/s Time Mode.

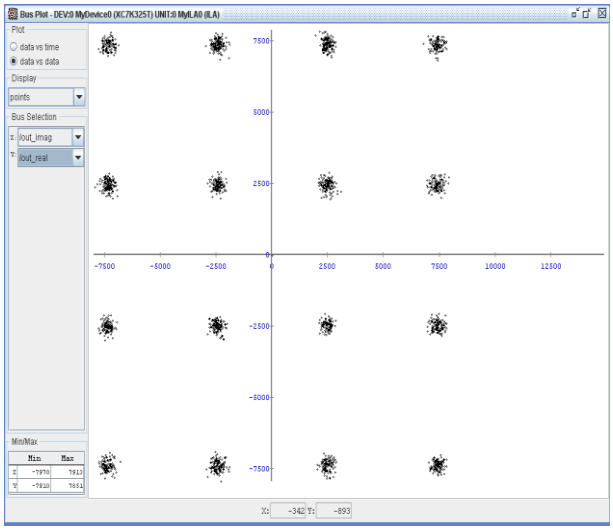


Fig. 13: AGC Output16-QAM Constellation with SNR 20 Db on Hardware in Chip Scope Bus Plot in Data v/s Data Mode.

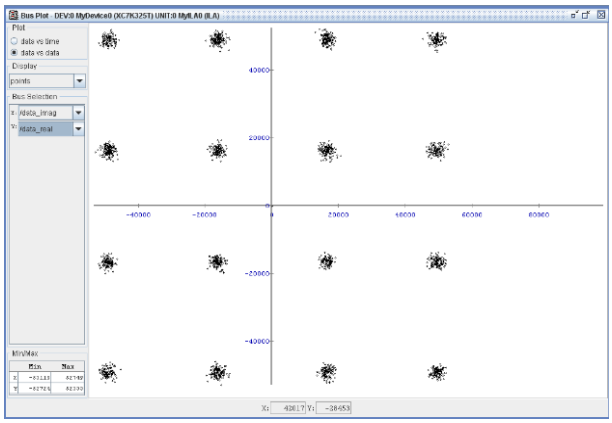


Fig. 14: AGC Output 16-QAM Constellation with SNR 20 Db on Hardware in Chip Scope Bus Plot in Data v/s Data Mode.

6. Conclusion

This paper presents a wide dynamic range low pass filter-based integrator in digital AGC loop for WLAN receivers. The proposed feedback Digital AGC has a dynamic range of 70dB with a gain error less than ± 1dB which meet the requirement of WLAN receivers. A novel AGC algorithm with a lowpass filter-based integrator is used to eliminate the overshoot effects caused by conventional AGC. The design is analyzed by considering 16, 64 QAM-OFDM signals with different attenuation factors. Validation of design is also carried out on Kintex-7 FPGA platform, which yield EVM less than 10% of the loop settling time, less than 1.2µs. hence the proposed AGC is more suitable for WLAN receivers.

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