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Research paper

Low Power Bus Encoding Schemes to Minimization of Crosstalk in Vlsi Interconnects

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Abstract

Data integrity is becoming more challenging task as the technology changes scales down in the direction of Deep Sub Micron (DSM) technology. Interconnects architecture design are now measured the bottleneck in the design of Integrated Circuits. In the DSM technology, a coupling capacitance between interconnects is the foremost factor in the total wire capacitance. The combination effect (capacitance formation) dominates the utilization of energy in the run-instant on chip bus. Bus Encoding is the most commonly used technique to change the data pattern before sending data on the bus it reduces the coupling effect on the bus then cuts the power dissipation. The proposed encoding method is the condition based temporal transition data encoding technique, i.e., upper bit inversion, lower bit inversion, upper-lower bit inversion. By using this encoding techniques, it saves the power and reduces the delay.

1. Introduction

In 1976 onwards the design engineers are working on VLSI they concentrated on the optimization of the circuit to reduce the complexity of circuit ,to reduce the number of gates in the given design, how much power dissipation and how much delay reduced ,they have proper planning about the architecture of the design , no thought of about the interconnects of the circuit, no planning about the architecture of the interconnecting devices like, bridges, buffers, decoders and wires.

According to ITRS survey [1] Communication architecture consumes up to 50% of the total on chip power and the communication architecture design in today's complex systems significantly affects the performance, power, cost and time to market. The main causes power consumption in interconnects buses are formation capacitance, they are self capacitance between the metal wire and substrate and coupling capacitance between two and more than two metal layers i.e. called crosstalk[2]. The reasons for capacitance formation is the transmitted data on bus changing dynamically changing from one's to zeros and zero's to one's. If we control these dynamic changes like reduce the number of one's and also avoiding the forbidden transitions (101,010) then only reduce the power of the interconnects. The total power consumption given as

$$P_{DYNAMIC}=\sum T\alpha.V^2_{DD}.f.C_L$$

Where $T\alpha$ is the transition activity factor

$T\alpha = \alpha s+\alpha c$

αs =Self transition activity

α c =Coupling transition activity

different ways of the crosstalk controlling techniques are developed in interconnection of the buses they are [3] i) Insertion of the repeaters ii) Insertion of the shielding between the adjacent wires iii) Minimizing spacing in between the signals lines and ground lines iv) Separating the clocks and critical signals from other lines v) Introduction to planned delay among coupled signal transmission vi) Bus encoding methods. In this paper we proposed a new bus encoding technique i.e. lower - upper bit inversion to reduce the coupling capacitance more over to reduce the power dissipation of the interconnection of the bus. The number of ways of encoding algorithms are developed. Classification of the bus encoding techniques are discussed and comparison of different algorithms are in detail [4]. Compare to other encoding techniques like BI,TO,LWC etc. The proposed algorithm had a more power saving but it is more circuit complexity. The Organization of this paper section ii overview of the different encoding techniques. section iii methodology of the proposed encoding technique. section iv result and discussion and finally conclusion.

2. Over view

In this section discuss about the different data encoding techniques related to control the dynamic changes of the data to reduce the existing capacitance between two conducting layers and metal to substrate. The function of the encoder is to transform the data from dynamic changing to gradual changing data as well as to reduce the number of transitions (to reduce the number of one's). Bus

invert(BI) is the basic encoding technique [5]used in data bus, in this method comparison between the previous encoded data with present data the hamming distance is greater than half of the bus width then invert the present data to indicate with one control signal for easily recovered at receiver. T0 is the another encoding technique[6] used in the addresses bus coding, comparison between previous coded data and present data the difference is +1 by present data by using the additional wire to freeze the present data as previous encoded data.

Limited weight code(LWC) is the commonly used method[7] to reduce the forbidden patterns in the bus, in this method dynamic transitions are converted into smooth transitions bus the size of the bus increases.NAT encoding is the best example in LWC[8]. Codebook based encoding, this is also example of the LWC. The code book [9]contains the limited weight codes for corresponding input. LWC is found fo given input i.e. hit, if not found i.e. miss. Dictionary based[10] encoding is maintaining the previous input data as the dictionary. present data is xor'ed with the all dictionary based data. Which one having the lowest hamming distance is send on the bus. Fibonacci series encoding[11] is one of the weight based method. While comparison between the binary series pattern and Fibonacci series pattern the number of transition changes are less in Fibonacci series and forbidden patterns are prohibited. S2AP (summation based subtracted added penultimate) is the recently developed weight based encoding technique[12], is also same as Fibonacci series but it is simple and efficient and less chances of coupling capacitance development patterns.

TPTM (two phase transfer method) this is delay based encoding technique[13] , before sending the data find that which couple of channels are suffering from capacitance and force to apply the delay in nanoseconds at one channel, the drawback of the is technique is applying delay and it's offer less capacitance. EVEN-ODD is the simple encoding method[13], comparison between the previous coded data and present data with different inversions i.e. even bit inversion, odd bit inversion, full inversion, no inversion, and select the which inversion having the lowest hamming distance and send out to the bus adding with control signals to easily recovered at the receiver.

3. Encoding Techniques

The main objective of the proposed encoding scheme is to decrease the number of self and coupling transitions of the given data as well as to reduce the self capacitance and coupling capacitance and further reduce the power and delay of the interconnects in DSM technology. The proposed encoding methods are divided into three schemes these are simple and easy to implement in FPGA kit, they are
scheme I: Lower bit inversion
scheme II: Upper-lower bit inversion
scheme III: Upper bit inversion

The dynamic power of the interconnection(bus) depends on the transition activity of the bus. While changing the transitions, the power also changes so, and we need to control the number of transitions on the bus. The dynamic power can be given as follows:

$P_{DYNAMIC} = \sum T_\alpha . V^2_{DD} . f . C_L$ **-----1**

T_α = transition activity factor is a weighted sum of different transition activity.

$T_\alpha = K_1T_1 + K_2T_2 + K_3T_3 + K_4T_4$-----2

Where Ti is the average number of type i transition, and Ki is its corresponding weight.
For research work, we consider only type I and type II transition reduction techniques $K_1=1$, $K_2=2$, and $K_3=K_4=0$. For every scheme comparison between the previous line (t-1) and present line (t), and perform the upper, lower, upper-lower operations and send the corresponding control signals for recovery easily at the decoder.

Scheme I
In this section, we focus on decreasing the switching activity of the type I and type II and converting them to type III, type IV and type I. if data is lower inverted, the dynamic power is
$P' \alpha (K_1T'_1 + K_2T'_2 + K_3T'_3 + K_4T'_4) + T'_{0\ to\ 1}$. ------3
Where Ti' coupling transition activity, T ' 0 to 1 self- transition activity. The transition indicated as T_1*, T_1**, T_1*** in table converted to type II, III, IV transitions. the equation (3) can be expressed as the (neglecting the self-transition)

$P \alpha [K_1(T_2+T_3+T_4) + K_2T_1{***} + K_3T_1{*} + K_4T_1{**}]$-----4

If P > P ', it is convenient to odd invert the data before transmission to reduce the power dissipation. Finally, the condition (4) reduced to

$T_1+2T_2 > T_2+T_3+T_4+2T_1{***}$-----5
$Tx = T_3+T_4+T_1{***}$

and

$Ty = T_2+T_1-T_1{***}$ ------5a

equation (5) written as

$Ty > Tx$

total transmission between adjacent lines is w-1

$Ty + Tx = w-1$

the condition for lower bit invert is

$Ty > \frac{(w-1)}{2}$ -----6

by using this condition to determine the whether the lower bit inversion to be performed or not.

Table 1. Effect of the lower bit and upper-lower bit inversion.

Time	Normal			Lower Inverted			Upper-Lower Inverted		
	Type I			Type II,III, and IV			Type I		
t-1	00,11	00,11,01,10	01,01	00,11	00,11,01,10	01,10	00,11	00,11,01,10	01,10
t	10,01	01,10,00,11	11,00	11,00	00,11,01,10	10,01	01,10	10,01,11,00	00,11
	T1*	T1**	T1***	Type III	Type IV	Type II	Type I	Type I	Type I
		Type II			Type I			Type IV	

t-1		01,10			01,10			01,10	
t		10,01			11,00			01,10	
		Type III			Type I			Type IV	
t-1		00,11			00,11			00,11	
t		11,00			10,01			00,11	
		Type IV			Type I			Type III &II	
t-1		00,11,01,10			00,11,01,10			00,11,01,10	
t		00,11,01,10			01,10,00,11			11,11,10,01	

Scheme II

In this scheme II, we use the scheme I along with upper-lower bit inversion. The upper-lower inversion the Type II transition convert them to Type IV transitions. P, P ', P " is the power dissipation of the no inversion and lower bit inversion, upper-lower bit inversion. The lower bit inversion leads to power reduction when P ' < P" and P ' < P.

The condition for P ' < P is already derived in scheme I, and P ' < P " as

$T_2+T_3+T_4+2T_1*** < T_1+2T_4**$

$T_2-2T_4** < T_1-T_3-T_4-2T_1$

$< T_1-T_x-T_1***$

add T_2 both sides

$2T_2 - 2T_4** < T_1 +T_2 -T_1***- W+1+Ty$

$2(T_2-T_4**) < 2Ty-W+1$.-----7

the conditions for lower bit inversion as eq (6),(7)

$2(T_2-T_4**) < 2Ty-W+1,\ Ty > \frac{(w-1)}{2}$ -----7a

similarly the condition for full inversion are P" < P and P" < P ' , P " is given as

$P " \alpha T_1 +2T_4**$

$2(T_2-T_4**) < 2Ty-W+1, T_2-T_4**$ -----8

Scheme III

In this scheme III, we use scheme II along with upper bit inversion. The lower bit inversion converts some of Type I (T1***) transitions to Type II transitions. Therefore, the upper bit inversion may reduce the power dissipation as well. Let P ', P", P"' are the power dissipation of the lower bit inversion, upper-lower bit inversion, upper bit inversion respectively. The conditions for upper bit inversion as P "' < P, P"' < P ', P"' < P" .

The condition P "' < P as

$T_1+2T_2 > T_2+T_3+T_4+2T_1*$ -----9

$Tz=T_2+T_1-T_1*$ -----9a

$Tz > \frac{(w-1)}{2}$ -----9b

similarly the condition for P"' < P ' as

$T_2+T_3+T_4+2T_1* < T_2+T_3+T_4+2T_1**$ -----10

Tz > Ty.----10a

and the condition P"' < P" as

$T_2+T_3+T_4+2T_1* < T_1+2T_4**$ -----11

define $T_P =T_3+T_4+T_1*$

Total transmission between adjacent lines is w-1 ,and equation (9a), and hence

$Tz+Tp=W-1$-----12

equation (11) becomes

$2(T_2-T_4**) < 2 Tz - W +1$.-----13

The upper bit inversion leads to power reduction when P "' < P, P"' < P ', P"' < P". based on (9b), (10a),(13).

$Tz > \frac{(w-1)}{2}$, Tz > Ty, $2(T_2-T_4**) < 2 Tz - W +1$. -----14

The upper-lower bit inversion leads to power reduction when P " < P, P" < P ', P" < P"'. based on equation (8),(13).

$2(T_2-T_4**) > 2Ty-W+1,\ T_2-T_4**$, $2(T_2-T_4**) < 2 Tz - W +1$. --15

The lower bit inversion leads to power reduction when P ' < P, P ' < P ", P ' < P" based on the equation (7a), (10a).

using the equation (5a) and (9a) we can rewrite the equation (10) as

$2(T_2-T_4**) < 2Ty-W+1,\ Ty > \frac{(w-1)}{2}$, Tz > Ty ---------16

when none of the equation (14),(15),(16) is satisfied ,no inversion will performed

Table 2. Effect of the upper bit inversion

Time	Normal			Upper Inverted		
	Type I			Type II,III, and IV		
t-1	01,10	00,11,01,10	00,11	01,10	00,11,01,10	00,11
t	00,11	10,01,11,00	01,10	10,01	00,11,01,10	11,00
	T1*	T1**	T1***	Type II	Type IV	Type III
		Type II			Type I	
t-1		01,10			01,10	
t		10,01			00,11	
		Type III			Type I	
t-1		00,11			00,11	
t		11,00			01,10	
		Type IV			Type I	
t-1		00,11,01,10			00,11,01,10	
t		00,11,01,10			10,01,11,00	

4. Experimental Result:

In this section, we present the experimental result of upper-lower bit inversion techniques applied to reduce the self and coupling transition activity of the interconnects of the bus in DSM technology. For this analysis purpose, we consider a thousand different patterns of the input data is applied to the proposed system. By using this technique, we concentrate on to reduce the type I and type II transition echnique. These two types saving more capacitive effect compare to type III and type IV as shown in table 1 and table 2. The proposed design and execution was done in the Xilinx vivado software, by using the IP core creates the BRAM to count the number of transitions before and after passing the design, then calculate the saving the transitions, and it saves the dynamic power and reduces the delay. The implementation was done by using the Spartan 6 family FPGA and device is XC6SLX4, and the speed is -3. The design creates the overhead to the existing circuit but long run it saves more power.

In this paper, we design the 4,8,16-bit data encoder and decoder for all three schemes and the 8-bit design simple and it became complex in 16 bit the number of LUT requirements also increases when the bit number increases and the power consumption also increases, while comparing the three schemes the scheme III offers the low power and less delay. To invert the data in scheme I i.e. Lower bit inversion when the condition is satisfied equation (6).

and Scheme II i.e. Full inversion when the condition is satisfied in equation (8), otherwise no inversion occur. In scheme III it consider the three conditions i.e. upper bit inversion, lower bit inversion, full inversion compare all which one offer the lowest power it send out. To perform this experiment consider the different data patterns and apply the random data with different combinations each, and every combination calculates power and delay of the proposed schemes.

The table 3. shows applying the same data patterns to all three schemes of 4,8,16-bit the average values of the power and delay. The static power of the design is constant and the dynamic power is varying according to given input and number of transitions and total power also changing according to dynamic power changes. From the above table 3. shows the average dynamic power in scheme I is 44.65mw is reduced to 44.37mw in scheme III, the percentage of saves is 0.62% of the power comparison of both the schemes. The average delay decreased from 16 ns to 12.1ns. The percentage of average delay decreases to 24%. The figure 2 &3. shows the graphical representation of the how the power and delay varies with 4,8,16 bit data input of comparison of the scheme I, II, III. The scheme III circuit was having more complicated, i.e., upper, lower, all inversion but it offers the fewer transitions across the output of the encoder.

Table 3.power and delay comparison of scheme I, II, III

No. of bits/ Parameter/ Scheme		Scheme I	Scheme II	Scheme III
4-bit	Power(mW)	9.01	9.01	9
	Delay(ns)	3.4	3.4	3.2
8-bit	Power(mW)	14.41	14.4	14.37
	Delay(ns)	4.1	4.1	3.8
16-bit	Power(mW)	21.23	21.2	21
	Delay(ns)	8.9	8.9	8.1

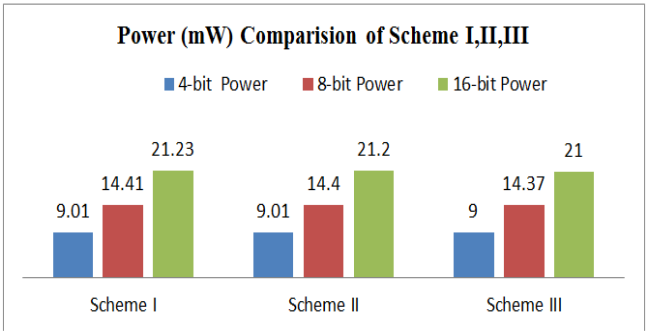

Fig 1. Power consumption of the three schemes

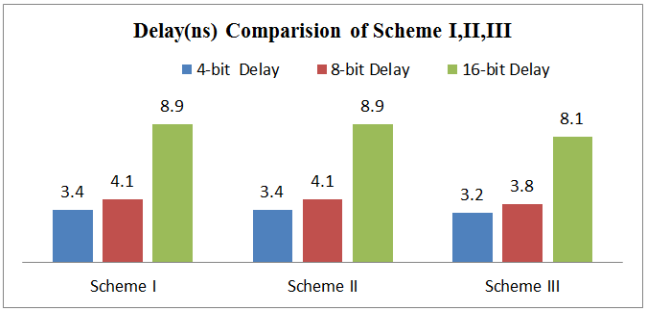

Fig 2 . Delay comparison of the three schemes

5. Conclusion

In this paper, we presented a set of new data encoding schemes aimed at decreasing the power dissipated on the system buses. As compared to the previous encoding schemes like even-odd inversion proposed in the literature, the proposed technique minimizes not only coupling transition switching but also reduces the self-transition switching. Scheme I inverts only lower bits, Scheme II inverts lower-upper bits, lower bits. Scheme III inverts lower bits, lower-upper bits, upper bits. By comparison of the all the above schemes, Scheme III saves more power and efficient encoding technique.

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