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Research paper

Performance comparison of SRAM cells in 45NM technology in the presence of a memory cell control circuit

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Abstract

Lowering power consumption and increasing the noise margin have become the two most important aspects to be considered in SRAM design. Additionally, a stable operation with good memory retention capability has gained greater importance in obtaining good yield at low-voltage and low-power SRAM designs, due to the fact that parameter variations play a major role in scaled technologies. In this paper, the 6T SRAM, 7T low power SRAM and 7T multi threshold low power SRAM designs are designed, to incorporate power gating technique. The architecture of each of the SRAM designs and their working are analyzed thoroughly. The outputs of the read, write and hold operations with transient response are observed and the power dissipation and static noise margin (SNM) of the each of the SRAM cells is calculated and compared. The paper also presents new power reduction solution through the cell control circuit which reduces the unwanted and spurious switching activities during read and writes operations. The paper demonstrates the reduction of the power con- sumption through the use of cell control circuit.

Keywords: *6T SRAM cell; 7T Multi threshold SRAM; 7T Low power SRAM; Memory Cell Control Circuit.*

1. Introduction

Due to the tremendous technological growth in data processing and data gathering equipment‟s, the information storage require- ment doubles every two years [1]. As one scales down the device channel length with lower technology nodes, the leakage current becomes a severe factor. The past few decades have been an era of the growth of handheld electronic devices which work on portable battery, which in turn make the power consumption a dominant concern. The only solution for these problems is low power opera- tion of nanometer length and efficient memory devices [2]. Tradi- tional random access memories have been divided into two major catego- ries, namely, the Dynamic Random Access Memory (DRAMs) and the Static Random Access Memory (SRAMs). DRAMs have very high packaging density because of the use of less number of de- vices, even as low as a single transistor (1T) with nodal capacitor 1C, bringing into existence the 1T1C struc- ture. However, due to the dynamic nature of the cell, one needs to refresh the memory cell every time it is read. On other hand, an SRAM cell uses a pair of cross-coupled inverters to store the one bit information and its com- plement in the nodal junctions [3]. Semiconductor memories have now become an integral and in- surmountable component of every SoC that the memory manage- ment and memory organization are of very critical concern in enhancing any system design. Fig. 1 shows the general architec- ture of a memory system. The control unit directs the operation of the row and column decoders so that the memory cell is addressed for read/write operations as required. According to the address specifications, the row and column decod- ers select the particularcell. Write driver and sense amplifiers are the additional peripheral circuitries needed for write and read oper- ations from and into the memory cell. This paper is organized as follows. Section II ex- plains the operation of a conventional SRAM cell (6T SRAM cell). Section III elaborates the 7T SRAM cell op- eration. Section IV elaborates the low power multi threshold 7T SRAM cell and Section V presents the simulation results and infer- ences. Section VI details the role of external circuits used for read write opera- tions and Section VII concludes

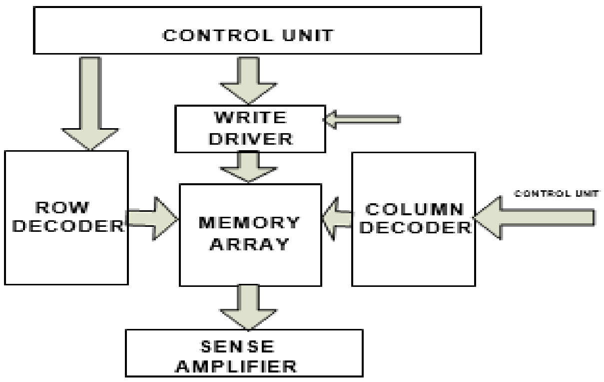

Fig. 1: General Memory Architecture

2. Conventional SRAM cell (6t SRAM cell)

As the name suggests, conventional SRAM cell is designed using 6 transistors normally with two transistors acting as access transis- tors and the remaining 4 transistors (two each of PMOS and NMOS devices) constituting a pair of cross coupled inverter. The cross cou- pled inverters reinstate the bit value as long as the power supply is applied to the memory cell. Fig. 2 shows the basic 6T SRAM cell. WBLB (BL) and WORDLINE (WL) are the com- mand signals employed to control the Read, Write and Hold oper- ations of the memory.

Write operation: Normally, the word line WL of the selected cell is at ground in order to turn off the access transistors. The appropriate value of data is asserted in the BL and BLB lines before the WL line is activated with the WL signal. Once data is stable on BL and BLB line, the WL line is connected to the logic high level for a certain time as required for the memory array. A WL pulse to
the access transistors (NMOS2 and NMOS3) switches ON the devices thus making them act as closed switches. In other words, the access transistors pass the value of BL and BLB to the cross coupled inverters and the data is stored into the cell.
Hold Operation: During the state of Hold process, the supply line remains connected to the cell to maintain the data into the cell through the appropriate load PMOS device as decided by the data in the memory nodes. The WL line is applied with ground potential as a result of which, both the access transistors become off acting as an OFF switch to the BL and BLB lines. In effect, the output of cross coupled inverters gets disconnected from the BL and BLB line and data is retained in the cell.
Read Operation: During the Read operation, with the WL line of selected cell remaining at ground potential, the BL and BLB lines are pre-charged to VDD. Then, by asserting the WL line access transistors with a pulse voltage of peak magnitude VDD, they turn ON. Assuming data 1 is stored in the left side node of the memory cell, and a 0 is stored in the right node, then asserting the WL enables the memory nodes read by the BL and BLB lines. The BL and BLB lines are connected to the sense amplifier to sense the nodal values without killing the memory data in the cell. The sense amplifier amplifies the minimum difference sensed between the memory nodes and amplifies it so that the data is read by the peripheral circuits [4-5].

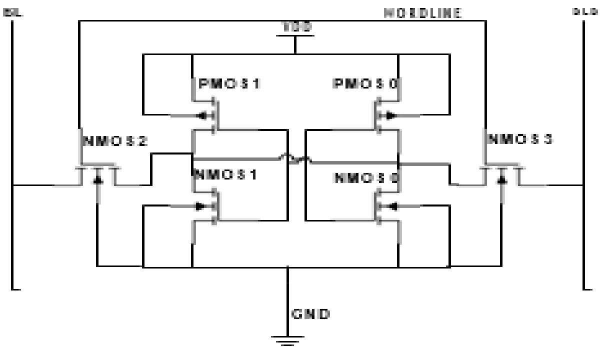

Fig. 2: Conventional 6T SRAM Cell.

3. Conventional 7T sramcell

In the standard 6T SRAM structure, the cell suffers mainly from Read and Write failures which occur due to voltage distribu- tion that occurs in the pull-up transistors with the node initially
storing a 1 attempting to discharge through the charge leakage in the vulnerable paths.

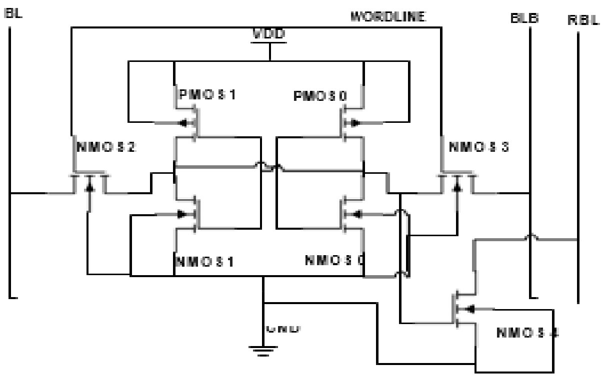

Fig. 3: 7T SRAM Cell.

This section presents the 7T SRAM cell as depicted in Fig. 3.
The major operations of the cells are as follows:

Hold Operation: The word line is made low for the hold oper- ation. If Q is holding 1, then the transistor NMOS 0 would go to ON state and transistor PMOS 0 to OFF state, so that ~Q is con- nected to ground. This would turn on PMOS 1 which cut off Q from ground. Hence, Q holds the state [1]. Similarly, the operation for holding 0 can also be explained in the same way.
Write Operation: Write operation in the 7T SRAM cell is the same as that of 6T SRAM cell. WBL/ WBLB bit line is pre- charged to the corresponding memory bit voltage level. Then, the word line is asserted. Assuming WBL is pre-charged to VDD and WBLB is connected to ground, this action will write a 1 at the node Q, irrespective of the previous state. With the Q becoming 1, the transistor NMOS 0 is turned on and ~Q is pulled down (ground). This will force PMOS 1 to turn ON into strong conduc- tion and then VDD is connected to node Q, reinstating the logic state 1. In similar lines, the write operation of [0] in Q node is also performed, with 1 written into the ~Q node.
Read Operation: For the read operation to be carried out suc- cess- fully without any harm to the stored charges, the RBL bit line is pre-charged to the VDD level. Assuming Q contains a „0", the RBL bit line will dis-charge through the NMOS 4. This can be sensed and amplified by the sense amplifier and it will enable indication of the read operation resulting in „0". If Q contains „1" then the RBL bit line will be having no path to get discharged, and hence, it remains at VDD. This indicates a read „1" operation. This will be sensed by the sense amplifier justifying read „1" operation.

4. Low power 7t multi thresh-old SRAM cell

The structure of a low power 7T multi threshold SRAM cell is basically a latch, with two inverters connected back to back (constituted by NMOS 0, PMOS 0, NMOS 1 and PMOS 1). The design employs the stacking effect. The tail or the footer transistor NMOS 5 is used to reduce the static power dissipation at the time of read and ideal state. NMOS 2 and NMOS 3 are responsible for the write operation and NMOS 4 is high threshold voltage NMOS transistor. Power gating technique is used in this design so that the tail transistor NMOS 5 is not the part of bit cell. It is commonly used for the entire row of the SRAM bit cells. This results in Fine grain structure or coarse grain structure. The length of all transistors has been made to be the standard length 45nm of the technology node employed in all the designs. Fig. 4 shows the arrangement of the 7T Multi threshold SRAM cell [5].
The design has separate write and read bit lines and transistor is connected in series. It acts as 2T buffer with transistor NMOS 4 for read operation and also reduces the static power dissipation. Bit cell is cut off from the ground during the write operation. This will further reduce the power dissipation [6].

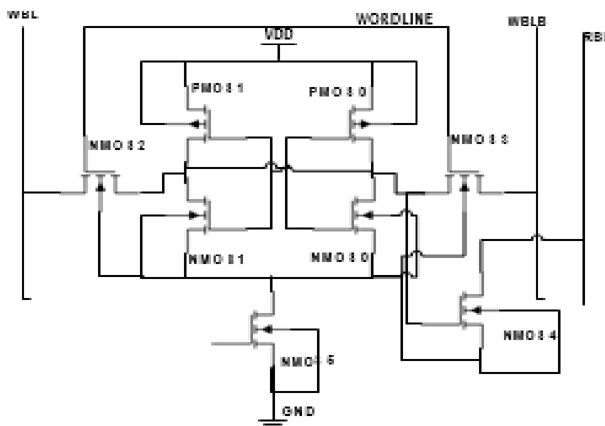

Fig. 4: 7T Low Power Multi Threshold SRAM Cell.

Hold Operation: For hold operation to perform the word line is made low and the chip select is made high. If Q is in the state 1, then transistor NMOS 0 would be on and transistor PMOS 0 would be off and hence ~Q is connected to the ground. This would turn on

PMOS 1 which cut off Q from ground. Hence 1 is main- tained at Q. the operation for holding the state 0 can also be ex- plained in the same way as above.

Write Operation: Write operation of 7T Multi-threshold SRAM cell is same as that of 6T SRAM. Both the bit lines WBL and WBLB are pre-charged to corresponding values and then the word line is emphasized. WBL is pre-charged to VDD and WBLB is connected to ground, to write [1] at Q which already has a 0 state stored. When the word line is emphasized transistor NMOS 0 is turned on and ~Q is pulled down (ground). Which force PMOS 1 to turn ON and then VDD is transferred to Q. On the similar way, a write 0 operation is performed.

Read Operation: In 6T SRAM voltage gets divided between the ac- cess transistor and the pull down transistor due to which operating voltage is scaled down which causes read operation failure. In this SRAM cell design that will not be possible because of a different single ended two transistor read buffer is used for read operation. For read operation, RBL bit line is pre-charged to VDD and chip select is also made high. If Q node contains „0‟, then RBL dis- charges through NMOS 4 and NMOS 5. That is sensed by the sense amplifier and indicates a read „0‟ operation. If Q contains „1‟ then RBL bit line will have no path to get discharge so it remains at VDD and hence indicating a read „1‟ operation. This will be sensed by the sense amplifier, thus justifying the read
„1‟ operation in 7T SRAM design. Due to the connection of source terminals of pull down transistors and the drain terminal of tail tran- sistor NMOS 5, the stacking effect is generated [7]. Stacking effect due to NMOS 0, NMOS 1 and NMOS 5 results in decrease of Vgs, negative Vbs and decrease in Vds, which in consequence reduce the static power dissipation. Firstly, the Vgs of transistor NMOS 0 and NMOS 1 become negative which causes reduction is sub threshold leakage current. Secondly, the voltage Vbs of tran- sistor NMOS 0 and NMOS 1 also get reduced due to which the threshold voltage increases and subsequently the sub-threshold leakage current gets reduced [8]. Thirdly, the voltage Vds of tran- sistor NMOS 0 and NMOS 1 also get reduced, due to which the threshold voltage get increased and sub-threshold leakage current gets reduced [9]. Re- duction in power dissipation is due to the rela- tionship of sub- threshold current on the above parameters.

5. Simulation results

The noise margin can be calculated by using the swiping method [8]. The node (Q) is changed from 0 to VDD and the correspond- ing values at the other node (~Q) are used to plot the voltage transfer characteristic (VTC) curve. The same operation is repeat- ed and ~Q is changed from 0 to VDD and the corresponding Q VTC is plotted at on the same graph. These two VTC curves
forms a plot in the shape of a butterfly with two lobes as shown in the Figs. 5(a) to 5(f) Read and hold Signal to noise margin (SNM) is calculated by using the smallest square side of the two largest possible squares that can be drawn inside the two lobes of the but- terfly figures. It can be observed that the write SNM and the
Read and Hold SNM butterfly plots are different. The read and hold SNM has one square only. Write SNM is the length of the side of the largest square drawn at the bottom of butterfly plot. Fig. 6 shows the Write operation related transients while Fig. 7 depicts the Read operation related transients pertaining to the 6T SRAM cell. Fig. 8 represents the transients for 7T multi threshold SRAM cell for the Read operation. Table 1 depicts the comparison of noise margins of the SRAMs under discussion.

Write SNM: To calculate the SNM for write operation, the word write line (WWL) is made high, and signal CS is also made low. The bit lines will be pre-charged according to write 1 and 0 at the node1. The butterfly diagrams are shown below for the 6T, conven- tional 7T and 7T multi threshold SRAM for comparison.

Read SNM: Read SNM is denoted as the noise voltage that is added to the SRAM cell bit lines till the contents of the nodes Q and ~Q remain unaltered during the read operation.

Hold SNM: The amount of noise voltage that is added to SRAM cell bit cell nodes Q and ~Q, such that the data stored in the cell cannot be altered is called a read SNM. This can be taken in the lower size lobe of the curve even while keeping the maxi- mum size of square.

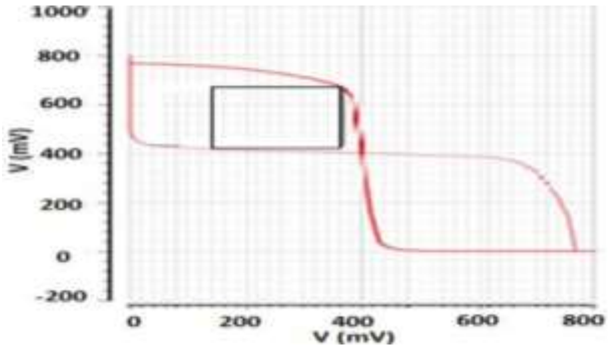

Fig. 5: A): Write SNM for 6T SRAM Cell.

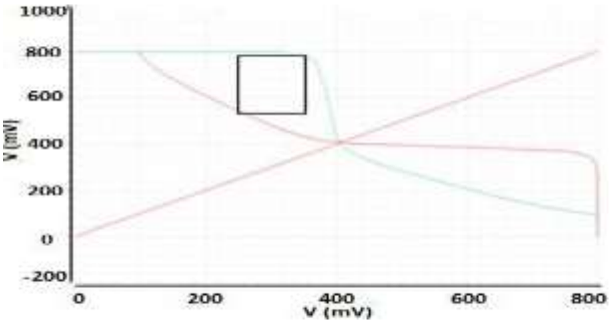

Fig. 5: B): Write SNM for 7T SRAM Cell.

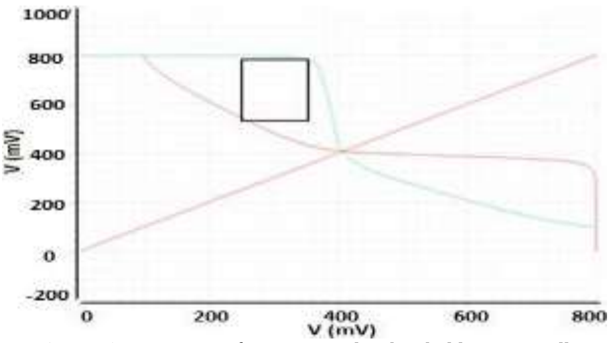

Fig. 5: C): Write SNM for 7T LP Multi Threshold SRAM Cell.

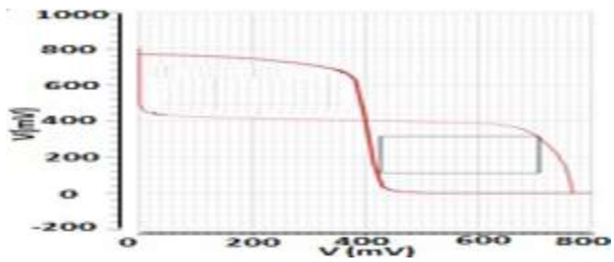

Fig. 5: D): Hold SNM for 6T SRAM Cell.

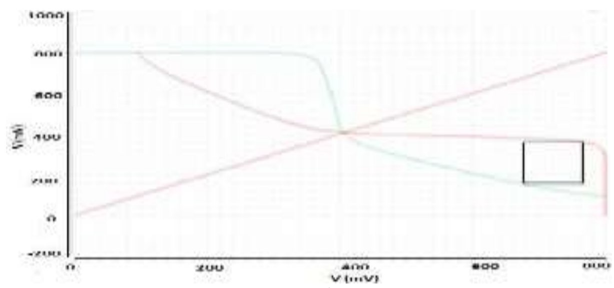

Fig. 5: E): Hold SNM for 7T SRAM Cell.

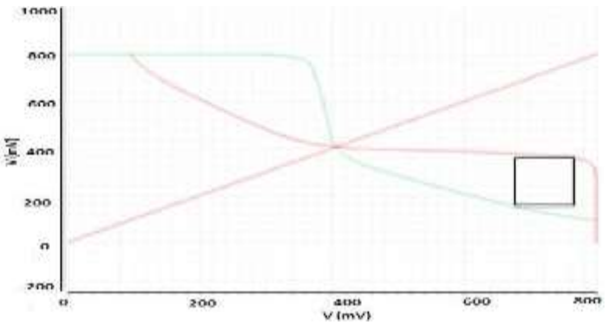

Fig. 5: F): Hold SNM for 7T Multi Threshold SRAM Cell.

Table 1: Comparison of Noise Margins of Srams

Sram Cell	Wsnm (Mv) '1'	Wsnm (Mv) '0'	Hold Snm (Mv)
6t Sram	240	240	200
7t Sram	240	230	210
7t Mt Sram	260	240	220

5.1. Transient responses of SRAM cells

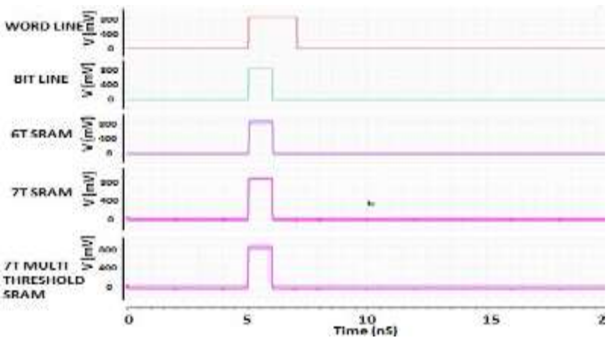

Fig. 6: Write Operation for the 6T SRAM Cell, 7T SRAM and 7T Multi Threshold SRAM.

5.1.2. Read operations

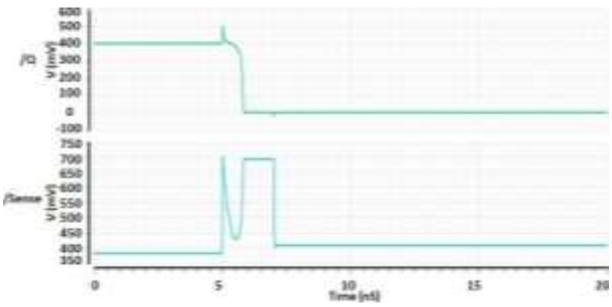

Fig. 7: Read Operation for Standard 6T SRAM Cell.

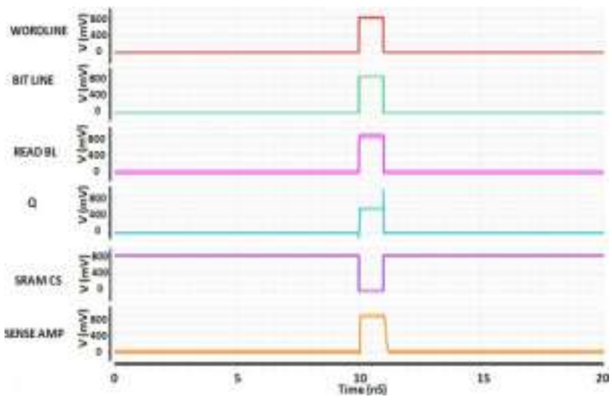

Fig. 8: Read Operation for 7T Multi Threshold SRAM Cell.

6. Power consumption

In semiconductor memory designs, the main problem is the power consumption, which is made all the more severe due to the densest possible memories of low technology mode struc- tures. The power dissipation is normally of two types, name- ly, the static and dy- namic power consumption components. The leakage power dissi- pation incurred due to the devices which are off is called the static power while the dynamic power arises due to the recurrent charge and discharge on the memory output nodes. Table 2 lists the power dissipation values incurred for the SRAM cells concerned. Table 3 de- picts the delay variation of the three types of SRAMs during the Write and Read operations.

Table 2: Power Dissipation for SRAM Cells

Sram Cell	Operation	Power Dissi- Pation
Standard 6t Sram	Read	44.23uw
	Write	35.73nw
	Hold	129.7uw
7t Conventional Sram	Read	652.8nw
	Write	28.6nw
	Hold	169.7nw
7t Multi Threshold Sram	Read	324.7pw
	Write	34.99nw
	Hold	324.5pw

Table 3: Delay Variation

Operation Performed	Standard 6t SRAM	7T SRAM	7T Multi Threshold
WRITE DE- LAY	38.11ps	28.23ps	19.99ps
READ DE-LAY	993.1fs	42.08ps	44.01ps

7. Monte carol analysis of scrams for threshold voltage in presence of temperature varia- tions

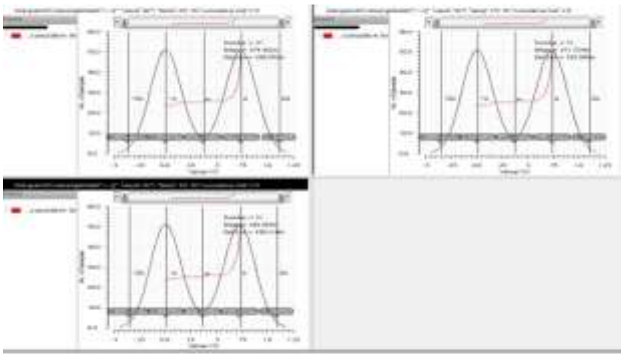
Fig. 9: 6T SRAM Cell.

The Monte-Carlo curves of temperature variations of 6T and 7T SRAM cells are given in the Fig. 9 and Fig. 10. Temperature vari- ations are taken at 22, 27 and 32 Degree Centigrade.

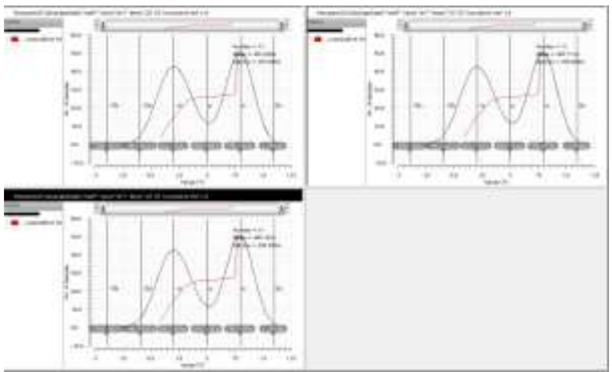
Fig. 10: 7T SRAM.

8. Peripheral circuits for cell operation

The expected and proper operation of a memory cell depends largely on the efficiency of various external circuits which are used in the process of reading from and writing into memory as explained in Fig 1.1. The sense amplifier circuits, write driver or buffer circuits, the precharging circuits, to name a few, are some of the important circuits. This paper proposes a cell control circuit as the basic circuit, which can be used in various stages of operation.

8.1. Pre-charge circuit

Pre-charge circuit is used while reading the cell data. Initially, the pre-charging is carried out with VDD con- nected so that both the transistor PMOS1 and PMOS2 are OFF. When one wishes to read the data, the pre- charge pulse node is applied with 0V which makes both the RBL and RBLB signals become high, due to the charging on the bit and bit bar line capacitances. Fig 11 depicts the pre-charge circuit employed in the process.

Recharge Pulse

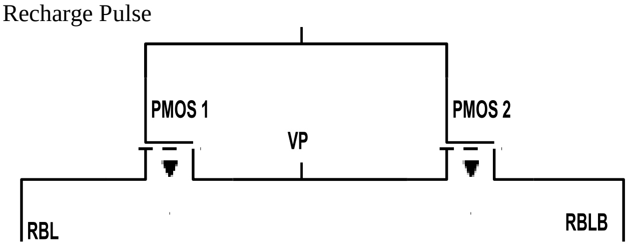

Fig. 11: Pre-Charge Circuit.

8.2. Sense amplifier

Sense amplifier is basically a differential amplifier circuit, which amplifies the differential input signal sensed across the bit and bit bar lines. In accordance to the sensed input, output is am- plified and sent to the other units of the processor. Fig. 12 shows the current mirror structured sense amplifier circuit. The devices PMOS1 and PMOS2 form the current mirror active loads of the circuit, and NMOS1 and NMOS2 are the differential input transis- tors.

8.3. Write driver circuit

The write driver circuitry is important in reducing the power dissipation of the SRAM. CS and Write signals eliminate the unnecessary switching of the NMOS1 and NMOS2. Initially CS signal is kept Low and the input data is applied to input terminal. When data is stable on the line, then the Write and CS pulses are made High. This turns ON the NMOS1 and NMOS2 according to data bit BL and BLB lines. Fig. 13 shows the Pre-charge circuit for selected cell.

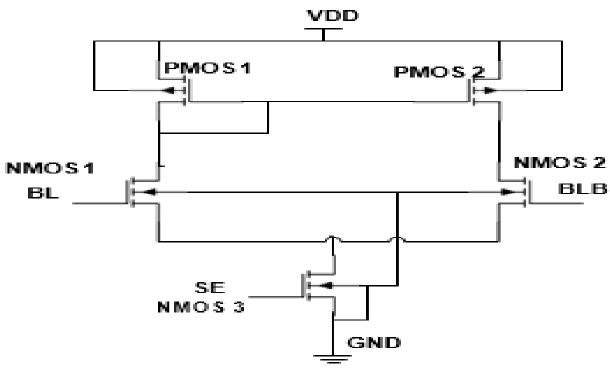

Fig. 12: Sense Amplifier.

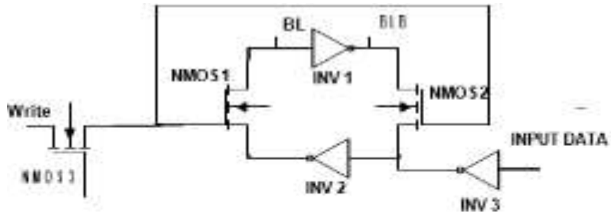

Fig. 13: Write Driver Circuit.

Table 4: Delay Variation

CS Signal	Write	Read	Operation
0	X	X	Cell not selected
1	1	0	Cell selection and Write
1	0	1	Cell selection and Read
1	0	0	Cell selection and Hold

8.4. Proposed cell control circuit

The cell control circuit is used to mainly reduce the power consumption due to the unnecessary or spurious switching of the transistors. During the write operation, CS and Write signals are asserted which 1) enable the cell select enable and write cell signals and 2) disables the read cell enable signal. During the read operation, CS and Read signals are asserted, which 1) enable the cell select enable and Read cell enable. Additionally, in order to align the delay write and read cell signals, two inverters are connected in cell select enable. Table 4 depicts the delay variation across the different states of Read and Write. During the Hold operation, only the Cell select enable signal is asserted, which provide VDD to the cell in order to retain its value. Fig. 14 shows the cell control circuit.

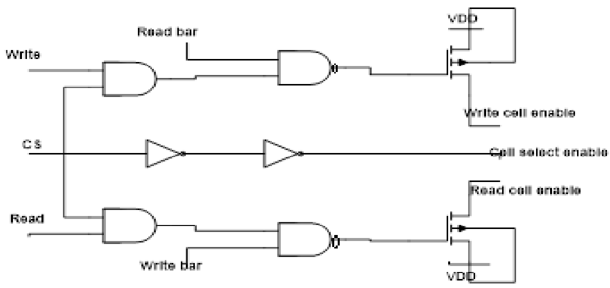

Fig. 14: Cell Control Circuit.

9. Conclusion

The paper presented the operational features and comparative advantages and demerits of the widely used 6T SARM, 7T low power SRAM and 7T multi threshold SRAM cells. Extensive performance comparison is done for realizing the SNM characteristics for the memory types concerned. It is found that the 7T Multi threshold SRAM enjoys the benefit of increased SNM values of 8.25% over the conventional 6T SRAM and 7T SRAM cell for the write operation, and for hold operation SNM of conventional 7T SRAM cell is increased by 5% and 7T Multi threshold SRAM by 10% over 6T SRAM. The power consumption characteristic study reveals that the hold and write power of 7T SRAM and 7T multi threshold SRAM is reduced by 99.8% and the write power of 7T SRAM is reduced by 21.5% as against the conventional 6T SRAM cell

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