International Journal of Engineering & Technology, 7 (4.10) (2018) 99-103

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper



Optimal Placement of Fuzzy based UPQC Topologies with Distributed Generation for Power Quality Enhancement in IEEE 14 Bus System

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Abstract

An Unified Power Quality Conditioner (UPQC), is a combination of shunt and series Active Power Filter (APF), has become a standard accepted solution in the area of current and voltage harmonics mitigation of a power system network. This paper furnishes a comparative analysis of the power quality enhancement and optimization in positioning for three different VSI based UPQC system configurations namely: 3P3W UPQC topology, 3P4W UPQC based on 2C shunt inverter topology and 3P4W UPQC based on 4L shunt inverter topology, all supported with the Fuzzy Logic Controller (FLC), placed at different locations in a standard IEEE 14 bus system. Simulation results using MATLAB/SIMULINK provides the optimal position of UPQC for mitigating the harmonic issues in the standard IEEE 14 bus system.

Keywords: *Distributed Generation (DG); Fuzzy Logic Controller (FLC); Power Quality (PQ); Unified Power Quality Conditioner (UPQC).*

1. Introduction

In the present flourishing world, life is inconceivable in the absence of usage of electricity. Hence electrical power plays an indispensable role. Besides, it is essential to maintain the uninterrupted and appreciable quality of electrical power to the end user for the efficient working of equipment. Many of the consumer end loads, mandates the distortion free, continual supply power. But, the employment of power electronic devices and the nonlinear loads in the power system causes heating, harmonics, flickers and many other disturbances which will impact the system's availability and reliability.

To alleviate the power quality issues, power quality monitoring equipment and power quality conditioners should be positioned in the distribution side to vanquish the harmonics of current and voltage signals, voltage swell, voltage sag, etc.

Rahul Virmani presented a work on the "Performance Comparison of UPQC and Active Power Filters for a Non-Linear Load". This work evidently mentioned that the bonus of enforcing the UPQC into the power system, when compared with an APF. The control algorithm is proposed to quench the harmonics, but with the requisite of increased memory space [1].

The work "A Low Cost High Performance UPQC for Current and Voltage Harmonics Compensations" carried out by Quoc-Nam Trinh along with Hong-Hee Lee from Ulsan University – Korea suggests the use of low cost, high performing UPQC devices in a power system. They further proposed that the insertion of a capacitor in succession with the shunt APF will substantially reduce the voltage across the DC link [2].

Mohammed Abdul Ahad Yahiya's work on "Performance Analysis of DVR, DSTATCOM and UPQC for Improving the Power Quality with Various Control Strategies" compares the voltage quality enrichment methods implemented using DVR, D-STATCOM and UPQC, actuated with PI controller and FLC, but are computationally rigorous due to the complex algorithm and entailment of more memory [3].

Vinod Khadkikar revealed a new comprehensive review on the different conceivable UPQC configurations for single phase and three phase networks, to enhance the PQ at the distribution level [4].

In addition to these, few accustomed solutions for PQ improvement were still controversial due to inefficient algorithms, over consumption of memory and less impact on harmonics. In order to cater this issue, there are reasonable advancements attempted in the literatures [5]-[10].

In this proposed research, the three stated UPQC topologies are implemented along with DG, implanted in different locations of an IEEE 14 bus system which are controlled with the FLC control algorithms. The simulation results, proving its effectiveness in harmonics reduction at different optimal location are presented.

The remainder of the proposed work is organized as follows. The Section 2 narrates the control strategies implemented in this research for UPQC. The detailed UPQC Configurations are given in Section 3. Contents of Section 4 present the IEEE 14 Bus system. Section 5 reports the simulation results, and the conclusion of this work is documented in the Section 6.

2. Structure of UPQC

The Fig. 1 exhibits the general structure of UPQC. It is comprehended with two 3-ϕ active voltage source inverter filters namely Series Active Filter (SAF) and Parallel Active Filter (PAF), con-

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nected in cascade with a common DC Link. The SAF is in series with the line through a transformer and operates to compensate the voltage quality problem in the line. The PAF is in shunt to the line aiming to compensate the current quality problem in the line and to regulate the DC link.

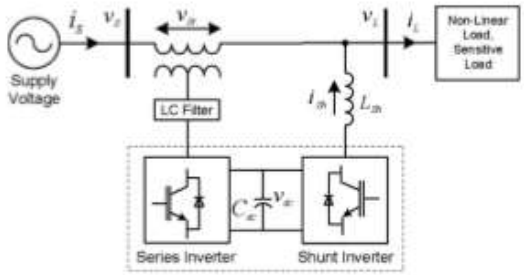


Fig. 1: The general structure of UPQC topology.

2.1. Structure of UPQC

The key idea of control strategy is to calculate and facilitate the injection of required quantity of the voltage and current signals to improvise the compensation effect in the system. To effectuate this, Fuzzy Logic Controller (FLC) is proposed in this research. The complete pattern of FLC is composed of Fuzzification, Inference engine, Defuzzification blocks.

The approach of converting input/output variable to linguistic labels is denominated as fuzzification. In the proposed paper, seven grades of linguistic labels are considered, namely: Large Positive (LP), Medium Positive (MP), Small Positive (SP), Zero (ZE), Small Negative (SN), Medium Negative (MN), Large Negative (LN) identified by membership grade are utilized, to decompose each system variable into fuzzy regions possessing the range [-1 1].

Inference Engine: The performance of the FLC, correlating the input and output variables of the system is directed by a set of rules. These rules relating the error and its rate of change are displayed in Table 1. Based on this table, 49 rules are formed and labelled as the Knowledge repository of the FLC.

Defuzzification: The fuzzy set symbolizing the controller output in linguistic labels has to be transfigured into a Crisp solution variable before it can be used to control the system. This is effectuated using a defuzzifier block.

Table 1: Fuzzy Control Rules

Error \ Rate of change of error	LP	MP	SP	ZE	SN	MN	LN
LN	ZE	SP	MP	MP	LP	LP	LP
MN	SN	ZE	SP	MP	MP	MP	LP
SN	MN	SN	ZE	SP	SP	MP	LP
ZE	MN	MN	SN	ZE	SP	MP	MP
SP	LN	MN	SN	SN	ZE	SP	MP
MP	LN	MN	MN	MN	SN	ZE	SP
LP	LN	LN	LN	MN	MN	SN	ZE

2.2. UPQC Configurations

In this section, three configurations of 3-ϕ UPQC systems, used to damp the power quality problems, are described. The Fig. 2 depicts the 3P3W VSI-based UPQC topology, feeding 3P3W load. This is the most widely used and commonly studied configuration. Apart from the three phase loads, numerous industrial plants often embraced of combined loads, having diverse of 1-ϕ loads and 3-ϕ loads, supplied by 3P4W source. The existence of fourth wire designated as the neutral conductor, stimulates an excessive neutral current flow and thus, requests additional compensation requirement. To mitigate the neutral current impact in 3P4W system a shunt inverter configuration 2C and 4L topologies has experimented as shown in the Fig. 3 and Fig. 4.

The 2C topology comprises of two split capacitors on the dc side. The midpoint of the capacitor, managed at zero potential, is employed as a connection point for the fourth wire. In 2C topology, it is necessary to maintain equal voltages across both the capacitors to circumvent the flow of circulating current. The 4L topology consists of an extra leg, providing two additional semiconductor switches, is used to nullify the load neutral current by connecting it into the fourth wire.

The equivalent electrical circuit of a conventional UPQC is represented in the Fig. 5.

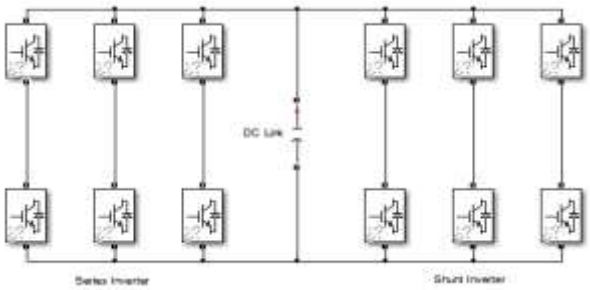


Fig. 2: 3P3W UPQC topology.

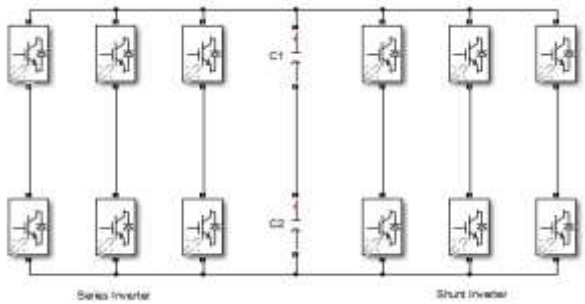


Fig. 3: 3P4W UPQC based on 2C shunt inverter topology.

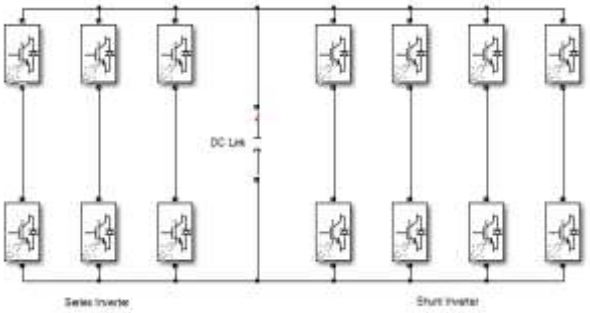


Fig. 4: 3P4W UPQC based on 4L shunt inverter topology.

The source voltage due to negative sequence currents and harmonics can be represented in (1)

$$V_s + V_{sr} = V_L \quad (1)$$

To derive the balanced sinusoidal load voltage with constant magnitude, output voltages of series active power filter is expressed as in (2)

$$V_{sr} = (V\text{-}V_{1p}) \sin(\omega t + \theta_{1p} - V_{Ln}(t) - V_k(t)) \quad (2)$$

Where,

V_s – Supply voltage

V_{sr} – Series APF voltage
V_L – Load voltage
As the shunt APF functions as a current source, to compensate the load currents in the system,

$$i_s = i_L - i_{sh}$$
$$= i_{1p} \sin(\omega t - \theta_{1p}) \cos(\Phi_{1p}) \quad (3)$$

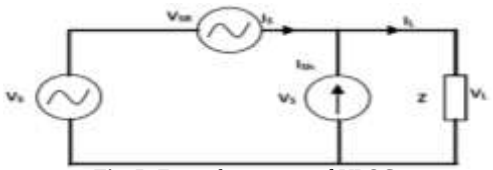


Fig. 5: Equivalent circuit of UPQC.

3. Wind Energy Generating System

The Stand-alone DG systems are typically used to supply the isolated areas or locations interconnected to a delicate grid. They unite several generation modules, typically assimilating diverse renewable energy sources. The applications of these DGs diminish the probability of energy shortage, incorporated with energy storage. The wind generation module is developed by a pitch controlled wind turbine coupled with a permanent-magnet synchronous generator (PMSG).
The power in the wind is proportional to the cube of the wind speed and it is given by the expression 4.

$$P = 0.5 * \rho * A * v_w^3 \quad (4)$$

Where, ρ is the air density (Kg/m^3), v_w is the wind speed at the center of the rotor (m/s), $A = \pi R^2$ is the frontal area of the wind turbine and R is the radius of the circumference of the blades. A wind turbine can only extract a partial quantity of power from the wind, which is bordered by the Betz limit (maximum 59%). The mechanical power extracted from the wind using a wind turbine is given by expression 5.

$$P_{wt} = 0.5 * \rho * A * v^3 * C_p(\beta, \lambda) \quad (5)$$

Where, Cp is the power coefficient of the wind turbine, followed by β as the blade pitch angle and λ as the tip speed ratio. The value of C_p is extremely non-linear and differs with the wind speed, the turbine blade parameters such as a pitch angle along with the rotator speed of the turbine.

4. IEEE 14 Bus System

A Single line diagram of the IEEE 14-Bus standard system is shown in Fig. 6 with loads presumed to be depicted by constant impedance and all generators are functioned with constant mechanical power input and with a steady excitation. It is composed of five synchronous machines supported with IEEE type-1 exciters, among which, three are synchronous compensators used dedicatedly for reactive power support and considering generator 1 taken as reference generator.

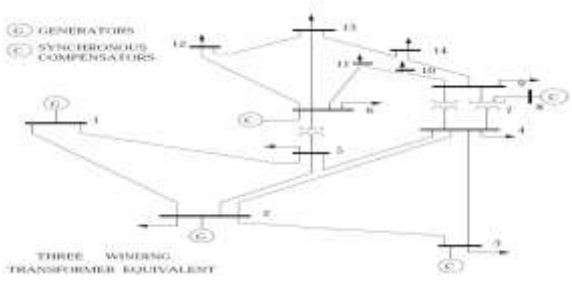


Fig. 6: IEEE 14 bus test system.

5. Results and Discussion

To enable the comparative harmonic analysis of the three stated UPQC configurations along with its influence of DG, the proposed UPQC models are constructed in the MATLAB/SIMULINK environment. The Fig. 7 shows the proposed SIMULINK model of a 3P3W UPQC configuration, supported with wind energy generation system. It consists of a 3-ϕ voltage source rated 400V, 50Hz feeding a critical 3-ϕ load through the power transformers and transmission line. The SAF and PAF are realized using IGBT bridge circuit, gated through the FLC. The 3-ϕ to ground fault having short circuit transition time of [0.15-0.3] s, is also simulated. Similarly, the other proposed configurations namely 2C and 4L topologies is also modeled in the SIMULINK and successfully executed. The UPQC models are placed in between all the branches of an IEEE 14 Bus system and the harmonic analysis of voltage and current waveforms, (for phase A), measured before compensation and after compensation for all the three stated UPQC configurations along with the DG are accomplished. The obtained results are processed through the harmonic FFT analysis.
Fig. 8 shows the voltage waveforms before compensation and after compensation and Fig. 9 represent the current waveforms before compensation and after compensation for 3P3W configuration. Both the figures indicating three phase waveforms in phases A, B and C are represented by the red, blue and green lines respectively.

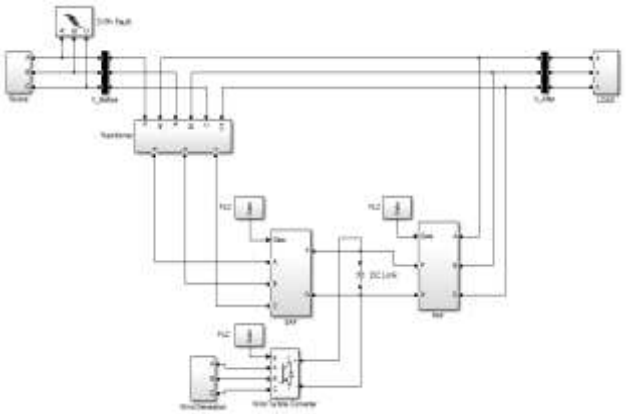


Fig. 7: Simulink model of 3P3W UPQC with DG.

As stated earlier, the fault block is made to operate with the transition time of [0.15-0.3] s, there is observable voltage sag, seen during the mentioned duration, indicated in the waveform labeled 'V_Before Compensation'. Because of the action of SAF, the voltage sag is compensated at a very fast rate and the system is restored back to its normal condition, thereby making the system to operate at a constant stabilized voltage. This action is depicted in the waveform labeled 'V_After Compensation'.

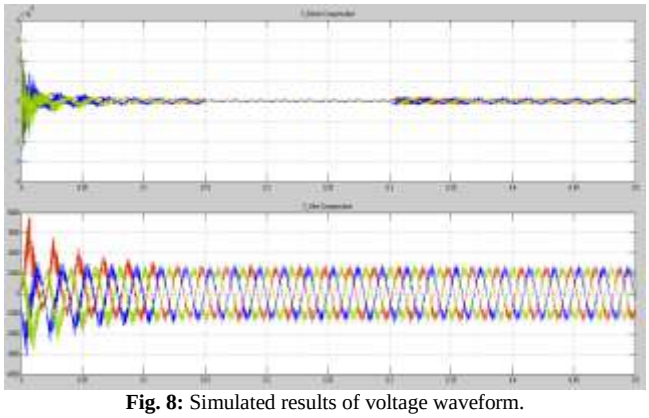


Fig. 8: Simulated results of voltage waveform.

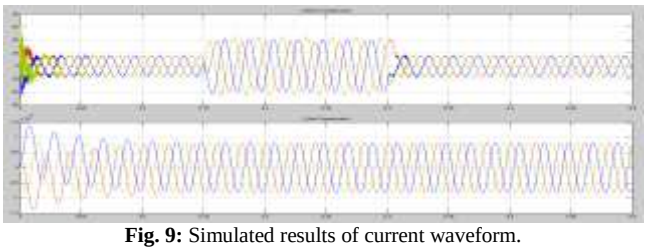


Fig. 9: Simulated results of current waveform.

Similarly, during that interval, the system current also shoots up to a high value as seen in the waveform labeled 'I_Before Compensation'. Due to the swift compensative action of PAF, the system's over current is quenched to a constant stabilized current value, thereby bringing the faulty system into its normal operating condition as indicated in the waveform labeled 'I_After Compensation'. The harmonic data of 3P3W, 3P4W-2C and 3P4W-4L topologies, along with the DG, placed between all the branches of IEEE 14 Bus system are summarized in the bar charts depicted as Fig. 10, Fig. 11 and Fig. 12 respectively.

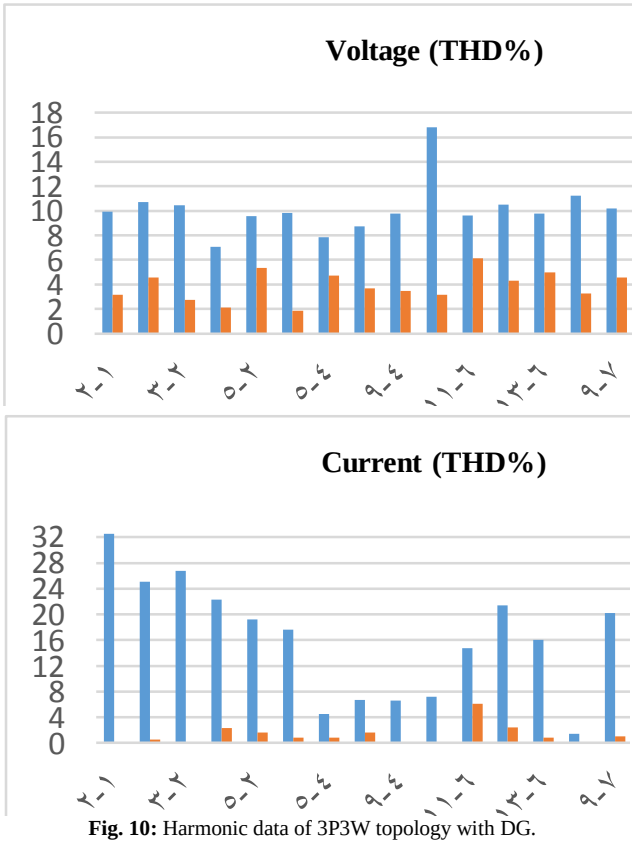
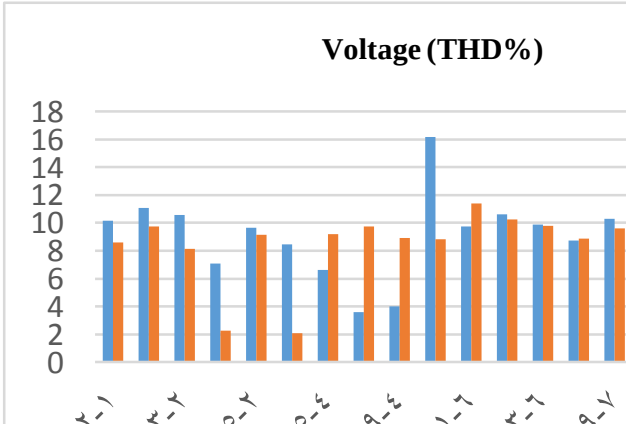


Fig. 10: Harmonic data of 3P3W topology with DG.



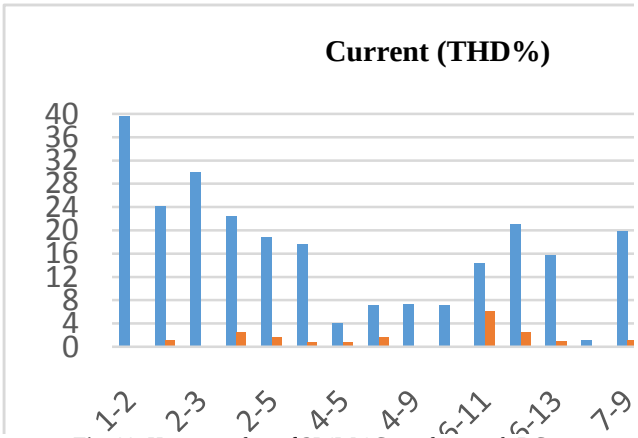


Fig. 11: Harmonic data of 3P4W-2C topology with DG.

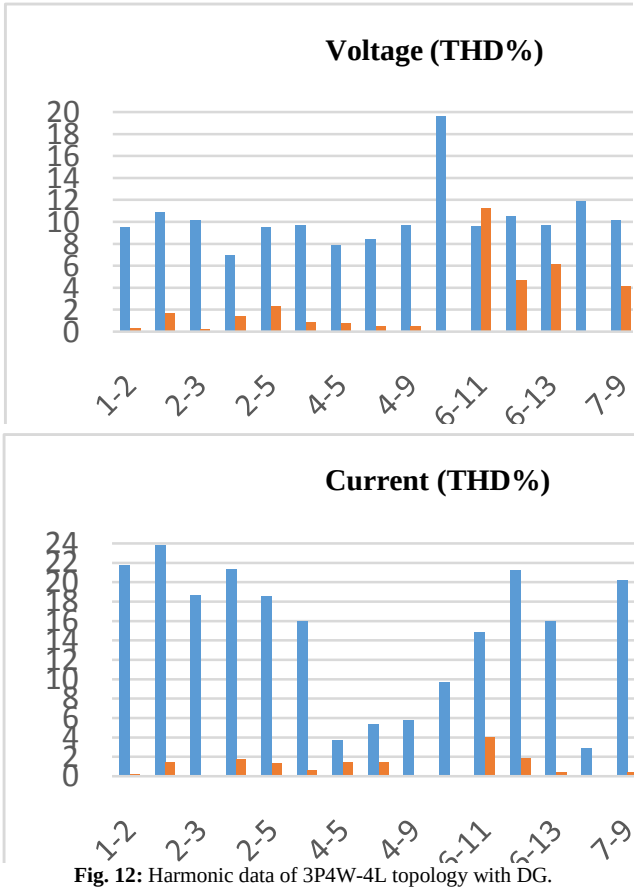


Fig. 12: Harmonic data of 3P4W-4L topology with DG.

6. Conclusion

Power quality issues such as voltage sag and swell are most commonly occurred in power distribution system. To overcome these issues, different topologies of UPQC are proposed in this paper. To enhance the power quality, UPQC with fuzzy logic controller, supported with DG, is implemented in MATLAB Simulink to curtail the voltage sag under different configurations.

From the harmonic analysis, it is clearly indicated that the for 3P3W topology with DG, placing the UPQC in between bus 3 and bus 4 will be the optimal location, where both the voltage and current harmonic level can be drastically reduced to 1.87% and 0.82% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 4 and bus 9 or between bus 7 and bus 8 is an optimal choice, where the current harmonic level is reduced to 0.07%.

Similarly, for 3P4W-2C topology with DG also, placing the UPQC in between bus 3 and bus 4 will be the optimized position

of placement, where both the voltage and current harmonic level can be quenched to 2.08% and 0.84% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 7 and bus 8 is an optimal choice, where the current harmonic level is reduced to 0.03%.

Likely, for 3P4W-4L topology with DG also, placing the UPQC in between bus 7 and bus 8 will be the optimized position of placement, where both the voltage and current harmonic level can be quenched to 0.03% and 0.07% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 2 and bus 3 is an optimal choice, where the current harmonic level is reduced to 0.04%.

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