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Research paper



Development of the Information Storage Micromodule for Spacecrafts with LATCH-UP Effect Protection

R.S. Litvinenko, I.V. Prokofiev

SPC "Technological center", Moscow, Zelenograd, Shokin sq. 1, bld. 7

Abstract

Exposure to outer space ionizing radiation places high demands on the circuits for fault tolerance. The issue of information safety on storage devices is especially acute in conditions of high radiation. Within the framework of the project on development of constructive and technological methods of creation of miniature data storage drives for onboard equipment for space purposes, the study of the radiation effects influence on the operation of memory chips and methods of counteracting these effects is carried out.

Keywords: *FPGA, latch-up effect, microassembly, radiation tolerant memory.*

1. Introduction

To date, one of the fastest growing areas in microelectronics is the creation of radiation – resistant electronic component base for equipment with increased resistance to the effects of outer space ionizing radiation. The driving force in this case is the growing market for launches of spacecraft and transport systems for various purposes. Exposure to ionizing radiation of outer space places high demands on the circuits for fault tolerance. The issue of information safety on storage devices in conditions of high radiation is especially acute.

According to foreign analysts, the further development of technologies will be aimed at meeting the needs in this area, which can significantly affect both the field of electronic technology and the economy as a whole. The development and demand for these products makes the leading electronics companies-manufacturers to develop new technologies and methods of packaging. In particular, a recent development focusing on technology 2.5 D - 3D integration and packaging are demonstrated at the level of the substrate (wafer level packaging) for the manufacture of products, including space applications. According to the Analytics of the authoritative consulting company on market development research, Yole Development, by 2020 modern packaging technologies will account 44% of all services for the assembly of electronics for the needs of customers [1].

As a result, the main direction in the development of techniques and technology is the trend towards miniaturization and increase of the functionality of electronic component base (ECB) and equipment. Moreover, the miniaturization of electronics is not an aim in itself, but rather a way to improve the efficiency of the final product, which contributes to its competitiveness. Since the reduction of the length of interconnections, reducing the size of the end elements leads to higher data rates, lower power consumption, expansion of the equipment's functionality.

In the field of microelectronics, the increase in the integration degree due to the reduction of the size of the final element is already approaching the border of physical capabilities, moreover, the economic feasibility is lost due to the complexity and high cost of technological processes. Moreover, the implementation of the finished device within a single crystal, the so-called SoC (system on chip), requires highly qualified specialists, large time and money spent on development. That is why the miniaturization of the finished device is implemented through the use of the latest assembly methods such as PoP (package on package), SiP (system in package) based on 2.5D and 3D technologies, and other leading world manufacturers started in a technological race, developing new and improving old methods to increase the packaging density. The development of technology that allows to use all modern methods of integration in a single design is very much in demand today and is necessary to create a fundamentally new competitive ECB and products based on it, especially for devices with high resistance to the effects of outer space ionizing radiation.

2. Literature Review

The problem of radiation resistance of integrated circuits (IC) comes out in the foreground, as in many cases it is radiation failures will determine the period of spacecraft active existence. At the same time, as the integration degree increases, local radiation effects come to the fore, which cause failures due to the impact of individual high-energy nuclear particles [2,3].

Radiation effects in electronics are most often divided into two types: cumulative dose effects, known as total ionizing doze (TID), and single effects or single event effects (SEE).

The effects of TID are related to the accumulation of charge inside the silicon structure, which lead, for example, to an increase in delays within the integrated circuit (IC) or a change in the stresses of field transistors cut-off and logical levels. Initially, the TID effects are manifested in the form of device parameters degradation, which then lead to failure. TID is measured in rad units where 1 rad is equal to 100 ergs per gram of material. The increase of chip resistance to TID effects is achieved mainly due to technological methods and shielding. The technological methods consist in the application of SOI (silicon on insulator) structures, reducing the thickness of the sub-gate dielectric of the MOSFET transistor, as well as the introduction of epitaxial layers under areas with a high dose of alloying. Shielding allows to absorb the most part of electrons and protons with low energy. Thus, the layer of 2 mm

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aluminium reduces the accumulated dose of cosmic radiation 100 times [4], but to reduce the dose two orders of magnitude more, it will require protection with a thickness of 8 mm. This paradox is easily explained by the fact that the composition of cosmic rays is non-uniform. If low-energy particles tend to linger in a thin screen, high-energy particles can easily penetrate it. Moreover, high-energy particles are able to knock particles out of the screen material, thereby creating secondary radiation.
The most common failures are detected in ICs with medium and high integration degree made on CMOS technology, in which local radiation effects of heavy charged particles and high-energy protons can develop a single latch-up effect. Latch-up effect is usually accompanied by the flow of high currents through the power supply chain, which can lead to IC heating and catastrophic failure (CF).
Increased sensitivity to latch-up effect in CMOS ICs is usually a strong argument for the refusal of the installation of the microelectronics product on the spacecraft. However, due to the inability to implement in another technological basis CMOS ICs, sensitive to latch-up effect, are often used in functionally complex products. In this case it is necessary to ensure the protection from CF.
Reversibility of the latch-up effect is the key feature to restore the IC functioning: when the power is turned off, the thyristor structure is turned off, and when the power is turned on again in specific time, the crystal temperature is reduced and the full efficiency and parameters of the IC are expected to be restored. This is the main principle to parry the latch-up effect in ICs.

The effect may occur in the form of micro-latch-up [5]. The consumption current at the same time increases significantly less than with conventional latch-up effect. Therefore, it is necessary to carefully approach the selection of critical current values, when the protected IC is disconnected from the power supply, in addition, in some cases, small increments of currents are difficult to distinguish against the background of large working dynamic consumption currents [6].
The most common principles for parrying the latch-up effect are:
- consumption current limit;
- short-term power off;
- suppression of "rush" current when the latch-up effect is occurred.

Current consumption is limited by an external power supply or current limiting resistor in order to reduce the current density in the latch-up position. This approach can be used if the current consumption of the IC is relatively small, and the current limit does not lead to a decrease in the supply voltage of the IC.
It should be mentioned that limiting the current consumption of the protection circuits in power supplies is an inertial proccess and may limit only the steady-state current of the enabled thyristor structure, thus the instantaneous current density, until they reach the steady-state value, can reach critical levels and lead to catastrophic failure [7].
The second approach is to parry the latch-up effect and prevent CF - short-term power switch off when detecting latch-up. This is a universal method of parrying the latch-up effect, which is most widely used. In this case the equipment reaction time is of great importance. Depending on the properties of the protected IC or module, it is necessary to choose hardware, software or combined methods for detection and parrying the latch-up, taking into account the characteristics of the IC and the CF occurrence time.
The third approach to prevent CF in the IC (suppression of "rush" current when the latch-up effect is occurred) is associated with the use of capacitors in IC power circuits that block high-frequency noise. Suppression of the" rush" current when switching on the thyristor structure is possible by increasing the time constant of the IC supply circuit, taking into account its own capacity on the power pins, while reducing the capacity of the blocking capacitors on the supply. It is obvious that such measures can lead to unacceptable deterioration of the IC performance and decrease in the stability of the supply voltage directly at the IC terminals, so the applicability of this approach is required to be determined by testing in electrical power and loading modes close to those in the equipment.

3. Methods

The study object is the micromodule prototype for information storage for spacecraft onboard equipment. The micromodule prototype has flash memory, latch-up protection chip and a programmable logic integrated circuit, which implements controller. The electric circuit of the micromodule is shown on figure 1.
The main advantage of the micromodule is that it is developed by 3D-integration technology. Small footprint is one of the most important factors for space applications. At the same time, the technology does not require special equipment, what reduces the price of the final product.
The controller performs tasks of information access, reading, writing to memory chips. The task of the controller is also to increase the radiation resistance of the micromodule by applying corrective codes. The controller can be implemented on the basis of an uncommitted logic array (ULA) or a field-programmable gate array (FPGA).
The ULA 5503 series, developed in SMC "Technological Centre", can be used as a base for micromodule controller.
The ULA 5529 series is a more advanced development than the 5503 series and is the preferred option at the time of the final product manufacture. Manufacturing technology can significantly reduce signal delay time and improve performance.
However the controller implementation on the FPGA chip is a more flexible method, since the logic of the FPGA is set not during the manufacturing process, but through programming. The necessary structure of the device can be implemented in the form of an electrical circuit or by programming languages Verilog or VHDL. The total number of valves in the scheme can reach from several thousand to several million. Programming the FPGA connects these elements in the desired pattern [8].
Another advantage of FPGA is the ability to transfer the controller project to ULA in a short time. This option is preferred for this project, as it allows to debug the operational logic using the flexibility of FPGA, and then transfer the project to the more reliable ULA.
As one of the main reasons of chip failures in space is the latch-up effect, it is necessary to include in the micromodule the latch-up protection chip 1469TK025 developed in SMC "Technology Centre". 1469TK025 is radiation tolerant and based on SOI structure. The working principle is based on control of the current consumption of the protected circuits. The chip switches off these circuits when the current exceeds the defined level of consumption [9]. In the micromodule one latch-up protection chip is applied (Fig. 1). Chip 1469TK025 monitors the current consumption level of all 4 memory chips and in case of exceeding the threshold of operation turns off the memory chips power and transfers all signal outputs to the ground. After the specified time, the 1469TK025 chip restores power and returns the micromodule to normal operation.
This approach allows to realize the latch-up protection, but in case of activation leads to temporary exclusion of the whole micromodule from the operation process. At the same time, the use of one protection chip saves space and reduces the micromodule size.
From the point of view of radiation resistance the best choice is a single-level memory type NAND-Flash [10,11]. The method of reserving memory to increase the resistance to single effects should be implemented by using four memory chips in one micromodule. This means that copies of the data are stored on each of the flash memory chips.

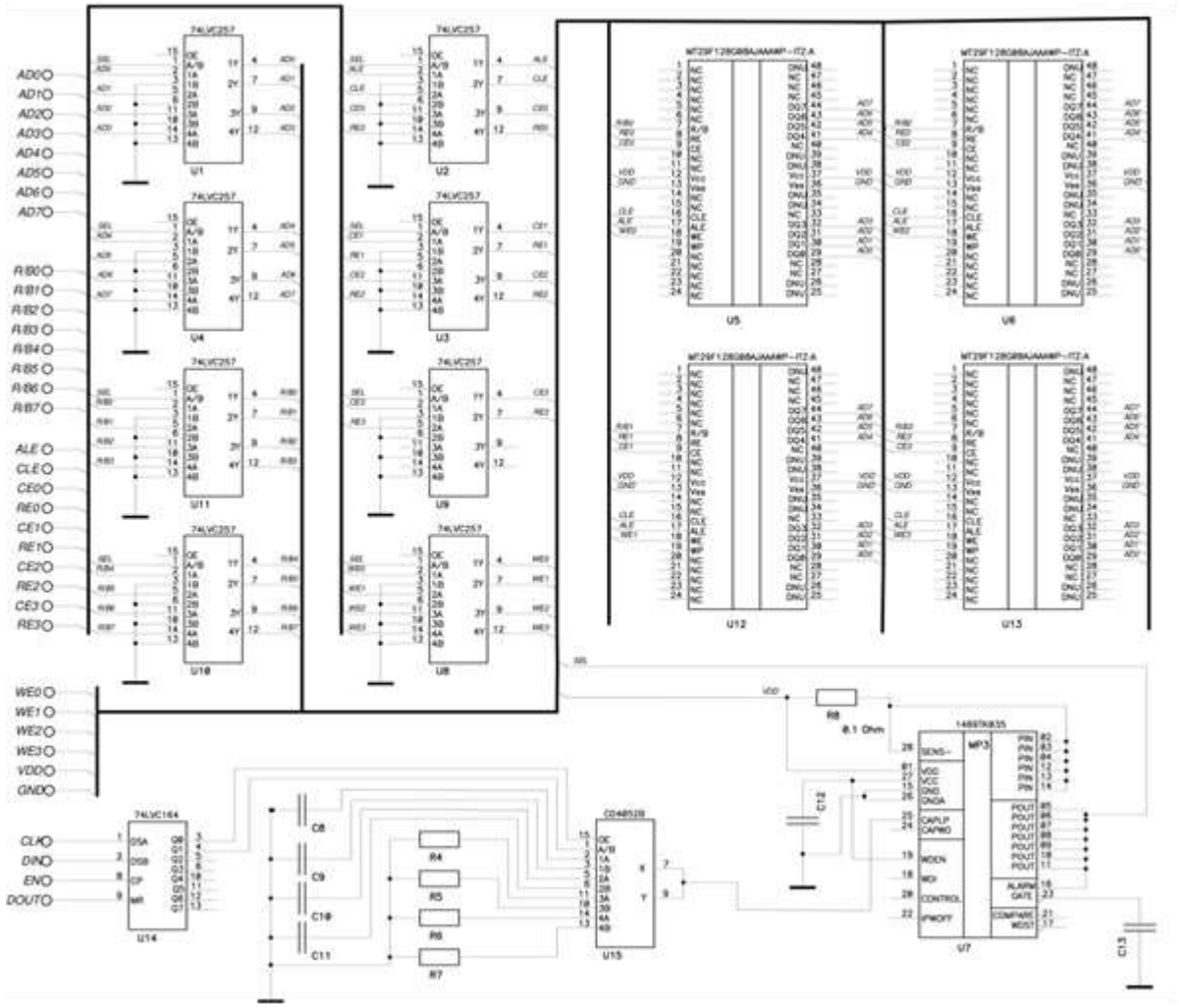


Figure 1 : micromodule electric scheme

4. Results

The micromodule sample is implemented as microassembly with dimensions 16x23x10.5 mm.

The micromodule controller is implemented on the basis of FPGAs of Xilinx company. The choice is made in favor of the manufacturer due to the wide range of chips and suitable characteristics. In addition, Xilinx produces space-grade chip family Virtex-5QV, which can be used in further development.

The chip involves 55 signal terminals. According to the simulation results in the Xilinx ISE program, the signal delay in the FPGA is 4.24 ns.

The bidirectional data bus is organized in the way the latch-up protection is activated, the current does not flow through the inputs of the memory chips. The module uses flash memory MICRON. According to the radiation resistance studies chip MT29F128G08AJAAAWP-ITZ:A have the following sensitivity characteristics to the effects of heavy charged particles: catastrophic failure - 69 MeV*cm2/mg [Si] with the cross-section of 2.5*10-10 cm2/bit. These values allow the use of the chips on shielded equipment operating on Earth orbit.

One of the most important characteristics of the micromodule is its performance speed. The studies of the reading time in the temperature range from minus 50 to +70 °C at Vdd +4.0 V ... + 1.8 V are shown on figure 2. The measurement of the delay time was carried out using an oscilloscope: the first channel was connected to the digital control input, the second channel to the data output. The load capacity was 5 pF.

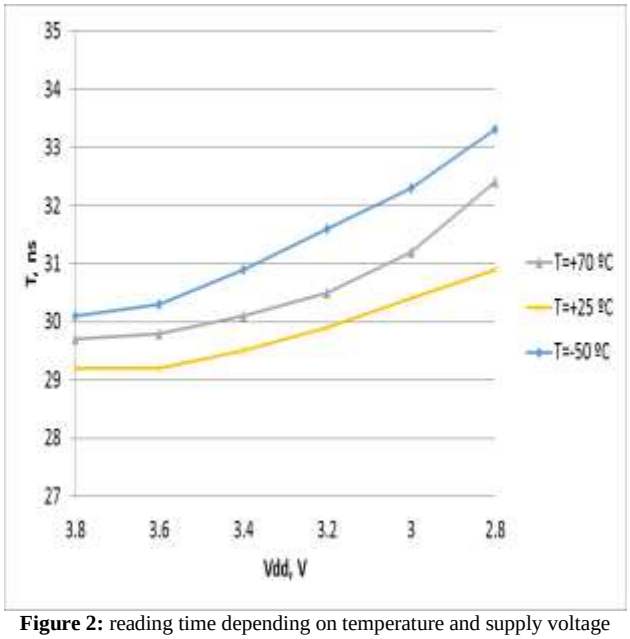


Figure 2: reading time depending on temperature and supply voltage

It is established that the reading time does not exceed 33 ns in the entire temperature range, which meets the requirements of the technical specification. It is expected that the reading time will be reduced to values less than 30 ns on samples with controller based on ULA. Micromodule characteristics meet the requirements of the project technical specifications.

5. Conclusions

The paper presents the main aspects of the development of the micromodule for operational storage of information for use in the onboard equipment for space purposes. According to the research results, the most common cause of catastrophic failures of microelectronic devices in the conditions of the space ionizing radiation is the latch-up effect. Among the considered methods of dealing with latch-up effect, it is most advisable to use the method of short-term power off. The advantage of this method is a relatively simple circuit implementation and the absence of a significant impact on the performance of the module. The reading time does not exceed 33 ns over the entire module temperature range. After the implementation of the controller on ULA, it is planned to test the micromodule for radiation resistance.

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