International Journal of Engineering & Technology, 7 (4.6) (2018) 177-180

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper



Harmonic cancellation in a Multi-level Inverter Configuration Suitable for PV Applications

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Abstract

Multi-level inverters are playing a major role in PV based systems because of numerous advantages like low dv/dt, better harmonic profile so on. But, conventional multi-level inverters consist of some drawbacks like capacitor balancing issues, greater requirement of capacitor banks and clamping diodes. To address these issues, a novel multi-level inverter has been presented in this paper, which can function as a seven-level, five-level and three-level inverter. The inverter circuit utilizes six switching devices and two isolated DC voltage sources. Moreover, when it is operated as a three-level inverter, a unipolar PWM technique is applied to the circuit which shifts all the lower order harmonics to twice of switching frequency whereas in conventional multi-level inverters, all the harmonics of lower order are present around switching frequency. In addition, proposed inverter can operate even if some switching devices of the circuit fails. Also, the behavior of the inverter during the failure of some switching devices and DC source is analyzed. The proposed inverter is simulated in MATLAB/Simulink and the results are also discussed.

Keywords: *Fault tolerant inverters; Multi level- inverters; PV applications; Sine-Triangle PWM.*

1. Introduction

Power generation using PV systems is becoming more popular due to lack of availability of fossil fuels [1]. As power generated with PV system is DC, inverters are required to converter it into AC quantity. But conventional two-level inverters which are popularly used has more harmonic component in the output voltage which deteriorates the lifetime of the load [2]-[5]. Moreover, if any switch of a two-level inverter fails, entire system will not function. Also, the rate of rise of output voltage (dv/dt) of this inverter is also significantly high [6]-[7]. All the aforementioned issues can be rectified by using multilevel inverters [8]-[9]. Traditional multilevel inverters have some major draw backs like capacitor voltage variations and requirement of capacitor banks so on [10]-[12]. To address these issues, several multilevel inverter circuits were presented in the literature. An interesting multi-level inverter configuration is introduced in [13] which produces five-level output voltage by utilizing the conventional two-level inverter. Consequently, the problems related with conventional multi-level inverters are minimized. The major disadvantage of this inverter circuit is that it requires higher number of switching devices when compared to traditional multi-level inverter. Further, the reliability of an inverter circuit is also an important issue when it is supplying the critical load. Conventional multilevel inverters will not operate if there is a failure of any one switch in the circuit, which may occur due to various reasons like aging, miss firing, dv/dt, over voltage, overt current etc. To address the reliability issue, a five-level inverter circuit is introduced in [14], which is developed by using seven switching devices and two isolated dc voltage sources. By extending this concept, a seven-level inverter circuit has been presented in this paper employing only six switching devices. Moreover, first center band harmonics are cancelled by using a unipolar pwm technique when the inverter is operated as a three-level inverter.

2. Design of Multi-level Inverter and PWM Technique

Fig.1 presents the power circuit of a multi-level inverter configuration which consists of six control switches, in which four are two quadrant switches and two are four quadrant switches. Four quadrant switches can be designed by using four uncontrolled switches and one controlled switch or it can also be designed by connecting two controlled switches in anti-series. Based on switching pattern, it can be operated as three-level, five-level and seven-level inverter. For a three-level inverter case, S1 and S2 forms one half bridge and S3 and S4 are forms the other half bride of an inverter. Gating pulses are not given to S5 and S6 switches thereby keeping these two switches as open. By using the pulse width modulation technique shown in Fig.2, first center band harmonics can be cancelled. Hence, all the lower order harmonics will appear at twice the switching frequency. In this PWM technique, gating pulses for inverter one are generated by using a sine wave and a carrier wave as shown in Fig. 2(a), where phase shift between these two signals is equal to zero. Similarly, gating signals for inverter-2 are generated by using a sine wave with a phase shift of 180^0 and a carrier wave with a phase shift of zero as shown in Fig. 2(b). By giving these gating signals, harmonic cancellation at first center band can be achieved and it is presented in the results section. This harmonic cancellation is possible only when this inverter functions as three-level inverter. The same inverter circuit can also be used to generate five-level voltage wave-

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form by operating the switches S1-S6 in a sequence as shown in Table-1. Similarly, the switching logic to generate seven-level voltage waveform from the same inverter circuit is also shown in Table-1. Current direction for various voltage levels is presented in Fig. 3. In this case, Vdc1 is taken as 2V and Vdc2 is taken as V. The seven voltages are denoted as 3V, 2V, V, 0, -V, -2V and -3V. In order to produce 3V at the output of inverter, load must be connected across two series connected dc voltage sources. Similarly, 2V can be produced by connecting load across Vdc1 and by triggering suitable switching devices as shown in Fig. 3(b). In order to produce V across load terminals, load must be connected across Vdc2. To produce zero inverter output voltage, load terminals are short circuited as shown in Fig 3 (d). Similarly –V, -2V and -3V are produced across load by connecting dc voltage sources in the reverse direction by suitable switching the devices.

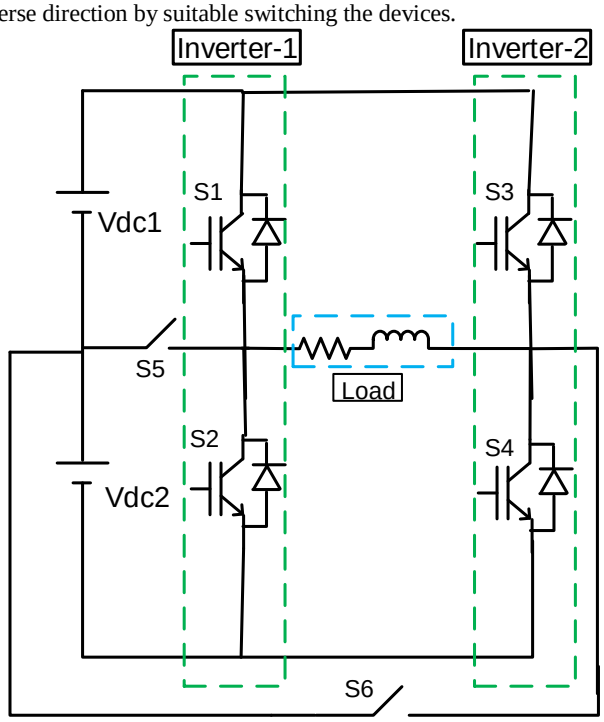


Fig. 1: Multi-level Inverter Configuration.

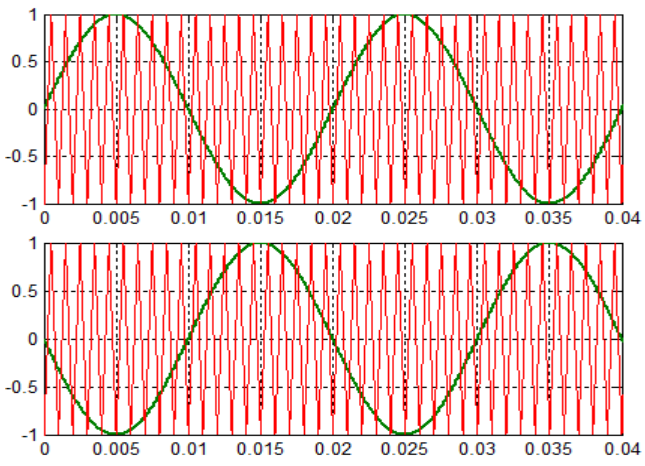


Fig. 2: Unipolar PWM technique for harmonic cancellation.

Table I: switching Combinations For Different Levels

	S1	S2	S3	S4	S5	S6
3V	1	0	0	1	0	0
2V	1	0	0	0	0	1
V	0	0	0	1	1	0
0	0	0	1	1	0	0
-V	0	0	1	0	0	1
-2V	0	1	0	0	1	0
-3V	0	1	1	0	0	0

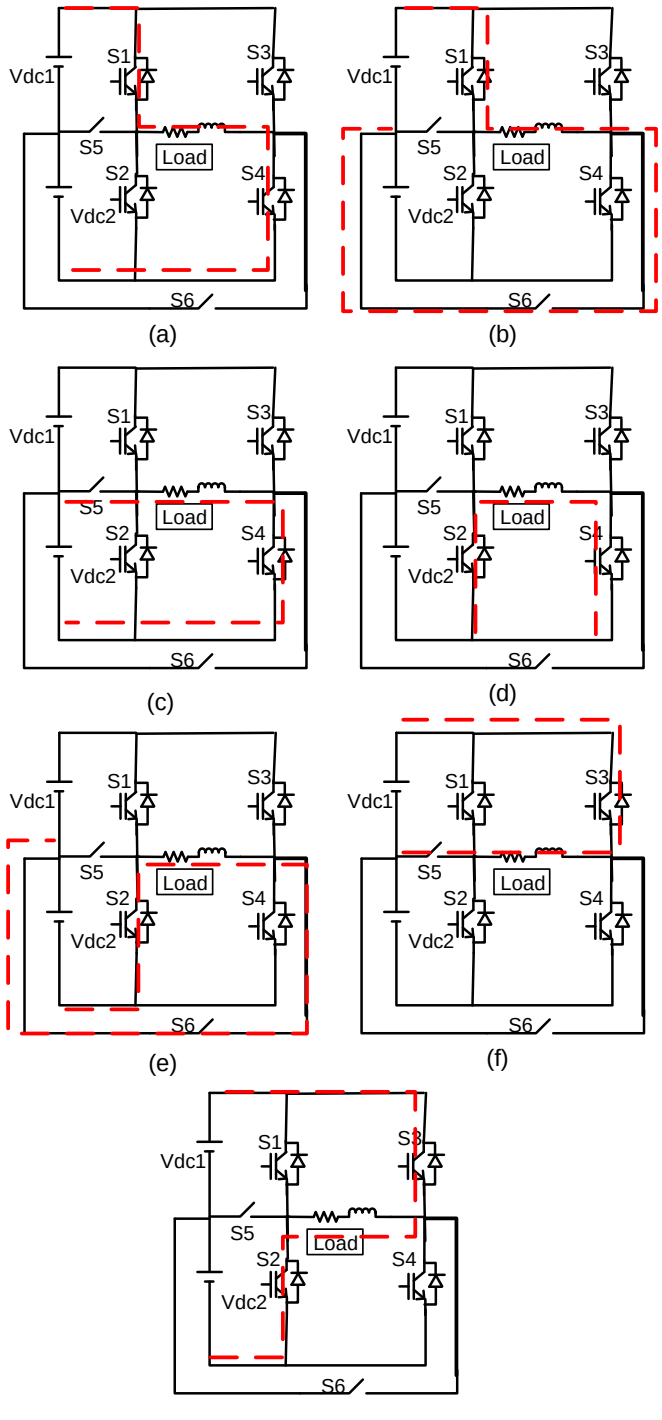


Fig. 3: Power circuits for getting five-level voltage wave forms (a) 3V (b) 2Vdc (c) V (d) Zero (e) –V (f) -2V and (g) $-V_{dc}$.

The main advantage of this circuit is it uses less number of switching devices to produce seven-level output voltage, whereas conventional seven-level inverter requires 12 switching devices. As the requirement of switching devices is more, control circuit and power circuit complexity will be increased considerably and also the cost will be increased. Moreover, in conventional multi-level inverters, there are some problems like capacitor voltage balancing issue, requirement of bulk size capacitors and requirement of higher number of dc voltage sources so on. All these problems can be eradicated with this proposed inverter configuration. The switching logic for seven level inverter is presented in Fig. 4, in which one modulating signal and six (n-1) carrier signals are utilized to produce the gating signals.

By providing 180^0 phase shift between modulating signals, harmonics will be shifted to two times the switching frequency. The harmonic spectrum of output voltages will be presented to show the cancellation of harmonics at first center band and it is presented in the next section.

3. Results and Discussion

The proposed inverter configuration has been simulated in MATLAB/Simulink and results are presented in this section.

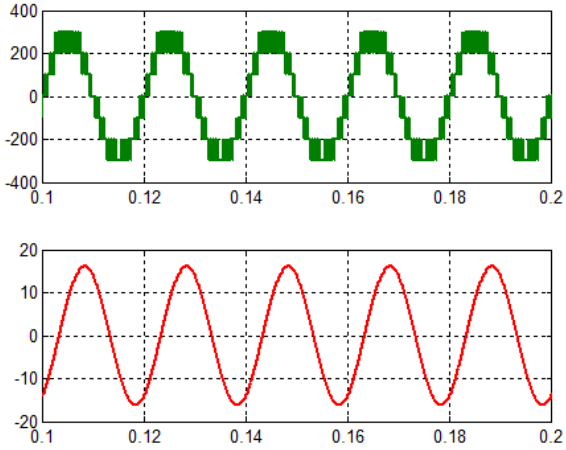


Fig.4: Load voltage (top trace) and load current (bottom trace)of a seven-level inverter.

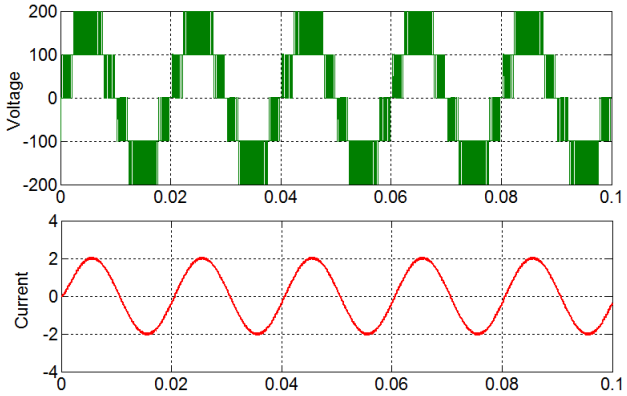


Fig.5: Load voltage (top trace) and load current (bottom trace)of a five-level inverter.

The magnitude of dc source voltage, V_{dc} is taken as 100V. The load considered is RL load with the R= 10Ω and L = 50mH.
The waveforms of load voltage and current when inverter is operated for a seven level output are shown in Fig. 4. It is clear from the figure that seven-level voltage waveform is produced by employing the switching pattern given in Table-1. As total voltage is divided into seven levels, dv/dt of the output voltage is also reduced. It is evident from Fig.4 that current waveform is sinusoidal and the voltage waveform is almost sinusoidal.

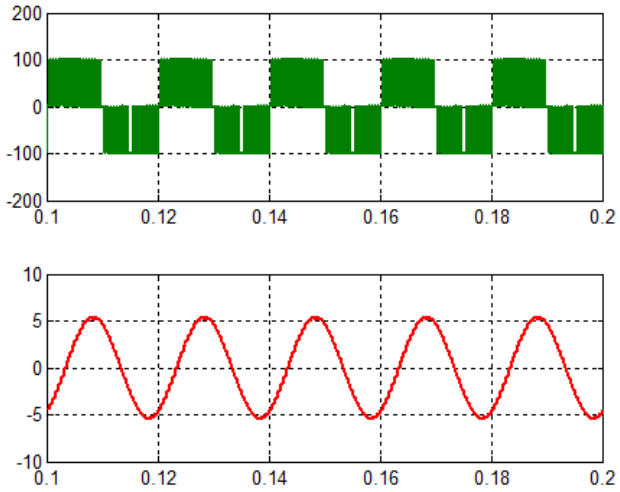
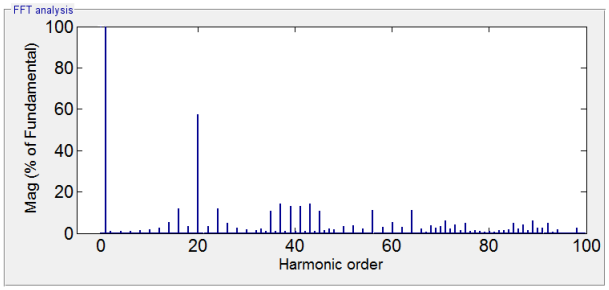


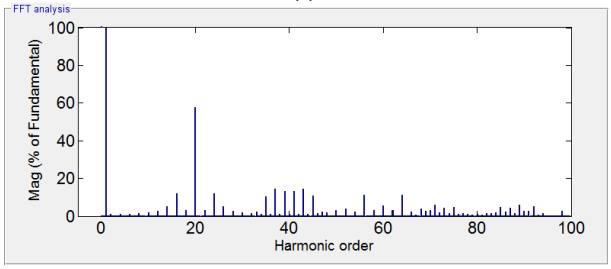
Fig.6: Load voltage (top trace) and load current (bottom trace)of a three-level inverter.

Fig.5 shows the five-level inverter output voltage and current which is generated by using same inverter circuit with small changes in gating pulses of the inverter switches. Three-level voltage waveform is shown in Fig.6 which will be produced when an unexpected failure of some switching devices occurs. Fig. 7(a) shows harmonic spectrum of two-level inverter pole voltage where harmonics are present near to first center band which is equal to switching frequency. Similarly, Fig. 7(b) shows the harmonic spectrum of other two-level inverter pole voltage where harmonics are present near to first center band.

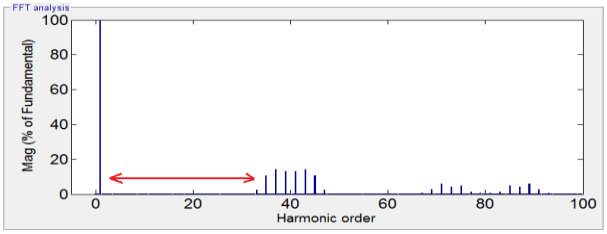
As the modulating signals of two two-level inverters are phase shifted by 180^0, all odd center band harmonics are also phase shifted by 180^0. Since the effective voltage is the difference of both inverter pole voltages, all odd center band harmonics are cancelled.



(a)



(b)



(c)

Fig.7: Harmonic spectrum of output voltage (a) Harmonic spectrum of two-level inverter pole voltage (b) Harmonic spectrum of three-level inverter pole voltage (c) Harmonic spectrum of total voltage.

Hence by employing the proposed inverter configuration and PWM technique, all center band harmonics are shifted to twice the switching frequency.

4. Conclusion

This paper proposes an inverter configuration which produces seven level, five level and three level output voltages by selecting a suitable switching pattern. Further, when it functions as three-level inverter, all the harmonics are shifted to twice the switching frequency without increasing the switching frequency. To achieve this, decoupled SPWM technique is used. Harmonic spectrum and voltage waveforms of different levels are presented to show the efficacy of the inverter. Moreover, the proposed configuration utilizes lesser number of switches and also the control complexity is greatly reduced when compared to traditional seven-level inverter. The same inverter can be operated as a five-level inverter and three-level inverter during the failure of different switching devices which is not possible in conventional neutral point clamped inverter/flying capacitor inverter. Also, the number of voltage levels can be increased further by cascading these units.

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